



NMC2147H 4096 x 1-Bit Static RAM

General Description

The NMC2147H is a 4096-word by 1-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

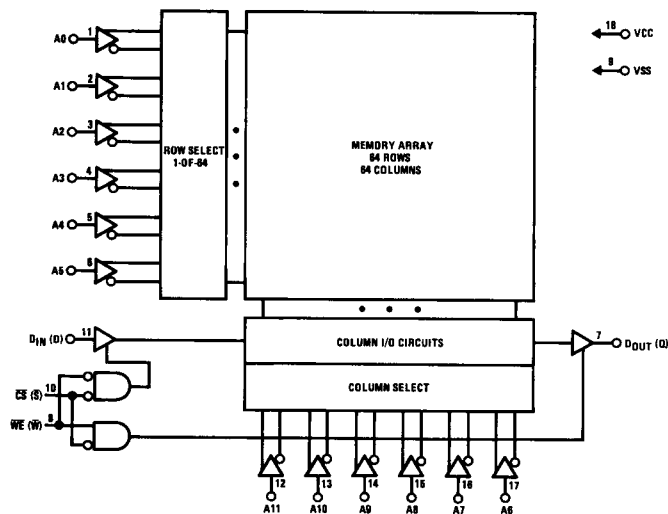
The separate chip select input automatically switches the part to its low power standby mode when it goes high.

The output is held in a high impedance state during write to simplify common I/O applications.

Features

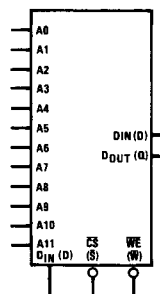
- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Automatic power-down
- High-speed—down to 35 ns access time
- TRI-STATE® output for bus interface
- Separate Data In and Data Out pins
- Single +5V supply
- Standard 18-pin dual-in-line package
- Available in MIL-STD-883 class B screening

Block Diagram*



TL/D/5257-1

Logic Symbol*



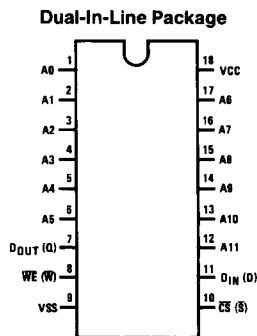
TL/D/5257-2

Pin Names*

- A0-A11 Address Inputs
- WE (W) Write Enable
- CS (S) Chip Select
- D_{IN} (D) Data In
- D_{OUT} (Q) Data Out
- V_{CC} Power (5V)
- V_{SS} Ground

**Order Number NMC2147HJ-1,
NMC2147HJ-2, NMC2147HJ-3,
or NMC2147HJ-3L
See NS Package Number J18A**

Connection Diagram*



TL/D/5257-3

Top View

*The symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Relative to VSS	-3.5V to +7V
Storage Temperature Range	-65°C to +150°C
Power Dissipation	1.2W
DC Output Current	20 mA
Bias Temperature Range	-65°C to +135°C
Lead Temperature (Soldering, 10 sec.)	300°C

Truth Table*

\overline{CS} (S)	\overline{WE} (W)	DIN (D)	DOUT (Q)	Mode	Power
H	X	X	Hi-Z	Not Selected	Standby
L	L	H	Hi-Z	Write 1	Active
L	L	L	Hi-Z	Write 0	Active
L	H	X	DOUT	Read	Active

DC Electrical Characteristics $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$ (Notes 1 and 2)

Symbol	Parameter	Conditions	NMC2147H-3L		NMC2147H-1 NMC2147H-2 NMC2147H-3		NMC2147H		Units
			Min	Max	Min	Max	Min	Max	
I _L	Input Load Current (All Input Pins)	V _{IN} = 0V to 5.5V, V _{CC} = Max		10		10		10	μA
I _{LO}	Output Leakage Current	$\overline{CS} = V_{IH}$, V _{OUT} = GND to 4.5V, V _{CC} = Max		50		50		50	μA
V _{IL}	Input Low Voltage		-3.0	0.8	-3.0	0.8	-3.0	0.8	V
V _{IH}	Input High Voltage		2.0	6.0	2.0	6.0	2.0	6.0	V
V _{OL}	Output Low Voltage	I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{OH}	Output High Voltage	I _{OH} = -4.0 mA	2.4		2.4		2.4		V
I _{CC}	Power Supply Current	V _{IN} = 5.5V, T _A = 0°C, Output Open		125		180		160	mA
I _{SB}	Standby Current	V _{CC} = Min to Max, $\overline{CS} = V_{IH}$		20		30		20	mA
I _{PO}	Peak Power-On Current	V _{CC} = V _{SS} to V _{CC} Min, $\overline{CS} = \text{Lower of } V_{CC} \text{ or } V_{IH} \text{ Min}$		30		40		30	mA

Capacitance $T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$ (Note 3)

Symbol	Parameter	Conditions	Min	Max	Units
C _{IN}	Address/Control Capacitance	V _{IN} = 0V		5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V		6	pF

Note 1: The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

Note 2: These circuits require 500 μs time delay after V_{CC} reaches the specified minimum limit to ensure proper orientation after power-on. This allows the internally generated substrate bias to reach its functional level.

Note 3: This parameter is guaranteed by periodic testing.

AC Test Conditions

Input Test Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Level	1.5V
Output Timing Reference Level (H-1)	1.5V
Output Timing Reference Level (H-2, H-3, H-3L)	0.8V and 2.0V
Output Load	See Figure 1

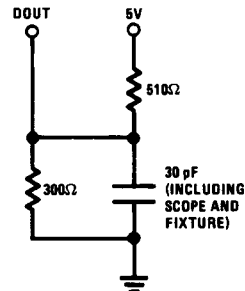


FIGURE 1. Output Load

TL/D/5257-4

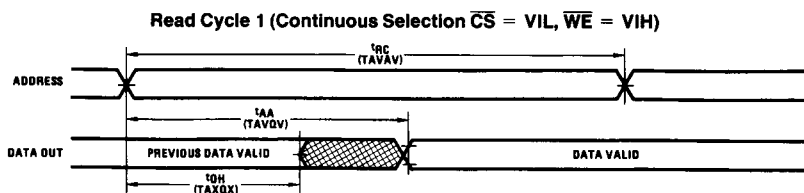
*Symbols in parentheses are proposed industry standard.

Read Cycle AC Electrical Characteristics $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 10\%$ (Note 1)

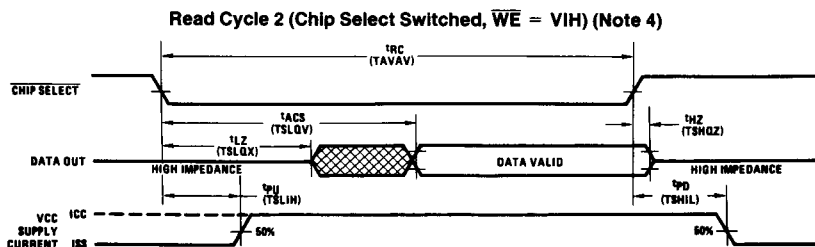
Symbol		Parameter	NMC2147H-1		NMC2147H-2		NMC2147H-3 NMC2147H-3L		NMC2147H		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	35		45		55		70		ns
t_{AA}	TAVQV	Address Access Time		35		45		55		70	ns
t_{ACS}	TSLQV	Chip Select Access Time (Notes 4)		35		45		55		70	ns
t_{LZ}	TSLQX	Chip Select to Output Active (Note 5)	5		5		10		10		ns
t_{HZ}	TSHQZ	Chip Deselect to Output TRI-STATE (Note 5)	0	30	0	30	0	30	0	30	ns
t_{OH}	TAXQX	Output Hold from Address Change	5		5		5		5		ns
t_{PU}	TSLIH	Chip Select to Power-Up	0		0		0		0		ns
t_{PD}	TSHIL	Chip Deselect to Power-Down		20		20		20		30	ns

Max Access/Current	NMC2147H-1	NMC2147H-2	NMC2147H-3	NMC2147H-3L	NMC2147H
Access (TAVQV—ns)	35	45	55	55	70
Active Current (ICC—mA)	180	180	180	125	160
Standby Current (ISB—mA)	30	30	30	20	20

Read Cycle Waveforms*



TL/D/5257-5



TL/D/5257-6

Note 4: Addresses must be valid coincident with or prior to the chip select transition from high to low.

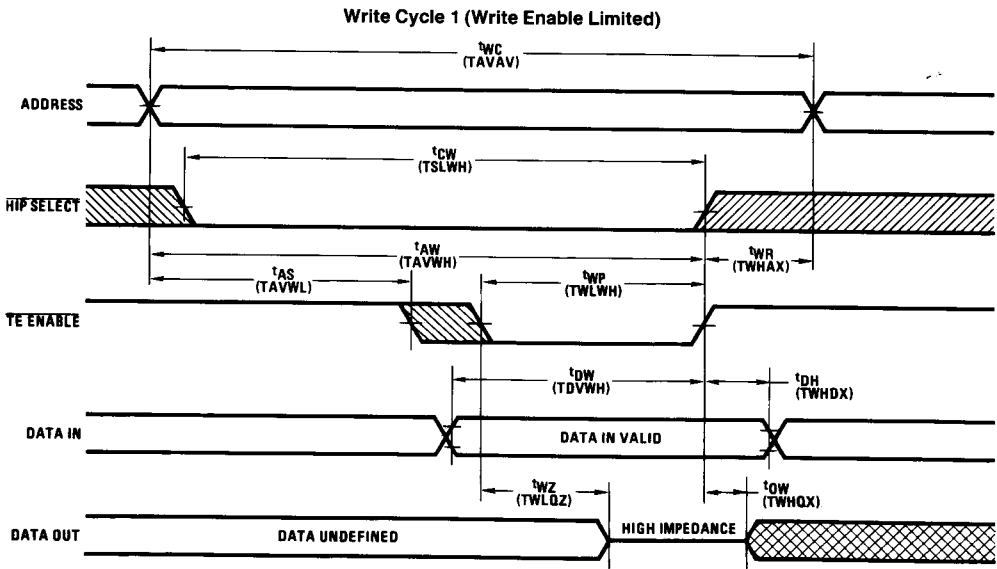
Note 5: Measured ± 50 mV from steady state voltage. This parameter is sampled and not 100% tested.

*The symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics TA = 0°C to 70°C, VCC = 5V ± 10% (Note 1)

Symbol		Parameter	NMC2147H-1		NMC2147H-2		NMC2147H-3 NMC2147H-3L		NMC2147H		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	Min	Max	
t _{WC}	TAVAV	Write Cycle Time	35		45		55		70		ns
t _{CW}	TSLWH	Chip Select to End of Write	35		45		45		55		ns
t _{AW}	TAVWH	Address Valid to End of Write	35		45		45		55		ns
t _{AS}	TAVSL TAVWL	Address Set-Up Time	0		0		0		0		ns
t _{WP}	TWLWH	Write Pulse Width	20		25		25		40		ns
t _{WR}	TWHAX	Write Recovery Time	0		0		10		15		ns
t _{DW}	TDVWH	Data Set-Up Time	20		25		25		30		ns
t _{DH}	TWHDX	Data Hold Time	10		10		10		10		ns
t _{WZ}	TWLQZ	Write Enable to Output TRI-STATE (Note 5)	0	20	0	25	0	25	0	35	ns
t _{OW}	TWHQX	Output Active from End of Write (Note 5)	0		0		0		0		ns

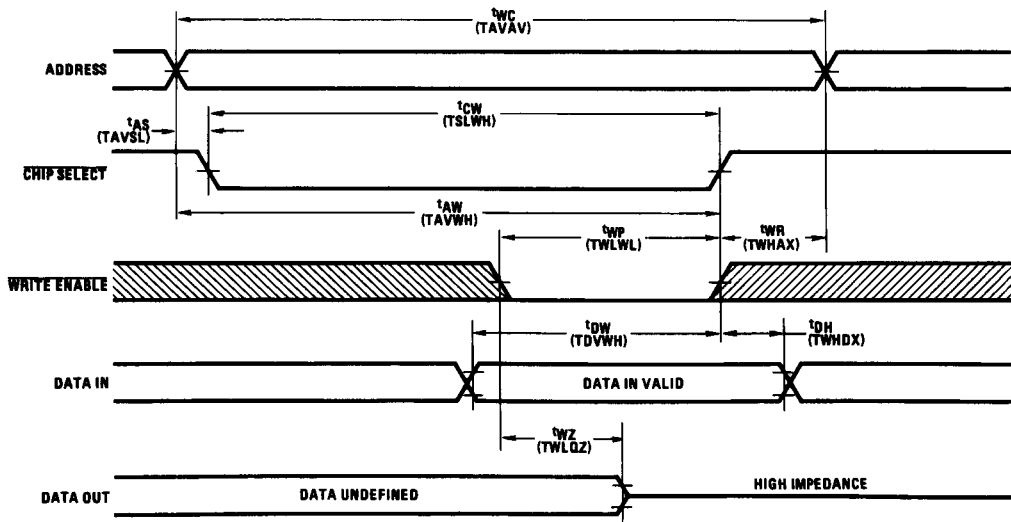
Write Cycle Waveforms* (Note 6)



TL/D/5257-7

Write Cycle Waveforms* (Note 6)

Write Cycle 2 (Chip Select Limited)



TL/D/5257-8

Note 6: The output remains TRI-STATE if the \overline{CS} and \overline{WE} go high simultaneously. \overline{WE} or \overline{CS} or both must be high during the address transitions to prevent an erroneous write.

*The symbols in parentheses are proposed industry standard.