

## Dual Output Differential Speed and Direction Sensor IC

### FEATURES AND BENEFITS

- High-speed switching bandwidth up to 40 kHz
- Two independent output channels with options for high resolution XOR speed, pulse, and direction protocol
- ASIL B(D) compliant (ISO 26262)
- Optional fault detection output protocol
- Immune to common external magnetic disturbance
- EEPROM enables factory traceability throughout product life cycle
- Ideally suited for asynchronous electric motor applications



### PACKAGE:



4-Pin SIP  
(suffix SG)

Not to scale

### DESCRIPTION

The ATS17501 is a single IC solution designed for rotational position sensing of a ferrous gear target found in automotive and industrial electric motor applications (often with specific application and safety requirements). The IC is housed in an SG package that incorporates a rare-earth magnetic pellet for ease of manufacturing, consistent application performance over temperature, and enhanced reliability.

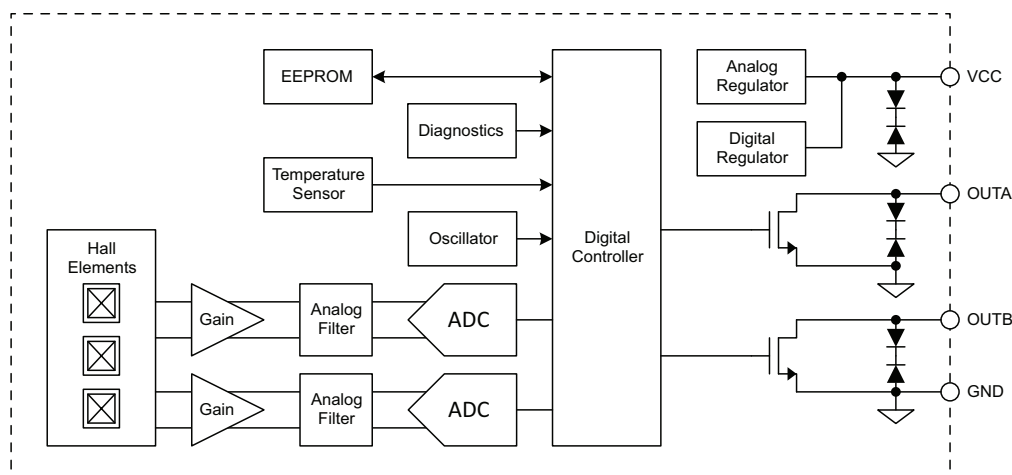
Three Hall elements are incorporated to create two independent differential channels. These inputs are processed by digital circuits and robust algorithms designed to eliminate the detrimental effects of magnetic and system offsets, and to address false output transitions caused by target vibrations in electric motors at startup and low speed operation. The differential signals are used to produce a highly accurate speed output and, if desired, provide information on the direction of rotation.

Advanced calibration techniques are used to optimize signal offset and amplitude. This calibration, combined with the digital tracking of the signal, results in accurate switch points over air gap, speed, and temperature.

The IC can be programmed for a variety of applications requiring dual-phase gear speed and position signal information or simultaneous high-resolution gear speed and direction information. It can be configured to enable Fault Detection mode for ASIL B(D) utilization.

The ATS17501 SG package is a lead (Pb) free 4-pin SIP package with an integrated back-biasing magnet and a 100% matte-tin-plated lead frame.

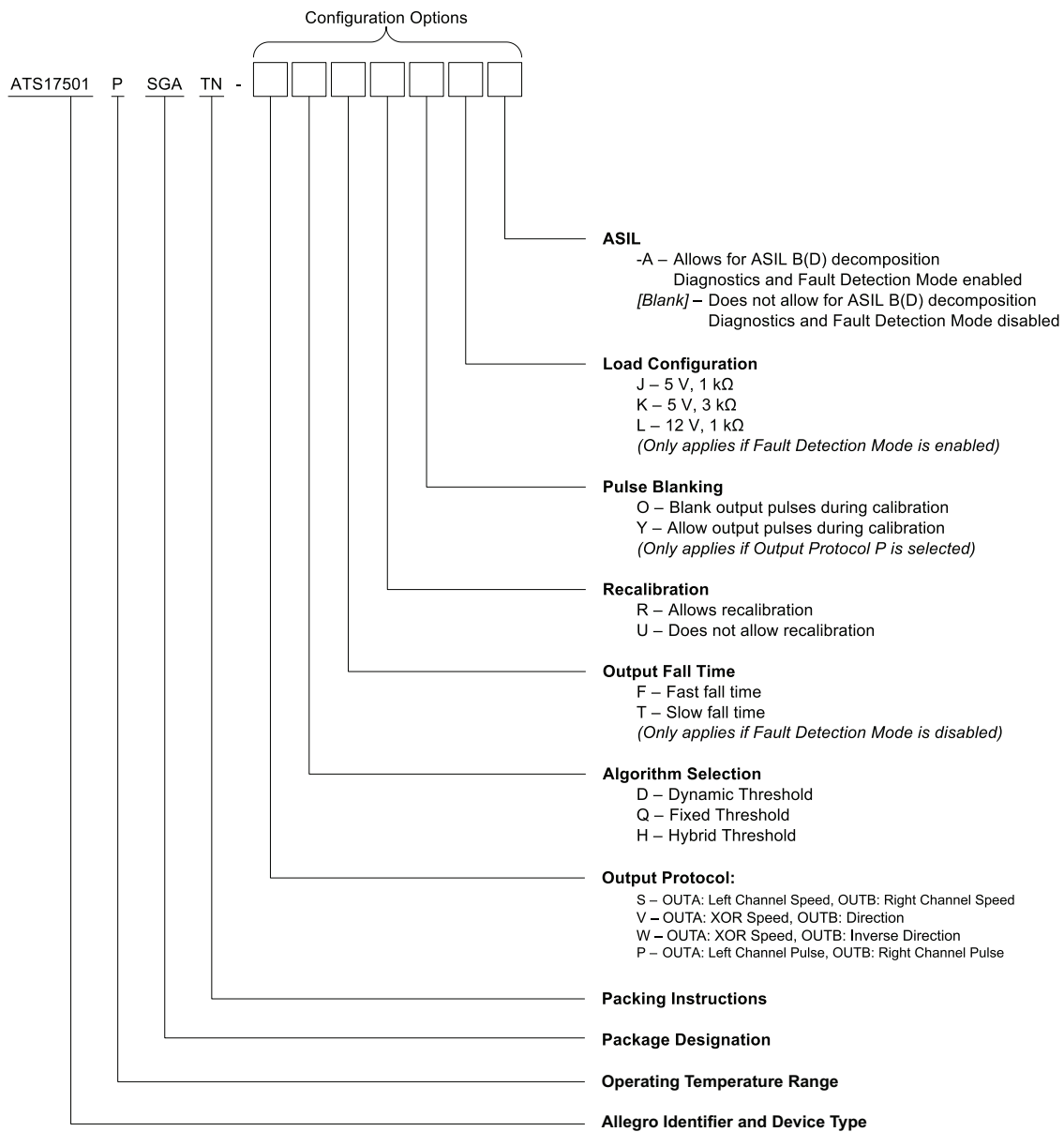
### Functional Block Diagram



## SELECTION GUIDE [1]

Part Number	Packing
ATS17501PSGATN-SDFUYJ	800 pieces per 13-inch reel
ATS17501PSGATN-VDFUYJ	
ATS17501PSGATN-WDFUYJ	
ATS17501PSGATN-SDFUYK-A	

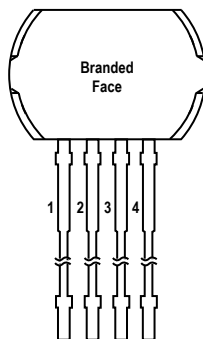
[1] Not all selectable combinations are available, contact Allegro for additional selections and packing options.



## ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	$V_{CC}$	Refer to Power Derating section	28	V
Reverse Supply Voltage	$V_{RCC}$		-18	V
Output Voltage	$V_{OUT}$	Each output pin	28	V
Reverse Output Voltage	$V_{ROUT}$	Each output pin; $R_{PULLUP} \geq 1\text{ k}\Omega$	-0.5	V
Output Sink Current	$I_{OUT}$	Short-term output current for OUTA and OUTB independently, not intended for continuous operation	50	mA
Operating Ambient Temperature Range	$T_A$		-40 to 160	°C
Junction Temperature	$T_J$		175	°C
Storage Temperature Range	$T_{stg}$		-65 to 170	°C

## PINOUT DIAGRAM

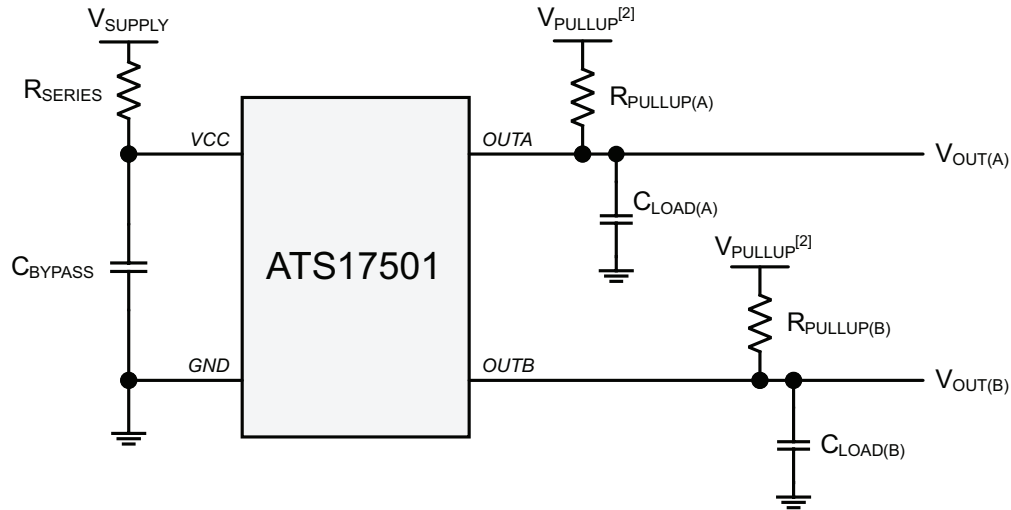


SG Package, 4-Pin SIP

## PINOUT TABLE

Name	Pin	Function
VCC	1	Supply Voltage
OUTA	2	Configurable Output A
OUTB	3	Configurable Output B
GND	4	Ground

## TYPICAL APPLICATION CIRCUIT



## COMPONENTS [3]

Characteristic	Symbol	Notes	Value (Typ.)	Unit
Series Resistance	$R_{SERIES}$	Recommended for typical EMC requirements	100	$\Omega$
OUTA Pullup Resistance	$R_{PULLUP(A)}$	Required for functional operation; recommended value dependent on programming options	1	k $\Omega$
OUTB Pullup Resistance	$R_{PULLUP(B)}$	Required for functional operation; recommended value dependent on programming options	1	k $\Omega$
Bypass Capacitance	$C_{BYPASS}$	Recommended for typical EMC requirements	100	nF
OUTA Load Capacitance	$C_{LOAD(A)}$	Recommended for typical EMC requirements; required for certain programming options	2.2	nF
OUTB Load Capacitance	$C_{LOAD(B)}$	Recommended for typical EMC requirements; required for certain programming options	2.2	nF

<sup>[2]</sup>  $V_{PULLUP}$  may be connected to  $V_{CC}$  if  $V_{CC}$  meets  $V_{PULLUP}$  requirements. See Operating Characteristics section.

<sup>[3]</sup> Components listed are typical recommended values and are not suited for all applications and/or programmable options. See Operating Characteristics and Selection Guide for more information.

### OPERATING CHARACTERISTICS: Valid throughout operating ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [4]	Max.	Unit	
<b>ELECTRICAL SUPPLY CHARACTERISTICS</b>							
Supply Voltage [5]	$V_{CC}$	Voltage across VCC and GND	4	–	24	V	
Undervoltage Lockout	$V_{CC(UV)}$		–	–	3.99	V	
Supply Current	$I_{CC}$		–	10	15	mA	
Reverse Supply Current	$I_{RCC}$	$V_{CC} = -18\text{ V}$	-10	–	–	mA	
<b>ELECTRICAL PROTECTION CHARACTERISTICS</b>							
Supply Clamp Voltage	$V_{CSUPPLY}$	$T_A = 25^\circ\text{C}; I_{CC} = 18\text{ mA}$	28	–	–	V	
Reverse Supply Clamp Voltage	$V_{RCSUPPLY}$	$T_A = 25^\circ\text{C}; I_{CC} = -3\text{ mA}$	–	–	-18	V	
Output Clamp Voltage	$V_{OUT}$	$T_A = 25^\circ\text{C}; I_{OUT} = 3\text{ mA}$	28	–	–	V	
Output Current Internal Limiter	$I_{OUT(LIM)}$	Current limited by design for short circuit event on OUTA and OUTB independently; low impedance output state	30	55	85	mA	
<b>POWER-ON CHARACTERISTICS</b>							
Power-On State	POS	For OUTA and OUTB	$V_{OUT(HIGH)}$			V	
Power-On Time	$t_{PO}$	Time from $V_{CC} > V_{CC(min)}$ to when sensor IC output is valid	–	–	1	ms	
<b>CALIBRATION CHARACTERISTICS</b>							
First Output Edge	–	Amount of target rotation with constant direction following power-on until first electrical output transition; Dynamic Threshold option; see Figure 1	–	1	–	$T_{CYCLE}$	
Initial Calibration	–	Amount of target rotation with constant direction following power-on until calibration is complete; Dynamic Threshold option; see Figure 1	–	2	–	$T_{CYCLE}$	
<b>OUTPUT CHARACTERISTICS [6]</b>							
Output Low Voltage	$V_{OUT(LOW)}$	Fault Detection Mode disabled; $I_{OUT} = 10\text{ mA}$	–	0.165	0.35	V	
		Fault Detection Mode enabled	5 V, 1 k $\Omega$ or 5 V, 3 k $\Omega$ option	0.5	–	1.25	V
			12 V, 1 k $\Omega$ option	1.2	–	3.6	V
Output High Voltage	$V_{OUT(HIGH)}$	Fault Detection Mode disabled	–	$V_{PULLUP}$	–	V	
		Fault Detection Mode enabled	5 V, 1 k $\Omega$ or 5 V, 3 k $\Omega$ option	3.75	–	4.5	V
			12 V, 1 k $\Omega$ option	8.4	–	10.8	V

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[4] Typical values are at  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{ V}$ . Performance may vary for individual units, within the specified maximum and minimum limits.

[5] Maximum voltage must be adjusted for power dissipation and junction temperature; see representative for Power Derating discussions.

[6] Output characteristics are valid for each output independently, unless otherwise specified.

## OPERATING CHARACTERISTICS (continued): Valid throughout operating ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [7]	Max.	Unit	
<b>OUTPUT CHARACTERISTICS (continued) [8]</b>							
Fault Voltage [9]	$V_{\text{FAULT}}$	Fault Detection Mode enabled; 5 V, 1 k $\Omega$ or 5 V, 3 k $\Omega$ option	High fault ( $V_{\text{FAULT(HIGH)}}$ )	4.5	–	–	V
			Mid fault ( $V_{\text{FAULT(MID)}}$ )	1.25	–	3.75	V
			Low fault ( $V_{\text{FAULT(LOW)}}$ )	–	–	0.5	V
		Fault Detection Mode enabled; 12 V, 1 k $\Omega$ option	High fault ( $V_{\text{FAULT(HIGH)}}$ )	10.8	–	–	V
			Mid fault ( $V_{\text{FAULT(MID)}}$ )	3.6	–	8.4	V
			Low fault ( $V_{\text{FAULT(LOW)}}$ )	–	–	1.2	V
Allowable Pullup Voltage	$V_{\text{PULLUP}}$	Fault Detection Mode disabled	4	–	24	V	
		Fault Detection Mode enabled	5 V, 1 k $\Omega$ or 5 V, 3 k $\Omega$ option	4.75	–	5.25	V
			12 V, 1 k $\Omega$ option	11.4	–	12.6	V
Allowable Pullup Resistor [10]	$R_{\text{PULLUP}}$	Fault Detection Mode disabled	–	1	–	k $\Omega$	
		Fault Detection Mode enabled	5 V, 1 k $\Omega$ option	0.8	–	1.46	k $\Omega$
			5 V, 3 k $\Omega$ option	1.46	–	3.4	k $\Omega$
			12 V, 1 k $\Omega$ option	0.9	–	1.1	k $\Omega$
Allowable Load Capacitor [11]	$C_{\text{LOAD}}$	Fault Detection Mode enabled	1	–	–	nF	
Output Leakage Current	$I_{\text{OUT(OFF)}}$	Fault Detection Mode disabled; $V_{\text{OUT}} = V_{\text{OUT(HIGH)}}$	–	–	10	$\mu\text{A}$	
Duty Cycle	D	Speed output protocol; Using Reference Target 60-0; Dynamic Threshold option; sinusoidal input signal; $f_{\text{OP}} < 1 \text{ kHz}$	45	50	55	%	
Output Rise Time	$t_r$	10% $\rightarrow$ 90%; $V_{\text{PULLUP}} = 5 \text{ V}$ ; $R_{\text{PULLUP}} = 1 \text{ k}\Omega$ ; $C_{\text{LOAD}} = 2.2 \text{ nF}$	–	5	–	$\mu\text{s}$	
Output Fall Time	$t_f$	90% $\rightarrow$ 10%; $V_{\text{PULLUP}} = 5 \text{ V}$ ; $R_{\text{PULLUP}} = 1 \text{ k}\Omega$ ; $C_{\text{LOAD}} = 2.2 \text{ nF}$	Fault Detection Mode disabled; Fast fall time option	–	0.5	–	$\mu\text{s}$
			Fault Detection Mode disabled; Slow fall time option	–	3.5	–	$\mu\text{s}$
			Fault Detection Mode enabled	–	6	–	$\mu\text{s}$
Forward Pulse Width [12]	$t_{\text{w(FWD)}}$		38	45	52	$\mu\text{s}$	
Reverse Pulse Width [12]	$t_{\text{w(REV)}}$		76	90	104	$\mu\text{s}$	
Propagation Delay	$t_d$	Delay from the magnetic signal crossing a switch point threshold to the start of the output transition	–	8	–	$\mu\text{s}$	
Jitter [13]	–	$\sigma \times 6$ ; sinusoidal input signal; $f_{\text{OP}} = 1 \text{ kHz}$	$B_{\text{DIFF(pk-pk)}} = 100 \text{ G}$	–	–	0.13	target degrees
			$B_{\text{DIFF(pk-pk)}} = 150 \text{ G}$	–	–	0.086	target degrees
			$B_{\text{DIFF(pk-pk)}} = 200 \text{ G}$	–	–	0.064	target degrees

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[7] Typical values are for  $V_{\text{CC}} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

[8] Output characteristics are valid for each output independently, unless otherwise specified.

[9] Valid with Fault Detection Mode enabled and correct programming of the Fault Detection Load Circuit option; see Selection Guide.

[10] See Application Circuit section.

[11] Minimum capacitor required when Fault Detection Mode is enabled to ensure correct output levels over operating conditions. Increased load capacitance will directly impact maximum operating frequency due to the increased rise and fall times; see Application Circuit section.

[12] Time from start of output transition from  $V_{\text{OUT(HIGH)}}$  to  $V_{\text{OUT(LOW)}}$  to start of output transition from  $V_{\text{OUT(LOW)}}$  to  $V_{\text{OUT(HIGH)}}$ . Measured pulse width will vary with load circuit configurations and measurement thresholds. Valid with Pulse or Pulse Inverted output protocol; see Programming Options section.

[13] Guaranteed by design and characterization only. Characterization performed by measuring greater than 1,000 falling output edges of the same target feature at constant temperature using Reference Target 60-0, see Reference Target Characteristics section. Value representative of a 6- $\sigma$  distribution, such that 99.76% of the measured values are within the specified target degree.

### OPERATING CHARACTERISTICS (continued): Valid over operating ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [14]	Max.	Unit		
<b>SWITCH POINT CHARACTERISTICS</b>								
Operate Point	$B_{OP}$	% of $B_{DIFF(PKPK)}$ ; $V_{OUT} = V_{OUT(LOW)} \rightarrow V_{OUT} = V_{OUT(HIGH)}$ ; Dynamic Threshold option	–	70	–	%		
Release Point	$B_{RP}$	% of $B_{DIFF(PKPK)}$ ; $V_{OUT} = V_{OUT(HIGH)} \rightarrow V_{OUT} = V_{OUT(LOW)}$ ; Dynamic Threshold option	–	30	–	%		
Hysteresis	$B_{HYS}$	$\Delta B_{DIFF}$ after switch point to allow next output transition		% of $B_{DIFF(PKPK)}$ ; Dynamic Threshold option	–	40	–	%
				Fixed Threshold option	–	10	–	G
<b>INPUT CHARACTERISTICS</b>								
Operating Frequency	$f_{OP}$	Sinusoidal input signal; forward and reverse target rotation; not valid for Pulse or Inverse Pulse output protocol	0	–	40	kHz		
Forward Pulse Operating Frequency	$f_{OP(FWD)}$	Pulse or Inverse Pulse output protocol	0	–	9	kHz		
Reverse Pulse Operating Frequency	$f_{OP(REV)}$	Pulse or Inverse Pulse output protocol	0	–	6	kHz		
Operating Magnetic Input [15]	$B_{DIFF(pk-pk)}$	See Figure 2		Dynamic Threshold option; $f_{OP} \leq 20$ kHz	30	–	–	G
				Dynamic Threshold option; $f_{OP} > 20$ kHz	40	–	–	G
				Fixed Threshold option	100	–	–	G
Operating Magnetic Input Peak [15]	$B_{DIFF}$	See Figure 2	–1150	–	1150	G		
Operating Magnetic Input Signal Variation [16]	$\Delta B_{DIFF(pk-pk)}$	Bounded amplitude ratio within $T_{WINDOW}$ ; no missed output transitions; possible incorrect direction information and/or reduction in switch point accuracy; see Figure 3 and Figure 4	0.6	–	2	–		
Operating Magnetic Input Signal Variation Window	$T_{WINDOW}$	Rolling window in which $\Delta B_{DIFF(pk-pk)}$ cannot exceed bounded ratio; see Figure 3 and Figure 4	8	–	–	$T_{CYCLE}$		
Operating Air Gap [17]	AG	Using Reference Target 60-0; $f_{OP} < 10$ kHz; Dynamic Threshold option		Fault Detection mode disabled	0.75	–	3	mm
				Fault Detection mode enabled	0.75	–	2.75	mm
<b>THERMAL CHARACTERISTICS</b>								
Package Thermal Resistance	$R_{\theta JA}$	Minimum-K PCB, single layer, single-sided, with copper limited to solder pads	–	126	–	°C/W		
		Low-K PCB, single layer, single-sided, with copper limited to solder pads and 3.57 in. <sup>2</sup> (23.03 cm <sup>2</sup> ) of copper area each side	–	84	–	°C/W		

[14] Typical values are for  $V_{CC} = 5$  V and  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

[15] Differential magnetic field is measured for Left Channel (F1-F2) and Right Channel (F2-F3) independently; see Package Diagram. Magnetic field is measured orthogonally to the branded package face.

[16] Operating magnetic input variation is valid for symmetrical peak variation about the signal offset.  $B_{DIFF(pk-pk)}$  must always be greater than  $B_{DIFF(pk-pk,min)}$ .

[17] Operating air gap is dependent on the available magnetic field. The available magnetic field is target geometry, material, and speed dependent. Operational air gap should be independently characterized for each target.

REFERENCE

Definition of Terms

$T_{CYCLE}$

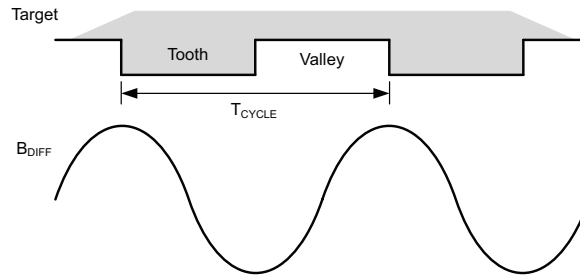


Figure 1: Definition of  $T_{CYCLE}$

$T_{CYCLE}$  = Target Cycle; the amount of rotation that moves one tooth and valley across the sensor.

$B_{DIFF}$  = The differential magnetic flux density sensed by the IC.

Differential Magnetic Input

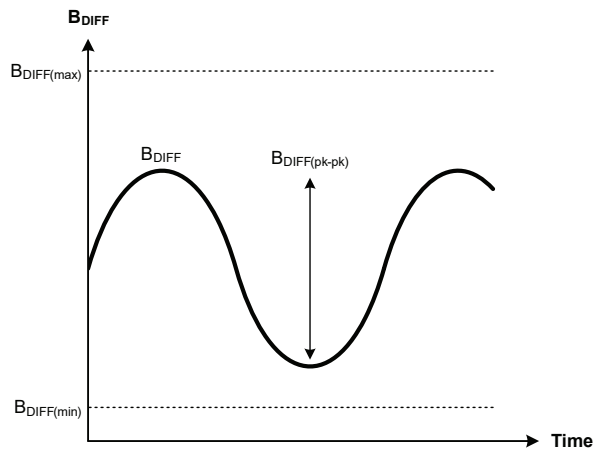


Figure 2: Differential Magnetic Input

$B_{DIFF(pk-pk)}$  = The peak-to-peak magnetic flux density sensed by the IC.



Operating Magnetic Signal Variation and Window

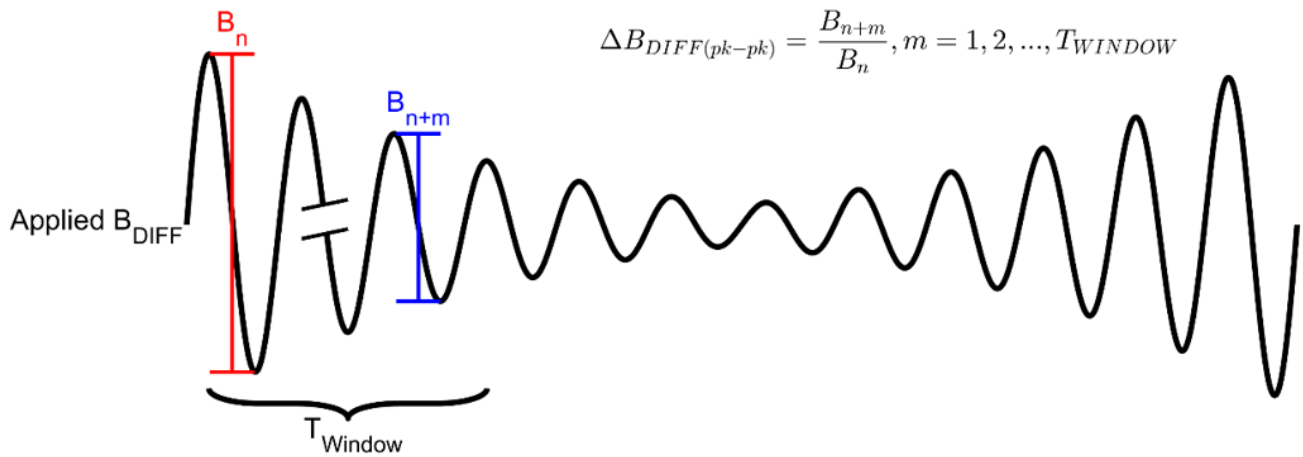


Figure 3: Repeated Period Variation

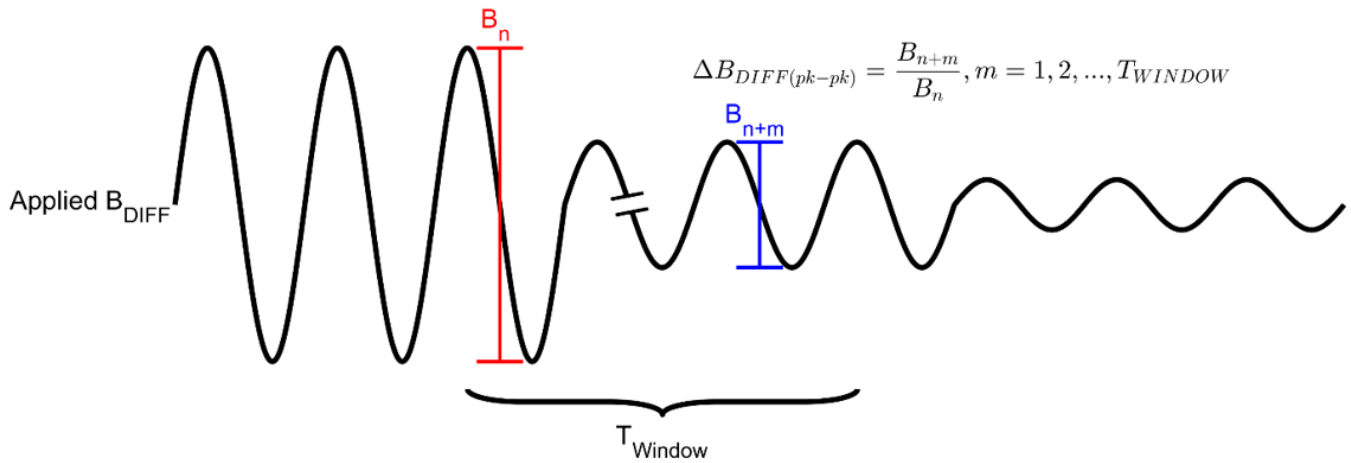


Figure 4: Single Period Variation

REFERENCE TARGET CHARACTERISTICS: Allegro Reference Target 60-0

Characteristics	Symbol	Test Conditions	Typ.	Units	Symbol Key
Outside Diameter	$D_o$	Outside diameter of target	120	mm	
Face Width	F	Breadth of tooth, with respect to branded face of the Sensor IC	6	mm	
Circular Tooth Length	t	Length of tooth, with respect to branded face of the Sensor IC	3	degrees	
Circular Valley Width	$t_v$	Length of valley, with respect to branded face of the Sensor IC	3	degrees	
Tooth Whole Depth	$h_t$		3	mm	
Material		Low Carbon Steel	-	-	

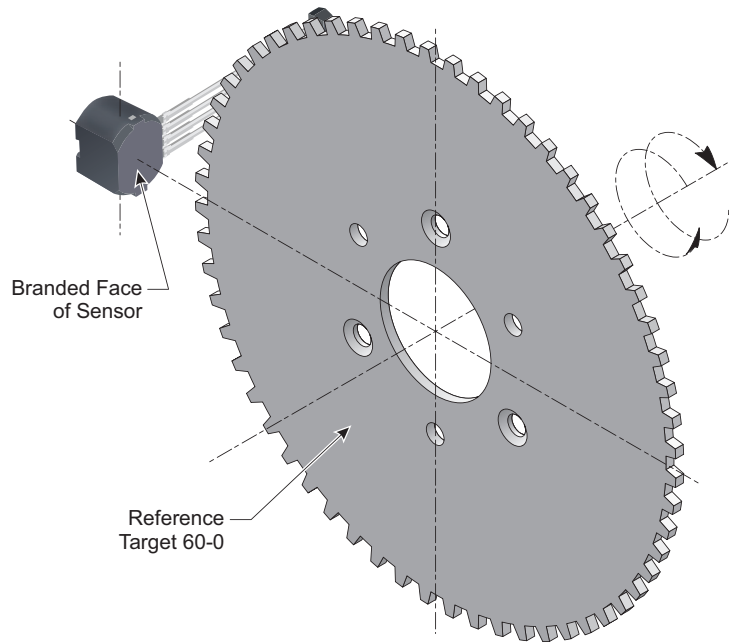
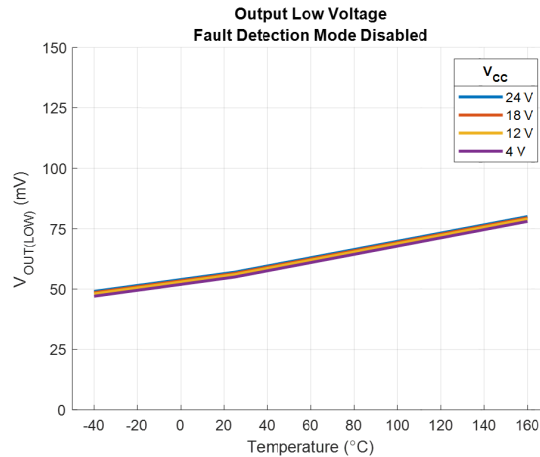
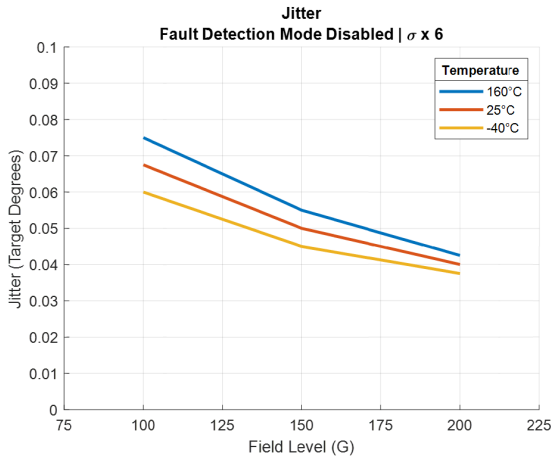
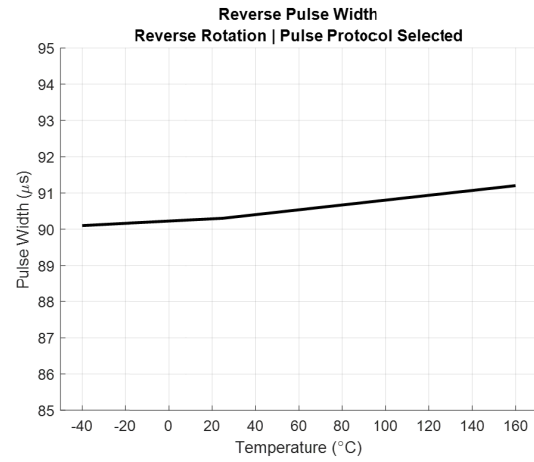
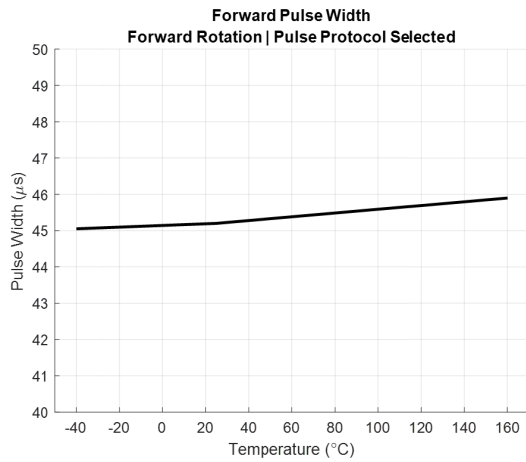
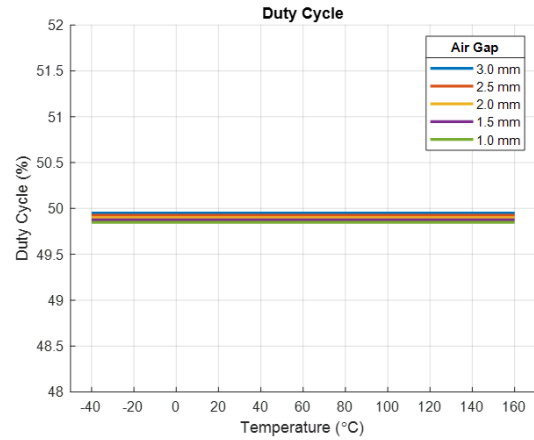
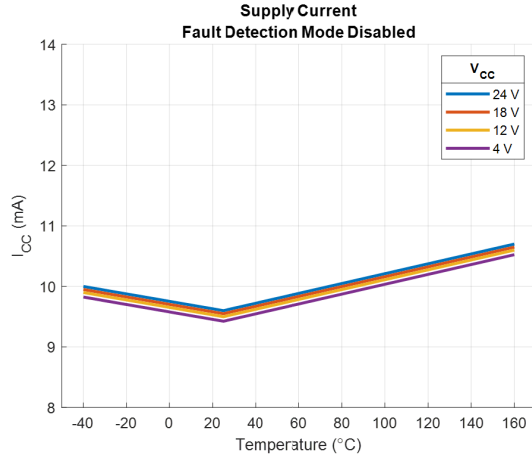
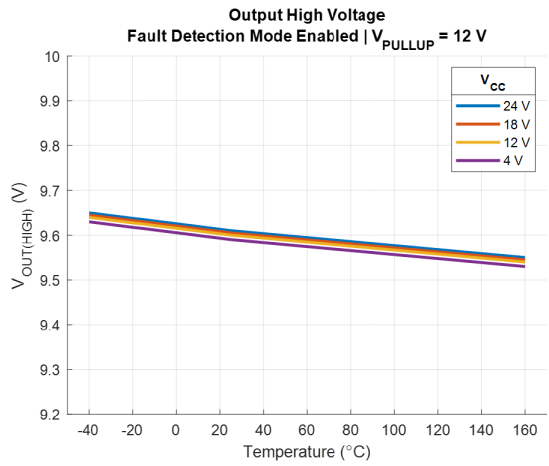
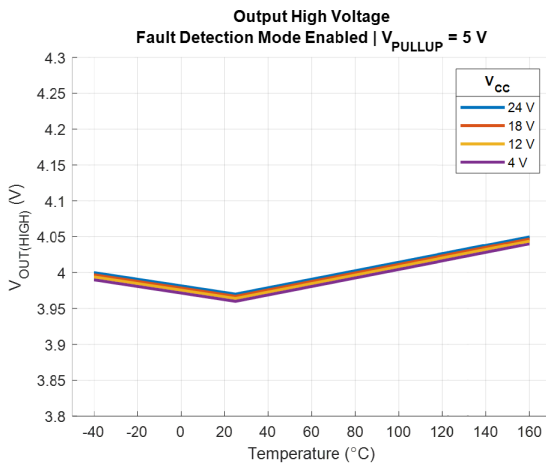
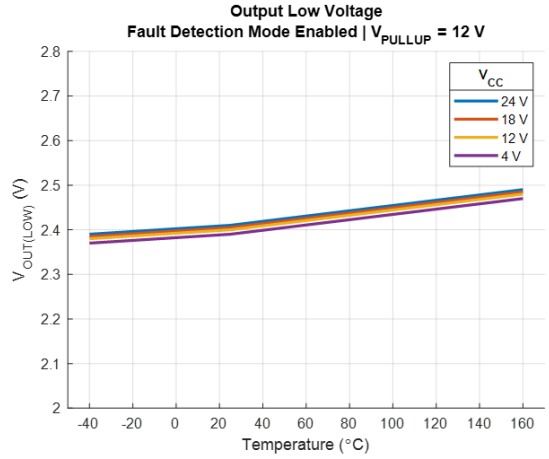
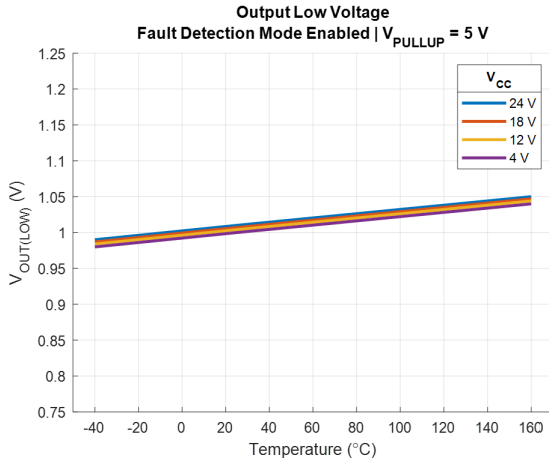


Figure 5: Reference Target 60-0

CHARACTERIZATION PLOTS [18]



[18] Characterization data representative of distribution averages. Characterization tested with Dynamic Threshold algorithm at  $f_{OP} = 1$  kHz,  $V_{CC} = 5$  V,  $V_{PULLUP} = 5$  V,  $R_{PULLUP} = 1$  k $\Omega$ , and  $C_{LOAD} = 2.2$  nF unless otherwise specified.



FUNCTIONAL DESCRIPTION

General

The ATS17501 sensor module contains a single-chip, dual differential Hall-effect sensor IC, a rare-earth pellet, and a flat ferrous pole piece (concentrator). As shown in Figure 6, the Hall-effect sensor IC supports three Hall elements that sense the magnetic profile of the ferrous gear target simultaneously but at different points (each channel spaced at 1.75 mm pitch), generating two differential internal signals processed for precise switching of the digital output signals. Direction of rotation can be determined based on the phase relationship of the two differential internal signals. The ATS17501 is intended for use with ferromagnetic targets.

The Hall-effect sensor IC is self-calibrating and possesses a temperature-compensated amplifier as well as a full-range analog-to-digital converter (ADC). This allows for accurate processing of a wide range of target magnetic profile amplitudes and offsets. The on-chip voltage regulator provides supply noise rejection throughout the operating voltage range. Changes in temperature do not greatly affect the ATS17501 due to the stable amplifier design and full-range ADC. The Hall elements and signal processing electronics are integrated on the same silicon substrate.

The ATS17501 is capable of providing digital information that is representative of the mechanical features of a rotating target gear. Figure 6 shows the automatic translation of the mechanical profile to the digital output signal. No additional optimization is needed, and minimum processing circuitry is required. This ease of use reduces design time and incremental assembly costs for most applications.

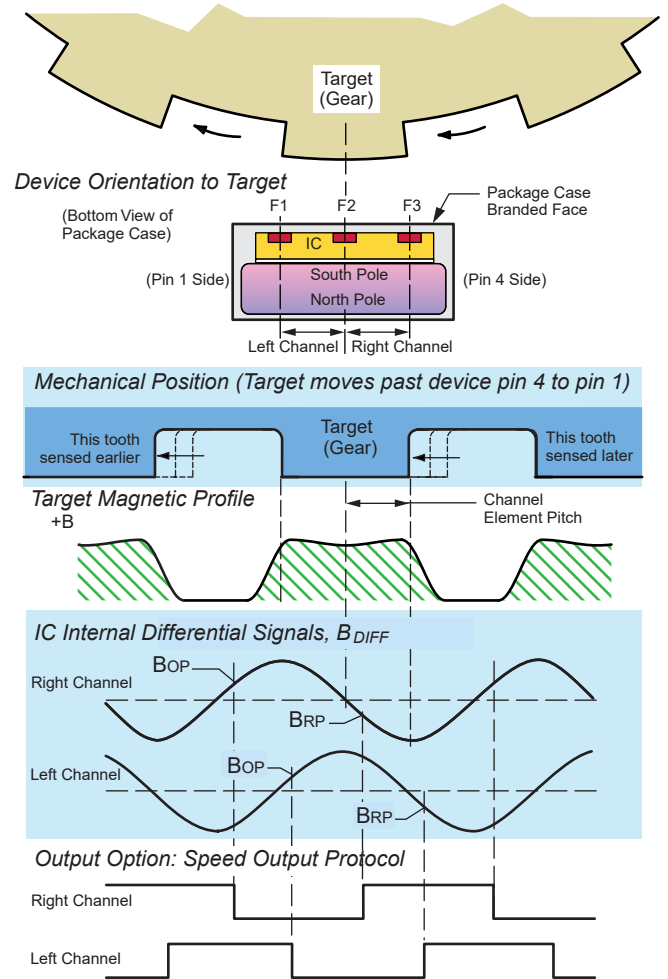


Figure 6: Magnetic Profile

**Threshold Algorithms**

The ATS17501 contains selectable algorithms for determining when to produce an output transition from the magnetic input signal. For all options, a threshold is set within the sensor IC that triggers the output transition when crossed by the digitized magnetic signals (switch point).

*Dynamic Threshold*

With the ATS17501 programmed for the Dynamic Threshold option, each switch point is calculated from information learned from the previous target feature. This algorithm allows for robust tracking to produce accurate output transitions for inconsistent magnetic input signals (offset drift, amplitude changes, etc.).

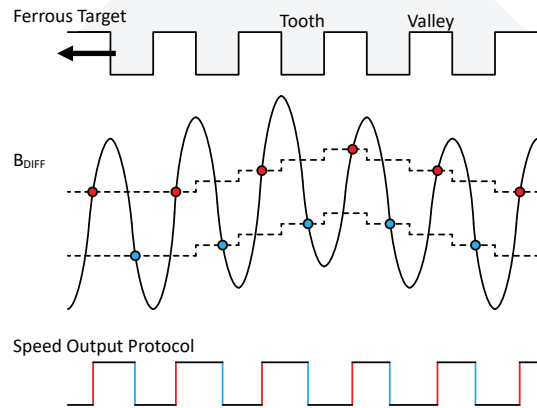
After power-on, the magnetic input signal is tracked to find the peaks of the signal. After each new peak is found, the switch points are updated based on a percentage of the previous two peaks.

*Fixed Threshold*

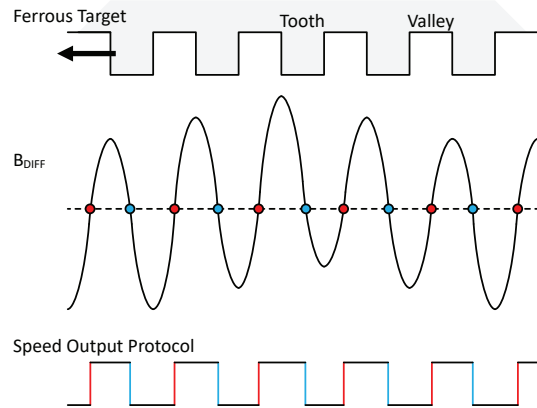
With the ATS17501 programmed for the Fixed Threshold option, an absolute threshold stored in memory is used to set the switch point for both the operate point and release point. This algorithm allows for accurate output transitions immediately after power-on for consistent magnetic input signals without the need to “learn” the signal. The threshold stored in memory and loaded during power-on contains threshold levels over temperature to allow for offset drift adjustment of the magnetic input signal over temperature. The ATS17501 sensor IC contains a temperature sensor used continuously to adjust the switch point over temperature as needed by the application.

The fixed thresholds stored in memory can be pre-programmed for unique switch points over temperature for each application. Additionally, the ATS17501 can find and set the threshold for each installation over temperature during end-of-line calibration.

If during the application the magnetic input signal offset does not match the programmed threshold stored in memory (due to inaccurate programming, mechanical shift, etc.), the ATS17501 identifies the threshold as “out of range”, calculates the threshold for the current temperature, and updates the threshold to produce correct output transitions. After the update, algorithms use the current temperature to recharacterize the threshold over the operational temperature range. This prevents the update from overcompensating the threshold at a distant temperature relative to the update temperature. After the updated threshold is confirmed to be within the magnetic input signal’s switch point range over several target features, the updated threshold is stored into memory such that it can be used for subsequent power-on cycles.



**Figure 7: Dynamic Threshold Option Switch Point Algorithm ( $B_{OP} = 70\%$ ,  $B_{RP} = 30\%$ )**



**Figure 8: Fixed Threshold Option Switch Point Algorithm**

### *Hybrid Threshold*

With the ATS17501 programmed for the Hybrid Threshold option, the threshold is determined from the Fixed Threshold option at startup, then transitions to the Dynamic Threshold option after tracking signals have correctly acquired the magnetic input signals. This algorithm allows for both accurate output transitions immediately following power-on for consistent magnetic input signals as well as robust tracking to produce accurate output transitions of inconsistent magnetic input signals (offset drift, amplitude changes, etc.).

Once the tracking signals have identified consistent peak values

from the magnetic input signal, the algorithm will transition from using the fixed threshold switch point to using the dynamic threshold switch points. This transition occurs only when the magnetic input signal is near a maximum or minimum value, such that “double-switching” on the transition can be avoided.

While the majority of the power-on will use the Dynamic Threshold option for robust signal tracking, the ATS17501 will continue to monitor the fixed threshold for comparison to the fixed threshold stored in memory. Should the fixed threshold require an update, the ATS17501 will update and write the new threshold to memory for use in subsequent power-on cycles.

**Output**

The ATS17501 contains a number of selectable options to change the output protocol or adjust the output behavior. These options allow for the ATS17501 to be programmed to application-level needs.

*Output Protocol*

The ATS17501 contains several programmable output protocols; see Figure 9. These protocols can be programmed for either output pin (OUTA or OUTB) independently. For example, Left Channel Speed can be programmed as the output protocol for OUTA, OUTB, or both output pins.

The ATS17501 contains two independent signal paths. Most output protocols reference a specific magnetic input signal channel ( $B_{DIFF(LEFT)}$  or  $B_{DIFF(RIGHT)}$ ), which is used to determine the out-

put transitions. These channels are determined by the Hall elements used to produce the differential signal, where the left channel differential signal is determined by the left and center element (F1-F2), and the right channel is referenced from the center and right element (F2-F3); see Package Diagram. XOR Speed and Direction output protocols are channel-independent, as both channels are used to determine the output transitions.

For Speed, XOR Speed and Direction output protocols, the polarity of the signal can be inverted by selecting the “Inverse” option of the corresponding protocol. Selecting one of these options will invert the polarity of the output ( $V_{OUT(HIGH)}$  and  $V_{OUT(LOW)}$ ) relative to the  $B_{DIFF}$  signal(s). For the Pulse output protocols, selecting the “Inverse” option will invert the pulse width for forward and reverse rotation ( $t_{w(FWD)}$  and  $t_{w(REV)}$ ).

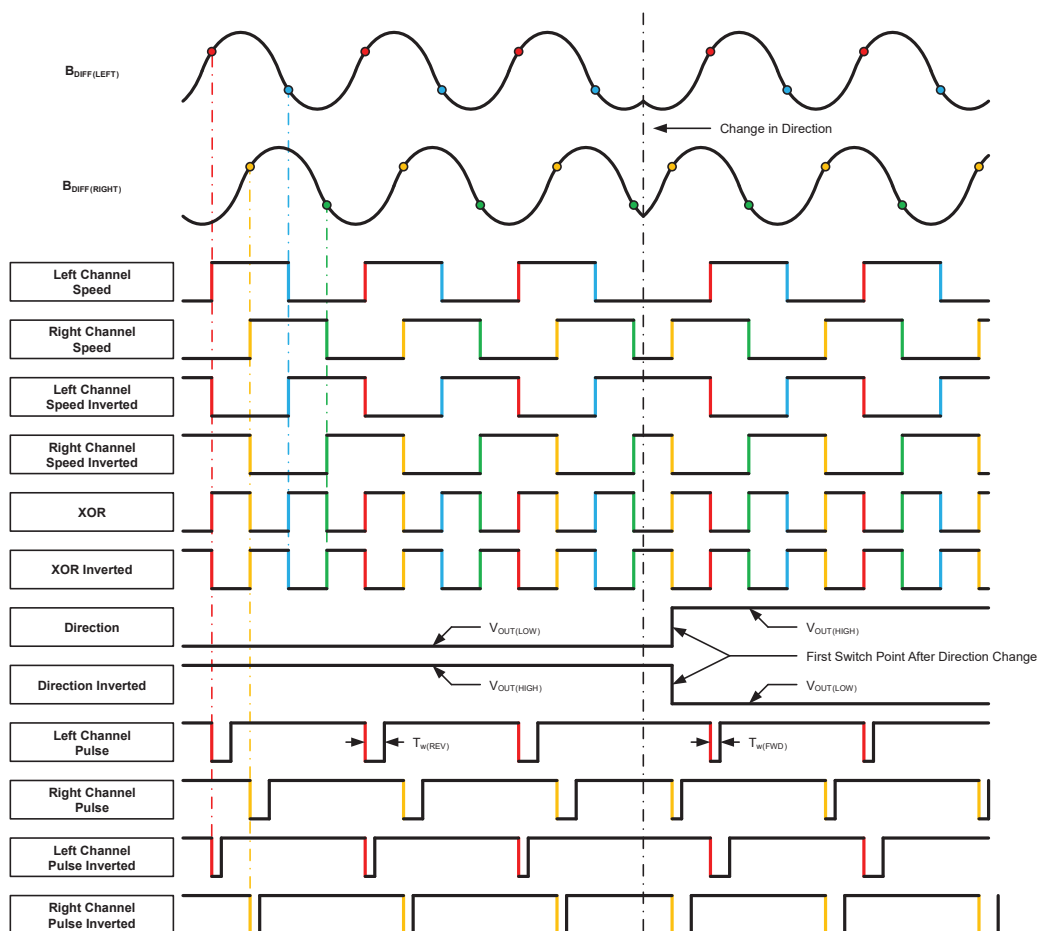


Figure 9: Output Protocol Options

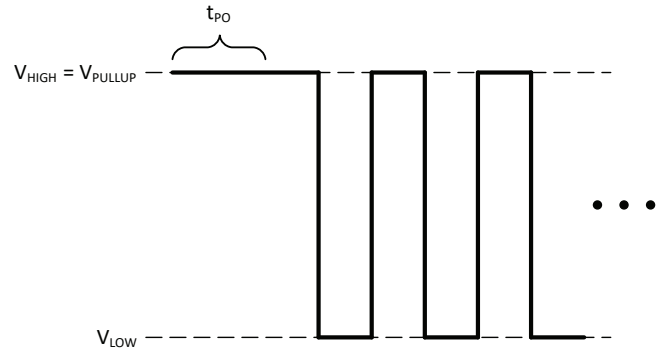


**Fault Detection Mode**

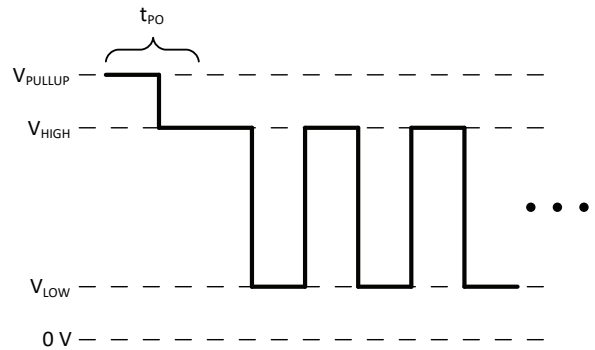
The ATS17501 allows for the output to transition between one of two sets of values. With Fault Detection mode disabled, the output will transition between approximately 0% and 100% of  $V_{PULLUP}$ . With Fault Detection mode disabled, the output transitions between approximately 20% and 80% of  $V_{PULLUP}$ .

At the beginning of power-on, the ATS17501 outputs initialize to the  $V_{PULLUP}$  level. With Fault Detection mode enabled, the output levels transition from  $V_{PULLUP}$  to  $V_{HIGH}$  before the end of power-on. After power-on, the output transitions as determined by the programmed algorithm and output protocol between  $V_{OUT(HIGH)}$  and  $V_{OUT(LOW)}$ .

Enabling Fault Detection mode allows for additional communication for cases of open wire or short circuit, as well as allowing for the ATS17501 to communicate a fault detected from the internal diagnostics. For a typical application load circuit, these cases can be detected by observing either OUTA or OUTB transition to approximately 0 V or  $V_{PULLUP}$  after  $t_{PO}$ .



**Figure 10: Fault Detection Mode Disabled Output**



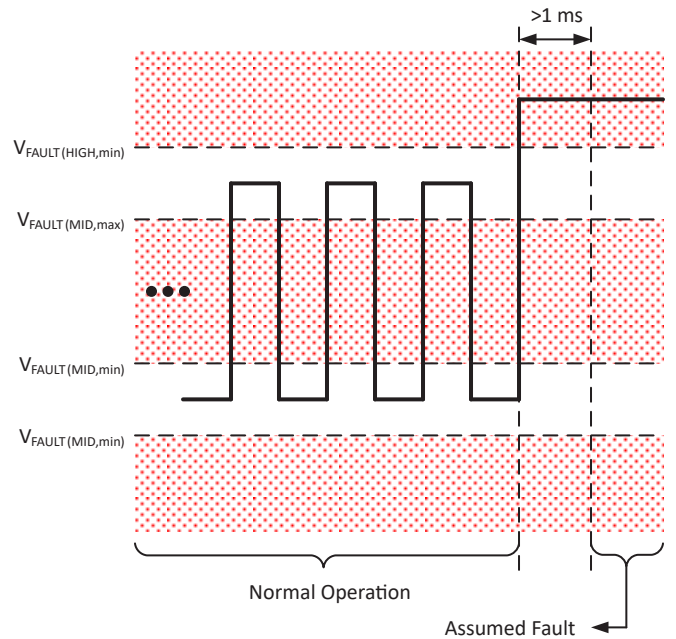
**Figure 11: Fault Detection Mode Enabled Output**

**Fault Voltage**

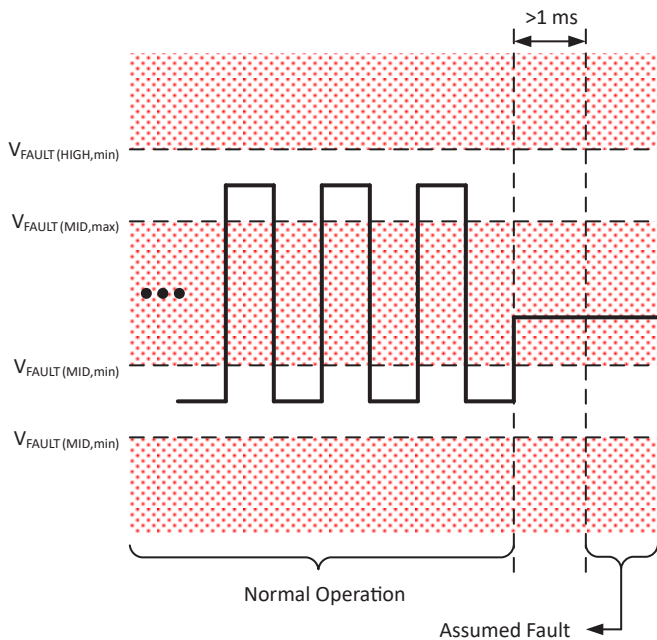
The ATS17501 communicates a fault condition by configuring either output to hold within one of three  $V_{FAULT}$  ranges (high, mid, and low) for greater than 1 millisecond. Normal operation allows for output transitions to occur over the  $V_{FAULT(MID)}$  range; as such, it is necessary to ignore fast transients for less than 1 millisecond through this range.

For internal diagnostics that trigger fault conditions (force the output to go to  $V_{FAULT}$ ), both outputs will go to the  $V_{FAULT(HIGH)}$  range. As there may exist internal or external faults that cause either or both output pins to hold a  $V_{FAULT(MID)}$  or  $V_{FAULT(LOW)}$  level, these fault ranges should also be monitored. Examples of these fault conditions could be a short circuit of the output to ground, forcing the output to  $V_{FAULT(LOW)}$ , or a fault in the IC output controller that forces the output to  $V_{FAULT(MID)}$ .

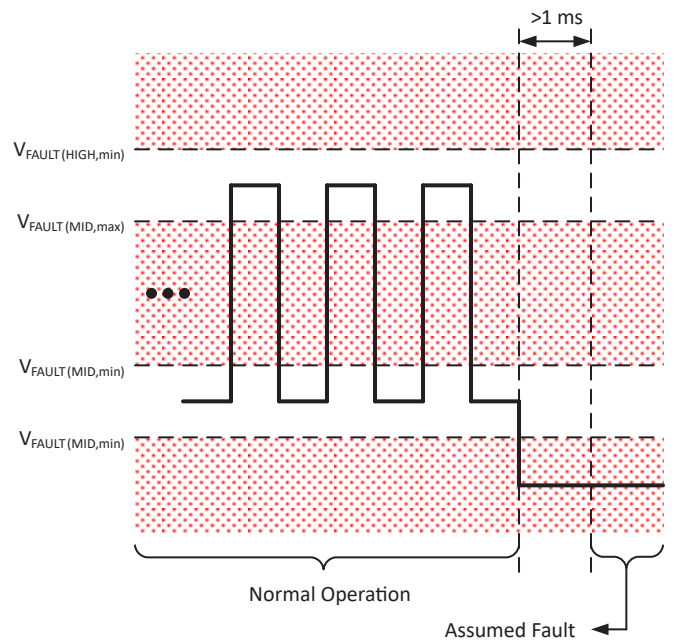
See Figure 12, Figure 13, and Figure 14 for examples of the output communicating a fault condition.



**Figure 12: Assumed Fault Example: High Fault**



**Figure 13: Assumed Fault Example: Mid Fault**



**Figure 14: Assumed Fault Example: Low Fault**

## DEVICE FEATURES

### *Undervoltage Lockout*

When supply voltage falls below the Undervoltage Lockout voltage ( $V_{CC(UV)}$ ), the ATS17501 enters Reset, where the output state returns to the Power-On State (POS) until sufficient  $V_{CC}$  is supplied. This feature prevents false signals, caused by undervoltage conditions, from propagating to the output of the sensor IC.

### *Power Supply Protection*

The ATS17501 contains an on-chip regulator and can operate over a wide  $V_{CC}$  range. For applications that need to operate from an unregulated power supply, transient protection must be added externally. For applications using a regulated line, EMI/RFI protection is recommended. Contact Allegro for more information about circuitry to address EMC requirement compliance. Refer to the Typical Application Circuit section.

### *Startup Hysteresis*

With a Power-On and a target held at zero-speed ( $f_{OP} \approx 0$  Hz), noise and/or vibration can produce magnetic input signals. Startup hysteresis prevents peak tracking and switch point setting at startup immediately following power-on. This occurs until the sensed differential magnetic signal has moved sufficiently to satisfy the hysteresis band for signal tracking. This feature helps to ensure optimal self-calibration of the magnetic signals by rejecting electrical noise and low-amplitude target vibrations during startup and ensures that calibration occurs on actual target features.

### *Small Signal Lockout*

When  $B_{DIFF(pk-pk)}$  falls below specification, the internal logic of the sensor IC will indicate a reduced signal, as measured in an excessive air gap or a vibration condition. Small Signal Lockout will hold the output state at the level when  $B_{DIFF(pk-pk)}$  was last in-specification. Once  $B_{DIFF(pk-pk)}$  returns to an in-specification value, the output state is released to transition as expected during normal operation. When direction information is not explicitly defined by the selected output protocol, Small Signal Lockout is controlled independently for each channel. For example, Left Channel Speed + Right Channel Speed output protocol will allow for one channel to continue switching while the other is in lockout. When direction information is explicitly communicated, for example XOR + Direction output protocol, Small Signal Lockout will occur when either channel's  $B_{DIFF(pk-pk)}$  falls below specification.

### *Vibration Robust Signal Tracking*

During vibration events, the magnetic input signals can produce oscillations with a sufficient amplitude for the peak tracking algorithms to bound in and produce a non-ideal peak-to-peak. When the ATS17501 detects a direction change, inward bounding of the peak tracking signals is prevented. This prevents cases of erroneous output transitions from switch points being incorrectly set from vibration signals. Additionally, this allows for immediate acquisition of the magnetic input signals once real target rotation resumes following a vibration event.

### *Signature Tooth Robust Signal Tracking*

Signature teeth (characterized by an extra target tooth and/or valley) can produce significant variations of the magnetic input signals. The bounded updating of the tracking signals prevent overcompensation for these signature variations to provide robust and accurate switch points for the signature region, as well as the features about the signature region.

### *Temperature Drift Robust Signal Tracking*

As temperature changes can impact both the amplitude and offset of the magnetic signal, a full-range ADC, advanced algorithms, temperature compensation, watchdog timers, and an internal temperature sensor ensure robust signal tracking over temperature.

To compensate for amplitude changes over temperature, temperature compensated gain is first applied to normalize the amplitude over temperature. The full-range ADC and peak tracking algorithms track and acquire the signal to accurately set the switch points.

To compensate for offset changes over temperature, two algorithms are implemented to ensure the signal tracking accurately follows and updates the switch points to follow the offset. With nominal target rotation, peak-tracking algorithms automatically follow and update the switch points over offset drift. With no target rotation (stopped condition), a watchdog timer is implemented which adjusts the algorithms to track together, allowing for preservation of the correct signal peak-to-peak and switch points once rotation resumes.

With the Fixed Threshold algorithm option selected, algorithms are implemented for continuous monitoring and updating of the fixed threshold over temperature to follow the offset drift of the system. This compensation is implemented for each channel independently to provide robust tracking of both signal channels over temperature.

### *Diagnostics and Fault Reporting*

The ATS17501 contains diagnostics monitors of analog and digital circuits of the IC. These continuously monitor and report if any defect, calculation error, or invalid input stimulus is found. If a diagnostic monitor fires, the outputs of the ATS17501 will transition to a  $V_{\text{FAULT}}$  level. For all faults, the outputs will remain at the  $V_{\text{FAULT}}$  level for enough time to allow the system controller to monitor that a fault has occurred. For some diagnostics, it is possible to clear the fault with a reset of the internal controller of the sensor IC. If any of those diagnostic monitors triggers the fault event, the ATS17501 will automatically perform a reset of the internal controller after the output is held  $V_{\text{FAULT}}$  for enough time to allow the system controller to monitor the fault event.

For diagnostics and fault reporting to perform correctly, proper programming and adherence to the specifications and assumptions stated in this datasheet, the ATS17501 Safety Manual, and any other addendum, corrigendum, and application note that applies to the ATS17501. For more information on diagnostics and fault reporting, see the ATS17501 Safety Manual.

### *Recalibration*

Under large amplitude vibration conditions at startup, the peak-

to-peak and phase relationship of the magnetic input signals can meet the conditions to calibrate. Once normal rotation resumes, the actual signal amplitudes can be much larger than the peak signals acquired during calibration. Rather than wait several  $T_{\text{CYCLE}}$  events for the peak signal to be tracked to actual levels, the ATS17501 will detect the difference and recalibrate on the new signal. Recalibration allows for fast and robust correction from cases of calibration on vibration events.

### *Pulse Collision Prevention*

In cases of “high-speed” vibration, output transitions can occur at very high frequencies, to prevent pulse collision (truncation of the pulse width), the ATS17501 will prevent output transitions until the current output pulse transition is complete to ensure the system controller can accurately interpret the output signal. This feature is only implemented when a pulse protocol option is selected.

### *High Configurability*

The ATS17501 contains programmable parameters, as shown in the Selection Guide, that can be configured to provide application-level optimization.

POWER DERATING

The device must be operated below the maximum junction temperature of the device ( $T_{J(max)}$ ). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating  $T_J$ . (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance ( $R_{\theta JA}$ ) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ( $R_{\theta JC}$ ) is a relatively small component of  $R_{\theta JA}$ . Ambient air temperature ( $T_A$ ) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation or  $P_D$ ), can be estimated. The following formulas represent the fundamental relationships used to estimate  $T_J$ , at  $P_D$ .

$$P_D = V_{IN} \times I_{IN} \tag{1}$$

$$\Delta T = P_D \times R_{\theta JA} \tag{2}$$

$$T_J = T_A + \Delta T \tag{3}$$

For example, given common conditions such as:  $T_A = 25^\circ C$ ,  $V_{CC} = 12 V$ ,  $I_{CC(avg)} = 8.5 mA$ , and  $R_{\theta JA} = 126^\circ C/W$ , then:

$$P_D = V_{CC} \times I_{CC(avg)} = 12 V \times 8.5 mA = 102 mW$$

$$\Delta T = P_D \times R_{\theta JA} = 102 mW \times 126^\circ C/W = 12.9^\circ C$$

$$T_J = T_A + \Delta T = 25^\circ C + 12.9^\circ C = 37.9^\circ C$$

A worst-case estimate,  $P_{D(max)}$ , represents the maximum allowable power level ( $V_{CC(max)}$ ,  $I_{CC(max)}$ ), without exceeding  $T_{J(max)}$ , at a selected  $R_{\theta JA}$  and  $T_A$ .

For example, calculating reliability of  $V_{CC}$  given observed worst-case ratings, specifically:

$$T_A = 160^\circ C, R_{\theta JA} = 126^\circ C/W, T_{J(max)} = 175^\circ C, V_{CC(max)} = 24 V, \text{ and } I_{CC(max)} = 15 mA.$$

Calculation of the maximum allowable power,  $P_{D(max)}$ , can be done by first inverting equation 3 and calculating the maximum allowable increase to  $T_J$ :

$$\Delta T_{max} = T_{J(max)} - T_A = 175^\circ C - 160^\circ C = 15^\circ C$$

Then, maximum allowable power can be calculated by:

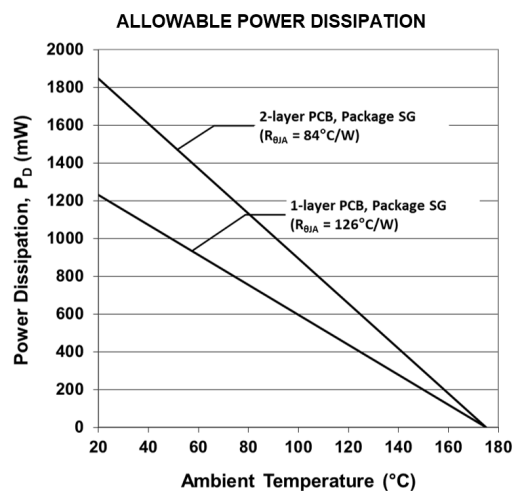
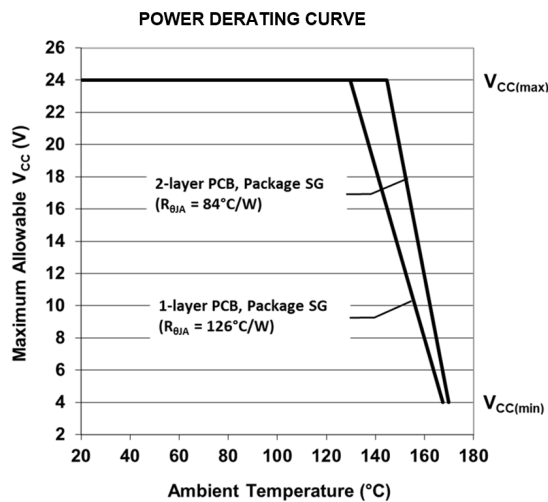
$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15^\circ C \div 126^\circ C/W = 119 mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 119 mW \div 15 mA = 7.9 V$$

The results indicate that, at  $T_A$ , the application and ATS17501 can dissipate adequate amounts of heat at voltages less than or equal to  $V_{CC(est)}$ .

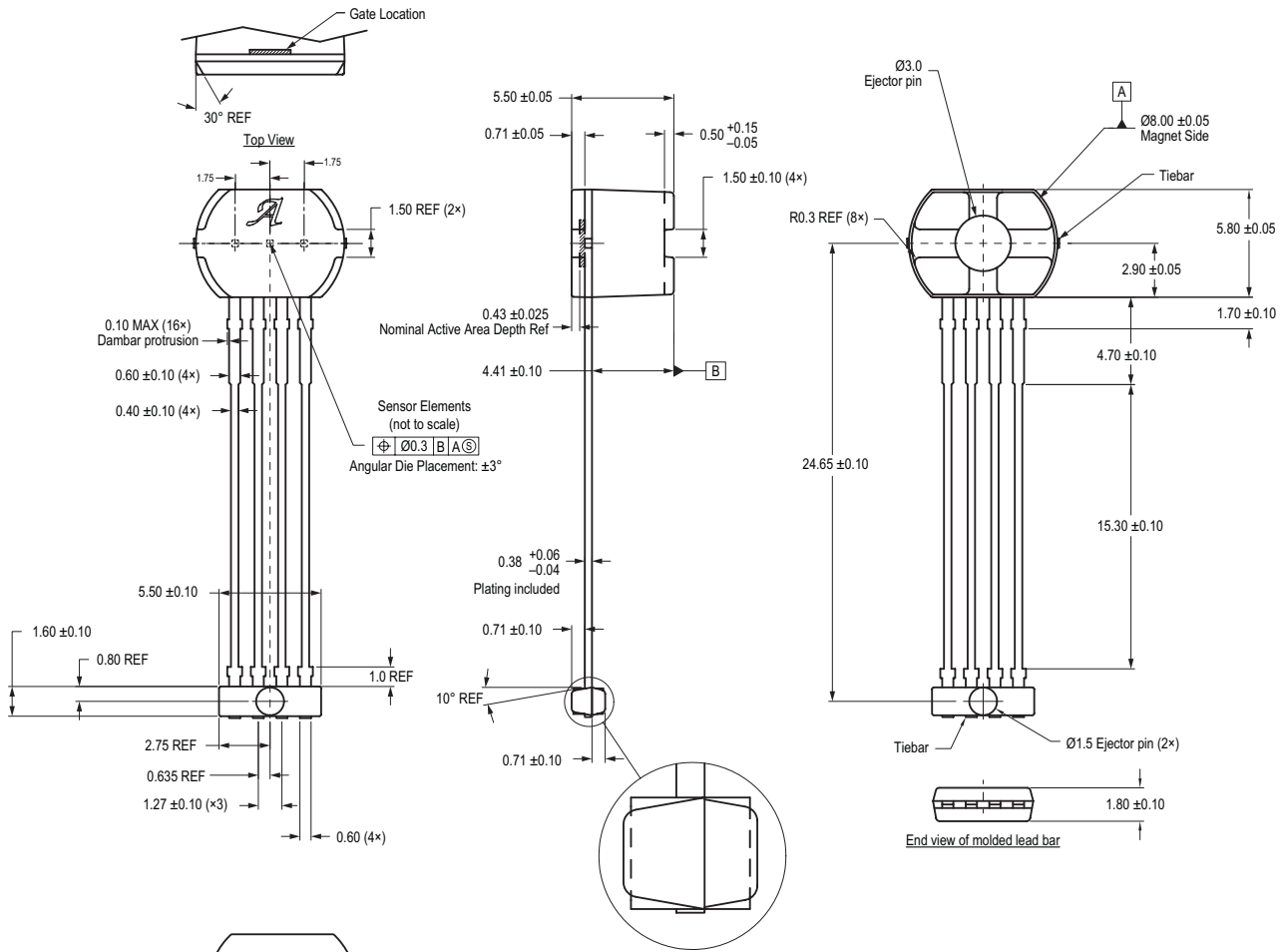
Compare  $V_{CC(est)}$  to  $V_{CC(max)}$ . If  $V_{CC(est)} \leq V_{CC(max)}$ , then reliable operation between  $V_{CC(est)}$  and  $V_{CC(max)}$  requires enhanced  $R_{\theta JA}$ . If  $V_{CC(est)} \geq V_{CC(max)}$ , then operation between  $V_{CC(est)}$  and  $V_{CC(max)}$  is reliable under these conditions.



**PACKAGE OUTLINE DRAWING**

**For Reference Only – Not for Tooling Use**

(Reference DWG-0000392)  
 Dimensions in millimeters. NOT TO SCALE.  
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
 Exact case and lead configuration at supplier discretion within limits shown



Branding scale and appearance at supplier discretion

**Figure 15: Package SG, 4-Pin SIP**

## Revision History

Number	Date	Description
–	November 18, 2019	Initial release
1	February 27, 2020	Updated Selection Guide (page 2), Electrical Protection Characteristics names and symbols (page 5), Operating Air Gap maximum value (page 7)
2	March 19, 2020	Updated Features and Benefits (page 1); removed 50%/50% switch point options (updated Selection Guide (page 2), Output Current Internal Limiter test conditions (page 5), Operate Point, Release Point, and Hysteresis characteristics (page 7); removed 50%/50% Dynamic Threshold Option figure (page 14); updated Output Protocol Options figure (page 16), Startup Hysteresis section (page 19); removed Hidden Hysteresis (page 20))
3	February 22, 2021	Removed Advance Information status and ASIL assessment status; updated Selection Guide; minor editorial updates
4	August 2, 2021	Split Operating Air Gap specification into fault detection mode disabled and enabled (page 7)
5	September 1, 2022	Updated product outline drawing and corrected reference drawing number (page 22)
6	March 8, 2023	Updated Output Characteristics (page 6)

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