

OP-77 Series Precision Operational Amplifiers

Features

- Ultra high gain – 5000 V/mV min
- Outstanding gain linearity
- Ultra low V_{os} drift – 0.3 $\mu\text{V}/\text{C}$ max
- Low V_{os} – 25 μV max
- Low noise – 0.3 μV_{p-p} (0.1 to 10 Hz)
- Low power consumption – 35 mW
- Low input offset current – 1.5 nA max
- High CMRR – 120 dB min
- High PSRR – 110 dB min
- Replaces OP-07, 108, 725, 741 types
- Wide range of package types

Description

Designed to upgrade OP-07 and other similar precision op amps, the OP-77 offers ultra high performance in applications requiring high gain, superior gain-linearity, and extremely low TCV_{os} . The OP-77's outstanding gain-linearity, which eliminates incorrecable system nonlinearities common in previous precision op amps, is achieved by an exceptional open-loop gain of more than 10 million maintained over $\pm 10\text{V}$ output range. The excellent TCV_{os} of 0.3 $\mu\text{V}/\text{C}$ maximum, plus an extremely low power consumption of 35 mW (which reduces warm-up drift) significantly increases system accuracy over temperature. These characteristics, along with low V_{os} , low I_{os} , high CMRR, high PSRR, and low input noise levels, combine to raise the performance level of many high-resolution instrumentation and data conversion systems.

Advanced circuit design and wafer processing are Raytheon's added advantages in quality and reliability. A patented, proprietary V_{os} trimming method after packaging significantly enhances yield and availability of top grade (A/E) devices.

Ordering Information

Part Number	Package	Operating Temperature Range
OP-77EN	N	0°C to +70°C
OP-77FN	N	0°C to +70°C
OP-77GN	N	0°C to +70°C
OP-77FM	M	0°C to +70°C
OP-77GM	M	0°C to +70°C
OP-77ET	T	-25°C to +85°C
OP-77FT	T	-25°C to +85°C
OP-77ED	D	-25°C to +85°C
OP-77FD	D	-25°C to +85°C
OP-77AT	T	-55°C to +125°C
OP-77AT/883B*	T	-55°C to +125°C
OP-77BT	T	-55°C to +125°C
OP-77BT/883B*	T	-55°C to +125°C
OP-77AD	D	-55°C to +125°C
OP-77AD/883B*	D	-55°C to +125°C
OP-77BD	D	-55°C to +125°C
OP-77BD/883B*	D	-55°C to +125°C
OP-77AL/883B*	L	-55°C to +125°C
OP-77BL/883B*	L	-55°C to +125°C

Notes:

/883B suffix denotes Mil-Std-883, Level B processing

N = 8-lead plastic DIP

D = 8 lead ceramic DIP

T = 8-lead metal can (TO-99)

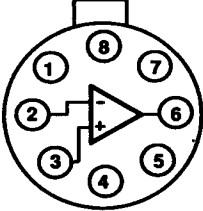
L = 20-pad leadless chip carrier

M = 8-lead plastic SOIC

Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

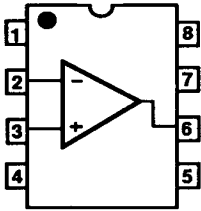
Connection Information

8-Lead TO-99 Metal Can
(Top View)



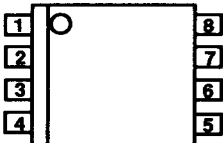
65-03205A

8-Lead Dual In-Line Package
(Top View)



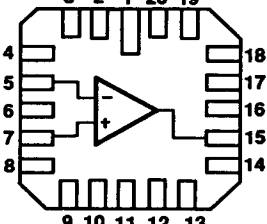
65-03206A

8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02696A

20-Pad LCC
(Top View)



65-02657A

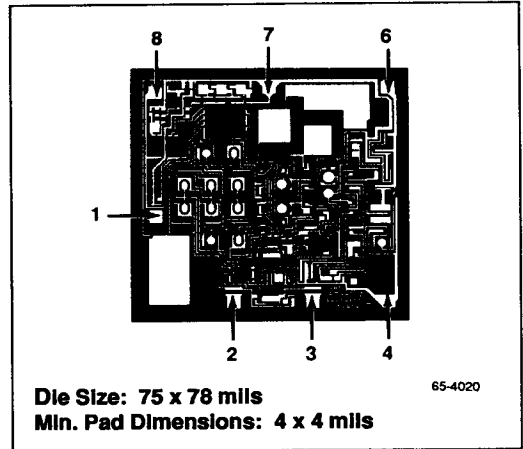
Pin	Function
1	V _{OS} Trim
2	-Input
3	+Input
4	-V _S (Case)
5	NC
6	Output
7	+V _S
8	V _{OS} Trim

Absolute Maximum Ratings

Supply Voltage	±22V
Input Voltage*	±22V
Differential Input Voltage	30V
Internal Power Dissipation**	500 mW
Output Short Circuit Duration	Indefinite
Storage Temperature	
Range	-65°C to +150°C
Operating Temperature Range	
OP77A,B	-55°C to +125°C
OP77E,F,G (Hermetic)	-25°C to +85°C
OP77E,F,G (Plastic)	0°C to +70°C
Lead Soldering Temperature	
TO-99, DIP, LCC (60 sec)	+300°C
SO-8 (10 sec)	+260°C

*For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
 **Observe package thermal characteristics.

Mask Pattern



Thermal Characteristics

	20-Pad LCC	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Plastic SO	8-Lead Plastic DIP
Max. Junction Temp.	175°C	175°C	175°C	125°C	125°C
Max. P _D T _A <50°C	925 mW	833 mW	658 mW	300 mW	468 mW
Therm. Res θ _{JC}	37°C/W	45°C/W	50°C/W	—	—
Therm. Res. θ _{JA}	105°C/W	150°C/W	190°C/W	240°C/W	160°C/W
For T _A >50°C Derate at	7.0 mW/°C	8.33 mW/°C	5.26 mW/°C	4.17 mW/°C	6.25 mW/°C

Electrical Characteristics ($V_s = \pm 15V$ and $T_A = +25^\circ C$ unless otherwise noted)

Parameters	Test Conditions	OP-77A			OP-77B			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ^a			± 10	± 25		± 20	± 60	μV
Long Term V_{OS} Stability ^a			0.2			0.2		$\mu V/Mo$
Input Offset Current			± 0.3	± 1.5		± 0.3	± 2.8	nA
Input Bias Current			± 1.2	± 2.0		± 1.2	± 2.8	nA
Input Noise Voltage ^a	0.1 Hz to 10 Hz		0.35	0.6		0.35	0.65	μV_{p-p}
Input Noise Voltage Density ^a	$F_o = 10$ Hz		10.3	18		10.3	18	$\frac{nV}{\sqrt{Hz}}$
	$F_o = 100$ Hz		10	13		10	13	$\frac{nV}{\sqrt{Hz}}$
	$F_o = 1000$ Hz		9.6	11		9.6	11	$\frac{nV}{\sqrt{Hz}}$
Input Noise Current ^a	0.1 Hz to 10 Hz		14	30		14	35	pA_{p-p}
Input Noise Current Density ^a	$F_o = 10$ Hz		0.32	0.8		0.32	0.8	$\frac{pA}{\sqrt{Hz}}$
	$F_o = 100$ Hz		0.14	0.23		0.14	0.23	$\frac{pA}{\sqrt{Hz}}$
	$F_o = 1000$ Hz		0.12	0.17		0.12	0.17	$\frac{pA}{\sqrt{Hz}}$
Input Resistance (Diff. Mode) ^a		26	45		18.5	45	M Ω	
Input Resistance (Com. Mode)			200			200	G Ω	
Input Voltage Range ^a		± 13	± 14		± 13	± 14	V	
Common Mode Rejection Ratio	$V_{CM} = \pm 11V$	120	140		116	140	dB	
Power Supply Rejection Ratio	$V_s = \pm 3V$ to $\pm 8V$	110	120		110	120	dB	
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_o = \pm 10V$	5000	12000		2000	8000	V/mV	
Output Voltage Swing	$R_L \geq 10$ k Ω ,	± 13	± 13.5		± 13	± 13.5	V	
	$R_L \geq 2$ k Ω ,	± 12.5	± 13		± 12.5	± 13		
	$R_L \geq 1$ k Ω ,	± 12	± 12.5		± 12	± 12.5		
Slew Rate ^a	$R_L \geq 2$ k Ω ,	0.1	0.2		0.1	0.2	V/ μS	
Closed Loop Bandwidth ^a	$A_{VCL} = +1.0$	0.4	0.6		0.4	0.6	MHz	
Open Loop Output Resistance	$V_o = 0$, $I_o = 0$		60			60	Ω	
Power Consumption	$V_s = \pm 15V$, $R_L = \infty$		35	60		35	60	mW
	$V_s = \pm 3V$, $R_L = \infty$		2.0	4.5		2.0	4.5	
Offset Adjustment Range	$R_p = 20$ k Ω		± 3.5			± 3.5	mV	

Notes:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV .
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. The OP-77A/E grades in T, D, and L packages are tested fully warmed up.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
5. Sample tested.

Electrical Characteristics ($V_s = \pm 15V$ and $T_A = +25^\circ C$ unless otherwise noted)

Parameters	Test Conditions	OP-77E			OP-77F			OP-77G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage*		± 10 ± 25			± 20 ± 60			± 50 ± 100			μV
Long Term Input Offset Voltage Stability*		0.3			0.4			0.4			$\mu V/Mo$
Input Offset Current		± 0.3 ± 1.5			± 0.3 ± 2.8			± 0.3 ± 2.8			nA
Input Bias Current		± 1.2 ± 2.0			± 1.2 ± 2.8			± 1.2 ± 2.8			nA
Input Noise Voltage*	0.1 Hz to 10 Hz	0.35 0.6			0.38 0.65			0.38 0.65			μV_{p-p}
Input Noise Voltage Density*	$F_o = 10$ Hz	10.3 18			10.5 20			10.5 20			nV
	$F_o = 100$ Hz	10 13			10.2 13.5			10.2 13.5			\sqrt{Hz}
	$F_o = 1000$ Hz	9.6 11			9.8 11.5			9.8 11.5			\sqrt{Hz}
Input Noise Current*	0.1 Hz to 10 Hz	14 30			15 35			15 35			pA_{p-p}
Input Noise Current Density*	$F_o = 10$ Hz	0.32 0.8			0.35 0.9			0.35 0.9			pA
	$F_o = 100$ Hz	0.14 0.23			0.15 0.27			0.15 0.27			\sqrt{Hz}
	$F_o = 1000$ Hz	0.12 0.17			0.13 0.18			0.13 0.18			\sqrt{Hz}
Input Resistance (Diff. Mode)*		26 45		18.5 45		18.5 45				M Ω	
Input Resistance (Com. Mode)		200			200			200			G Ω
Input Voltage Range*		± 13 ± 14			± 13 ± 14			± 13 ± 14			V
Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	120 140			116 140			116 140			dB
Power Supply Rejection Ratio	$V_s = \pm 3V$ to $\pm 18V$	110 123			110 123			110 123			dB
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_o = \pm 10V$	5000 12000			2000 6000			2000 6000			V/mV
Output Voltage Swing	$R_L \geq 10$ k Ω	± 13 ± 13.5			± 13 ± 13.5			± 13 ± 13.5			V
	$R_L \geq 2$ k Ω	± 12.5 ± 13			± 12.5 ± 13			± 12.5 ± 13			
	$R_L \geq 1$ k Ω	± 12 ± 12.5			± 12 ± 12.5			± 12 ± 12.5			
Slew Rate*	$R_L \geq 2$ k Ω	0.1 0.2			0.1 0.2			0.1 0.2			V/ μS
Closed-Loop Bandwidth*	$A_{VCL} = +1.0$	0.4 0.6			0.4 0.6			0.4 0.6			MHz
Open Loop Output Resistance	$V_o = 0, I_o = 0$	60			60			60			Ω
Power Consumption	$V_s = \pm 15V, R_L = \infty$	35 60			35 60			35 60			mW
	$V_s = \pm 3V, R_L = \infty$	2.0 4.5			2.0 4.5			2.0 4.5			
Offset Adjustment Range	$R_p = 20$ k Ω	± 3.5			± 3.5			± 3.5			mV

Notes:

- Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{os} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{os} during the first 30 operating days are typically 2.5 μV .
- Guaranteed by design.
- Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. The OP-77A/E grades on T, D, and L packages are tested fully warmed up.
- The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
- Sample tested.

Electrical Characteristics ($V_s = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ unless otherwise noted)

Parameters	Test Conditions	OP-77A			OP-77B			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			± 25	± 60		± 45	± 120	μV
Average Input Offset Voltage Drift ¹			0.1	0.3		0.2	0.6	$\mu V/^\circ C$
Input Offset Current			± 0.8	± 2.2		± 1.0	± 4.5	nA
Average Input Offset Current Drift ²			± 5.0	± 25		± 5.0	± 50	$\mu A/^\circ C$
Input Bias Current			± 2.4	± 4.0		± 2.4	± 6.0	nA
Average Input Bias Current Drift ²			± 8.0	± 25		± 15	± 35	$\mu A/^\circ C$
Input Voltage Range		± 13	± 13.5		± 13	± 13.5		V
Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	120	140		110	140		dB
Power Supply Rejection Ratio	$V_s = \pm 3V$ to $\pm 8V$	110	120		106	120		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	2000	6000		1000	4000		V/mV
Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	± 12	± 13		± 12	± 13		V
Power Consumption	$R_L = \infty$		40	75		40	75	mW

Electrical Characteristics
 $(V_s = \pm 15V$; $-25^\circ C \leq T_A \leq +85^\circ C$ for T, D, and L packages; $0^\circ C \leq T_A \leq +70^\circ C$ for N and M packages unless otherwise noted)

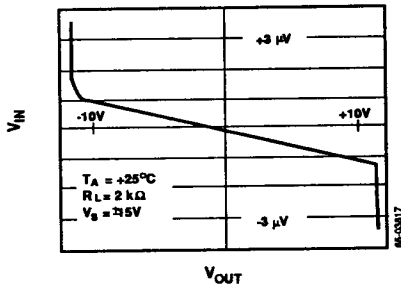
Parameters	Test Conditions	OP-77E			OP-77F			OP-77G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			± 10	± 45		± 20	± 100		± 80	± 100	μV
Average Input Offset Voltage Drift			0.1	0.3		0.2	0.6		0.3	1.2	$\mu V/^\circ C$
Input Offset Current			± 0.5	± 2.2		± 0.5	± 4.5		± 0.5	± 4.5	nA
Average Input Offset Current Drift ²			± 1.5	± 40		± 1.5	± 85		± 1.5	± 85	$\mu A/^\circ C$
Input Bias Current			± 2.4	± 4.0		± 2.4	± 6.0		± 2.4	± 6.0	nA
Average Input Bias Current Drift ²			± 8	± 40		± 15	± 60		± 15	± 60	$\mu A/^\circ C$
Input Voltage Range		± 13	± 13.5		± 13	± 13.5		± 13	± 13.5		V
Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	120	140		110	140		110	140		dB
Power Supply Rejection Ratio	$V_s = \pm 3V$ to $\pm 18V$	110	120		106	120		106	120		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	2000	6000		1000	4000		1000	4000		V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	± 12	± 13		± 12	± 13		± 12	± 13		V
Power Consumption	$R_L = \infty$		40	75		40	75		40	75	mW

Notes:

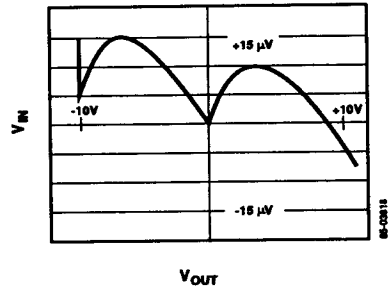
- 100% tested for Grade A on T, and L packages.
- Sample tested.

Raytheon

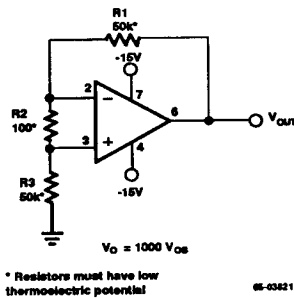
4-115



OP-77 Improved Open-Loop Gain Linearity



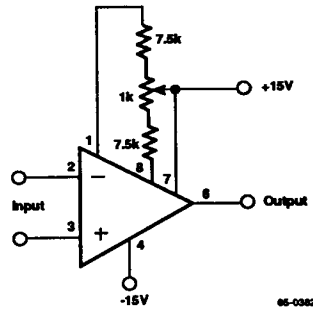
Typical Precision Op Amp Gain Linearity



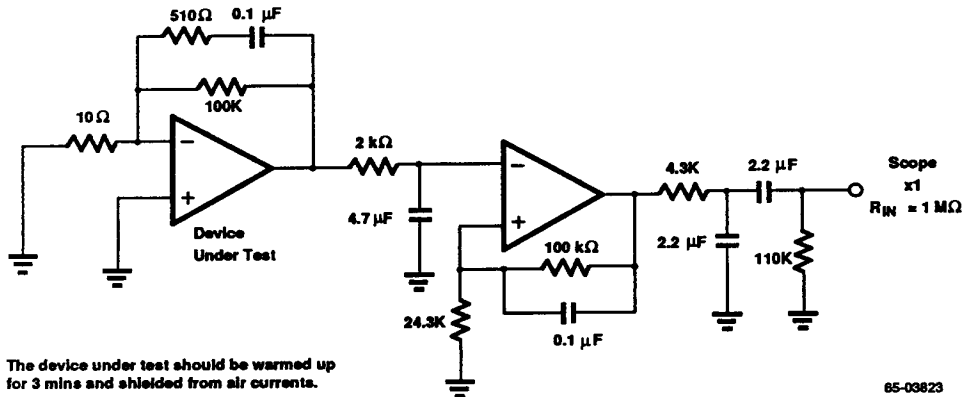
* Resistors must have low thermoelectric potential

65-03821

Test Circuit for Offset Voltage and its Drift With Temperature



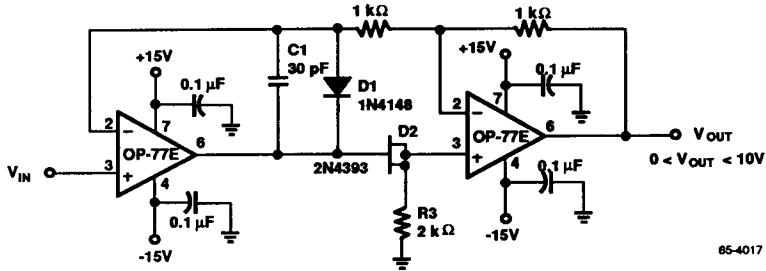
Improved Sensitivity V_{OS} Adjustment



The device under test should be warmed up for 3 mins and shielded from air currents.

0.1 Hz to 10 Hz Noise Test Circuit
(peak to peak noise measured in 10 sec interval)

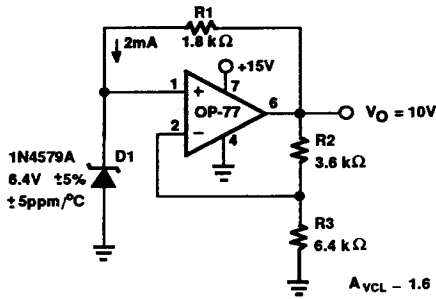
Typical Applications



65-4017

The high gain and low TCV_{OS} assure accurate operation with inputs from microvolts to volts. In this circuit, the signal always appears as a common-mode signal to the op amps. The OP-77E CMRR of $1 \mu V/V$ assures errors of less than 2 ppm.

Precision Absolute Value Amplifier

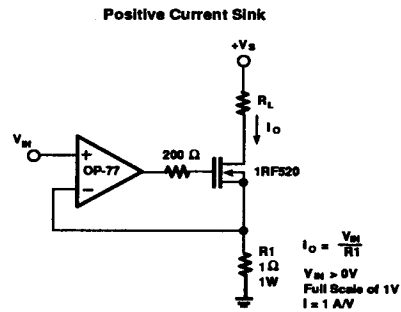


65-04018

This simple bootstrapped voltage reference provides a precise 10V virtually independent of changes in power supply voltage, ambient temperature and output loading. Correct zener operating current of exactly 2 mA is maintained by R1, a selected 5 ppm/C resistor, connected to the regulated output. Accuracy is primarily determined by three factors: the 5 ppm/C temperature coefficient of D1, 1 ppm/C ratio tracking of R2 and R3, and operational amplifier V_{OS} errors.

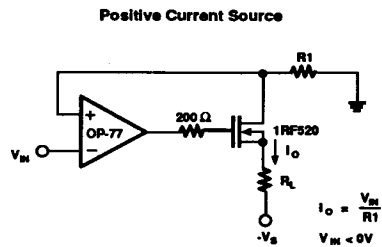
V_{OS} errors, amplified by 1.6 (A_{VCL}), appear at the output and can be significant with most monolithic amplifiers. For example: an ordinary amplifier with TCV_{OS} of $5 \mu V/C$ contributes 0.8 ppm/C of output error while the OP-77, with TCV_{OS} of $0.3 \mu V/C$, contributes but 0.05 ppm/C of output error, thus effectively eliminating TCV_{OS} as an error consideration.

High Stability Voltage Reference



$$I_o = \frac{V_{IN}}{R1}$$

$V_{IN} > 0V$
Full Scale of 1V
 $I = 1 \mu A$



$$I_o = \frac{V_{IN}}{R1}$$

$V_{IN} < 0V$

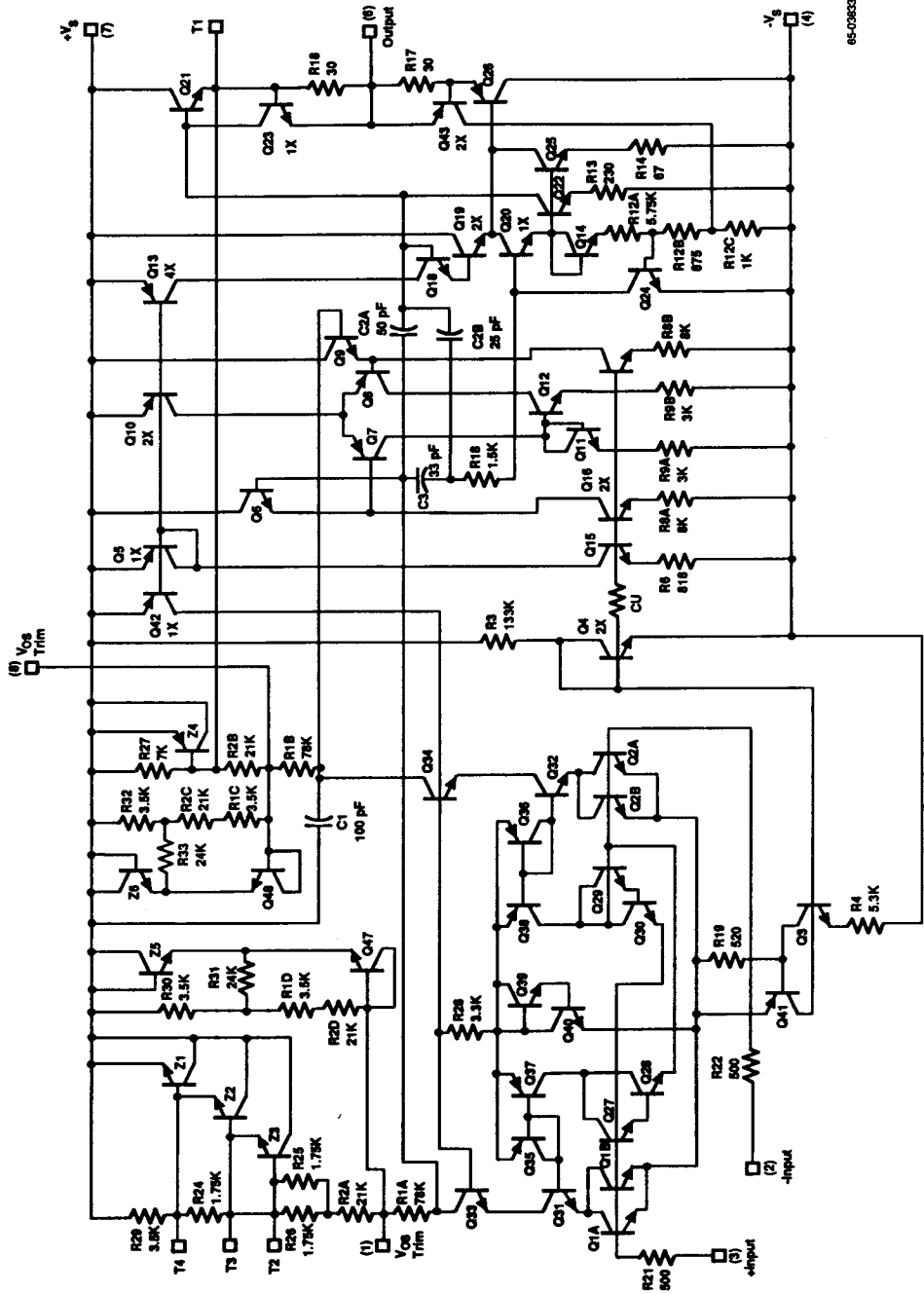
65-04019

These simple high current sinks require that the load float between the power supply and the sink.

In these circuits, OP-77's high gain, high CMRR, and low TCV_{OS} assure high accuracy.

Precision Current Sinks

Simplified Schematic Diagram



65-08633

