ZVN13A

PRODUCT CHARACTERIZATION

N-Channel Enhancement-Mode Vertical DMOS Power FET's.

APPLICATIONS:

- Direct Interfacing with Microprocessors and IC Logic Families (CMOS, TTL, DTL and MOS) to Drive High Current/High Voltage outputs.
- Power Supply Circuits: Switch Mode Supplies, DC/DC Converters, Regulators and Current Sources
- Audio Amplification: Push-Pull Audio Outputs, High Performance Linear Class A and Fast Class D operation.
- RF Amplification: Low Noise Amplification at High Frequencies and RF Output Stages.
- Analog Switching (Including Variable Resistance Applications).
- High Speed Switching Drivers for Displays, Lamps, Relays and Solenoids.
- Sensor Applications: Touch Switches and Delay Circuits.
- Timing and Delay Circuits.

FEATURES:

- Silicon-Gate Vertical DMOS Planar Process for Increased Stability
- Interdigitated Geometry for Low Input Capacitance and Fast Switching Speeds.
- Low Drive Current Requirement (I_{GSS} < 100nA).
- High Input Impedance and High Gain.
- Easily Paralleled without the need for Base Current Sharing Resistors.
- No Thermal Runaway or Thermally Induced Secondary Breakdown.
- Complementary N-Channel and P-Channel Devices.

CHIP SIZE: .030" x .030"

ABSOLUTE MAXIMUM RATINGS:

V_{DS} Drain-Source Voltage	
ZVN1304	40V
ZVN1306	60V
ZVN1308	80V
ZVN1309	90V
V_{DG} Drain-Gate Voltage	
ZVN1304	40V
ZVN1306	60V
ZVN1308	80V
ZVN1309	90V
I_D Continuous Drain Current (see note 1)	1.5A
I_{DM} Pulsed Drain Current (see notes 1 & 2)	3A
V_{GS} Gate-Source Voltage	±20V
Operating and Storage Temperature	−55 to + 150 °C

NOTE 1: The power dissipation capability of a packaged device may result in lower practical continuous and pulsed drain currents. Refer to the Product Selector section for details.
NOTE 2: Measured under pulsed conditions. Pulse width = 300μs. Duty cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS
(at 25°C ambient temperature unless otherwise stated)

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
1.	Drain-Source Breakdown Voltage	BV_{DSS}					
	ZVN1304		40	–	–	V	I_D = 1mA, V_{GS} = 0V
	ZVN1306		60	–	–	V	
	ZVN1308		80	–	–	V	
	ZVN1309		90	–	–	V	
2.	Gate-Threshold Voltage	$V_{GS(th)}$	0.8	–	2.4	V	I_D = 1mA, V_{DS} = V_{GS}
3.	Gate-Body Leakage	I_{GSS}	–	0.1	100	nA	V_{GS} = ±20V, V_{DS} = 0
4.	Zero Gate Voltage Drain Current	I_{DSS}	–	–	1	μA	V_{DS} = Max. Rating, V_{GS} = 0
			–	–	50	μA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0, T_{amb} = 125°C (Note 2)
5.	On-State Drain Current*	$I_{D(on)}$	0.25	0.6	–	A	V_{DS} = 25V, V_{GS} = 5V
			0.5	1.4	–	A	V_{DS} = 25V, V_{GS} = 10V
6.	Static Drain-Source On-State Resistance*	$R_{DS(on)}$					
	ZVN1304		–	11	15	Ω	I_D = 50mA, V_{GS} = 5V
	ZVN1306		–	12	15	Ω	
	ZVN1308		–	13	15	Ω	
	ZVN1309		–	14	15	Ω	
	ZVN1304		–	4	10	Ω	I_D = 500mA, V_{GS} = 10V
	ZVN1306		–	5	10	Ω	
	ZVN1308		–	6	10	Ω	
	ZVN1309		–	7	10	Ω	
7.	Forward Transconductance*	g_{fs}	200	250	–	m℧	V_{DS} = 25V, I_D = 0.5A (Note 2)
8.	Input Capacitance	C_{iss}	–	27	30	pF	V_{DS} = 25V, V_{GS} = 0, f = 1MHz. (Note 2)
9.	Common Source Output Capacitance	C_{oss}	–	13	15	pF	
10.	Reverse Transfer Capacitance	C_{rss}	–	3	5	pF	
11.	Turn-On Delay Time	$t_{d(on)}$	–	3	5	ns	V_{DD} = 25V, I_D = 0.5A (Notes 1 & 2)
12.	Rise Time	t_r	–	5	7	ns	
13.	Turn-Off Delay Time	$t_{d(off)}$	–	4	6	ns	
14.	Fall Time	t_f	–	5	7	ns	

*Measured under pulsed conditions. Pulse width = 300μs. Duty cycle ≤2%.
NOTE 1: Switching times measured with 50 ohm source impedance and 5ns rise time on a pulse generator.
NOTE 2: Sample test.

TYPICAL ELECTRICAL CHARACTERISTIC CURVES
(at 25°C ambient temperature unless otherwise stated)

Fig. 1—OUTPUT CHARACTERISTICS

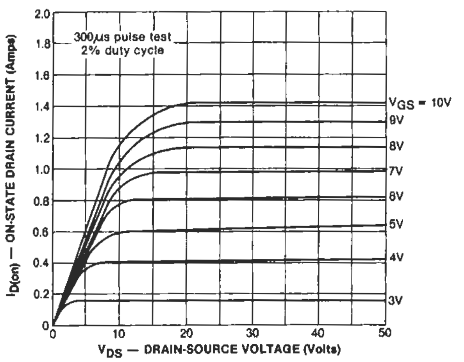


Fig. 2—SATURATION CHARACTERISTICS

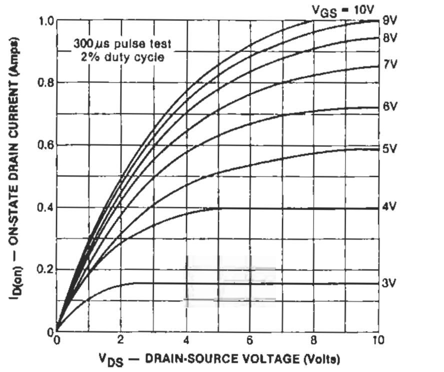


Fig. 3—TRANSFER CHARACTERISTICS

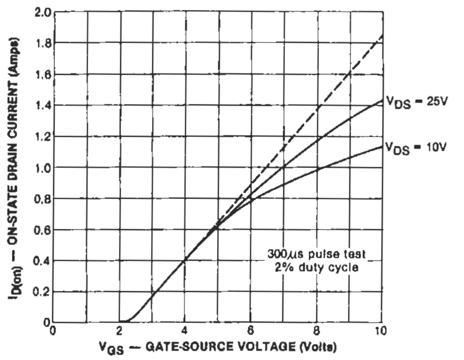


Fig. 4—CAPACITANCE vs DRAIN-SOURCE VOLTAGE

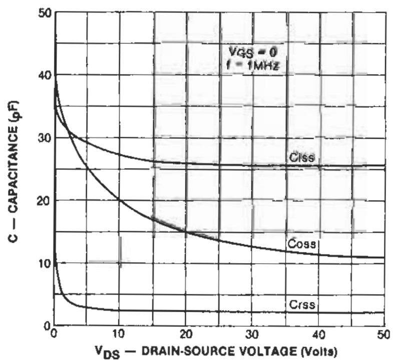


Fig. 5—TRANSCONDUCTANCE vs DRAIN CURRENT

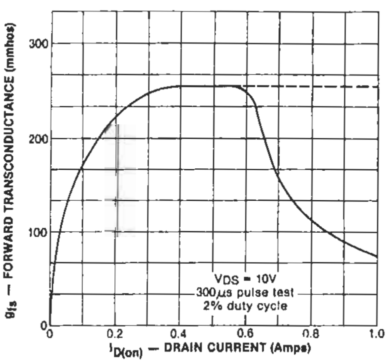
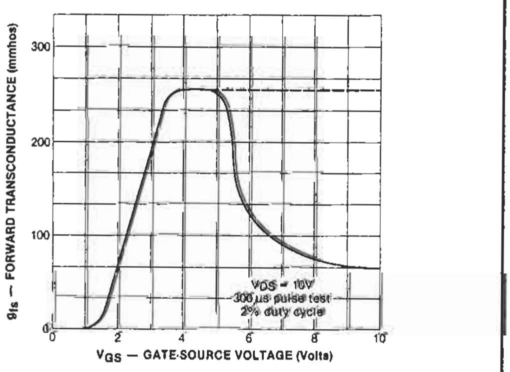


Fig. 6—TRANSCONDUCTANCE vs GATE-SOURCE VOLTAGE



TYPICAL ELECTRICAL CHARACTERISTIC CURVES (Cont'd)

(at 25°C ambient temperature unless otherwise stated)

Fig. 7—ON RESISTANCE vs GATE-SOURCE VOLTAGE

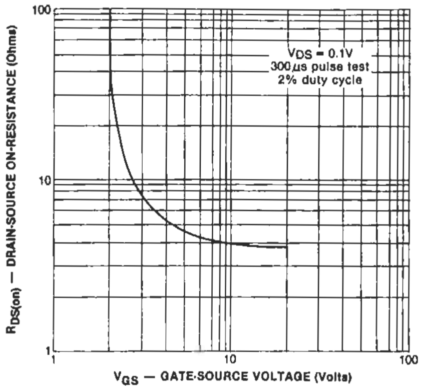


Fig. 8—NORMALIZED DRAIN-SOURCE RESISTANCE AND GATE-THRESHOLD VOLTAGE vs TEMPERATURE

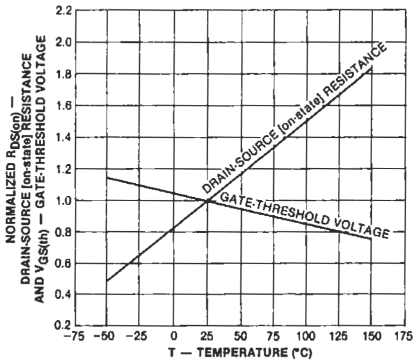


Fig. 9—GATE CHARGE vs GATE-SOURCE VOLTAGE AND DRAIN-SOURCE VOLTAGE

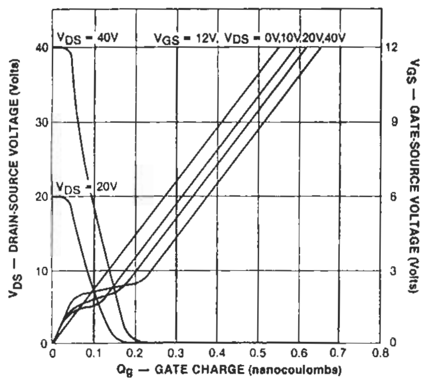


Fig. 10—SAFE OPERATING AREA

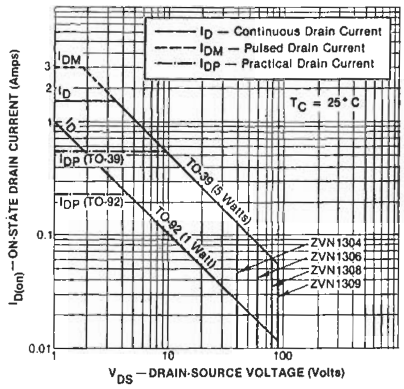


Fig. 11—POWER DISSIPATION vs AMBIENT TEMPERATURE

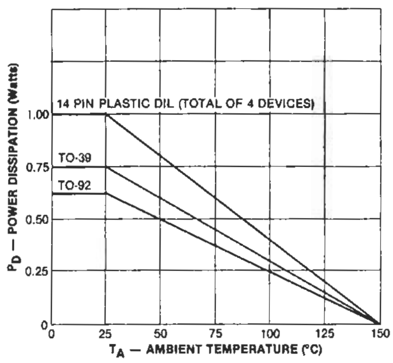


Fig. 12—POWER DISSIPATION vs CASE TEMPERATURE