

**NEC**  
NEC Electronics Inc.

**μPD43256**  
**32,768 x 8-BIT**  
**STATIC MIX-MOS RAM**

Revision 1

**Description**

The μPD43256 is a high-speed, low-power, 32,768-word by 8-bit static MIX-MOS RAM fabricated with advanced silicon-gate MIX-MOS technology. The μPD43256 is a low standby power device using n-channel memory cells with polysilicon resistors. Furthermore, a novel circuitry technique makes the μPD43256 a high-speed and low operating power device which requires no clock or refreshing to operate.

Minimum standby power is drawn by this device when CS is at a high level, independently of the other inputs' levels.

Data retention is guaranteed at a power supply voltage as low as 2 V (μPD43256-10L/12L/15L).

The μPD43256C is packaged in a standard 28-pin plastic dual-in-line package.

The μPD43256G is packaged in a standard 28-pin plastic miniflat (SOP) package.

**Features**

- Single +5 V supply
- Fully static operation — no clock or refreshing required
- TTL-compatible — all inputs and outputs
- Common I/O using three-state output
- One Chip Select and one Output Enable input for easy application
- Data retention voltage  
— μPD43256-10L/12L/15L: 2 V min
- Standard 28-pin plastic DIP and miniflat (SOP) packages

**Performance Ranges**

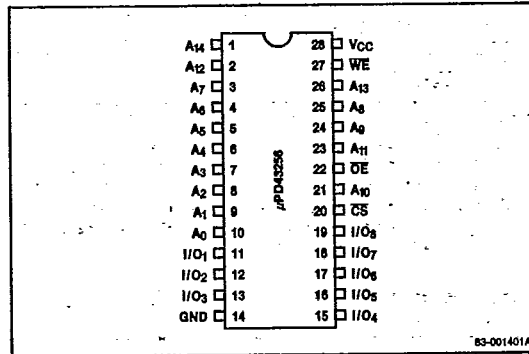
Device	Access Time	Cycle Time	Power Supply (Max)	
			Active	Standby
μPD43256-10	100 ns	100 ns	70 mA	2 mA
μPD43256-12	120 ns	120 ns	70 mA	2 mA
μPD43256-15	150 ns	150 ns	70 mA	2 mA
μPD43256-10L	100 ns	100 ns	70 mA	100 μA
μPD43256-12L	120 ns	120 ns	70 mA	100 μA
μPD43256-15L	150 ns	150 ns	70 mA	100 μA

**Capacitance**

T<sub>A</sub> = 25°C, f = 1 MHz

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input capacitance	C <sub>IN</sub>			5	pF	V <sub>IN</sub> = 0V
Input/output capacitance	C <sub>I/O</sub>			8	pF	V <sub>I/O</sub> = 0V

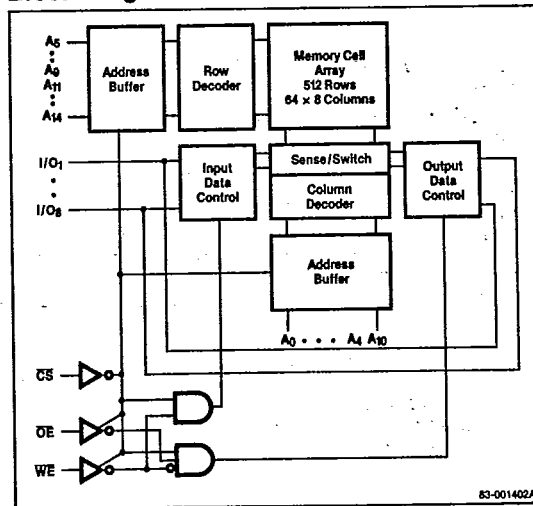
**Pin Configuration**



**Pin Identification Table**

No.	Symbol	Function
1-10, 21, 23-26	A <sub>0</sub> -A <sub>14</sub>	Address input
11-13, 15-19	I/O <sub>1</sub> -I/O <sub>8</sub>	Data input/output
14	GND	Ground
20	CS	Chip select
22	OE	Output enable
27	WE	Write enable
28	VCC	Power (+5 V)

**Block Diagram**



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**μPD43256**



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**Absolute Maximum Ratings**

Power supply voltage, $V_{CC}$	-0.5[1] to 7.0 V
Input voltage, $V_{IN}$	-0.5[1] to $V_{CC} + 0.5 V$
Output voltage, $V_{I/O}$	-0.5[1] to $V_{CC} + 0.5 V$
Operating temperature, $T_{OPR}$	0 to 70°C
Storage temperature, $T_{STG}$	-55 to 125°C
Power dissipation, $P_D$	1.0 W

Note: [1] -3.0 V min (pulse width 50 ns)

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended DC Operating Conditions**

$T_A = 0$  to 70°C

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
Input low voltage	$V_{IL}$	-0.3[1]		0.8	V
Input high voltage	$V_{IH}$	2.2		$V_{CC} + 0.5$	V

Note: [1] -3.0 V min (pulse width 50 ns)

**DC Characteristics**

$T_A = 0$  to 70°C,  $V_{CC} = 5 V \pm 10\%$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input leakage current	$I_{LI}$			1	$\mu A$	$V_{IN} = 0$ to $V_{CC}$
I/O leakage current	$I_{LO}$			1	$\mu A$	$V_{I/O} = 0$ to $V_{CC}$ $\overline{CS} \geq V_{IH}$ or $OE \geq V_{IH}$ or $WE < V_{IL}$
Operating supply current	$I_{CCA}$	Note 1	70		mA	$\overline{CS} < V_{IL}$ , Min Cycle $I_{I/O} = 0$
Standby supply current	$I_{SB}$		Note 2		mA	$\overline{CS} \geq V_{IH}$
Standby supply current	$I_{SB1}$	Note 3	Note 3		mA	$\overline{CS} \geq V_{CC} - 0.2 V$
Output low voltage	$V_{OL}$			0.4	V	$I_{OL} = 2.1 mA$
Output high voltage	$V_{OH}$	2.4			V	$I_{OH} = -1.0 mA$

- Notes: [1] μPD43256-10/10L: 35 mA typ  
 μPD43256-12/12L: 30 mA typ  
 μPD43256-15/15L: 25 mA typ  
 [2] μPD43256-10/12/15: 5 mA max  
 μPD43256-10L/12L/15L: 3 mA max  
 [3] μPD43256-10/12/15: 20 μA typ, 2 mA max  
 μPD43256-10L/12L/15L: 2 μA typ, 100 μA max

**AC Characteristics**

$T_A = 0$  to 70°C,  $V_{CC} = 5 V \pm 10\%$

Parameter	Symbol	μPD43256-10/10L		μPD43256-12/12L		μPD43256-15/15L		Unit
		Min	Max	Min	Max	Min	Max	
<b>Read Cycle</b>								
Read cycle time	$t_{RC}$	100		120		150		ns
Address access time	$t_{AA}$		100		120		150	ns
Chip select access time	$t_{ACS}$		100		120		150	ns
Output enable to output valid	$t_{OE}$		50		60		70	ns
Output hold from address change	$t_{OH}$	10		10		10		ns
Chip select to output in Lo-Z	$t_{CLZ}$	10		10		10		ns
Output enable to output in Lo-Z	$t_{OLZ}$	5		5		5		ns
Chip select to output in Hi-Z	$t_{CHZ}$		35		40		50	ns
Output enable to output in Hi-Z	$t_{OHZ}$		35		40		50	ns
<b>Write Cycle</b>								
Write cycle time	$t_{WC}$	100		120		150		ns
Chip select to end of write	$t_{CW}$	80		85		100		ns
Address valid to end of write	$t_{AW}$	80		85		100		ns
Address setup time	$t_{AS}$	0		0		0		ns
Write pulse width	$t_{WP}$	70		70		90		ns
Write recovery time	$t_{WR}$	5		5		5		ns
Data valid to end of write	$t_{DW}$	40		50		60		ns
Data hold time	$t_{DH}$	0		0		0		ns
Write enable to output in Hi-Z	$t_{WHZ}$		35		40		50	ns
Output active from end of write	$t_{OW}$	10		10		10		ns

**AC Test Conditions**

Input pulse levels	0.8 to 2.2 V
Input pulse rise and fall time	5 ns
Timing reference levels	1.5 V

**Truth Table**

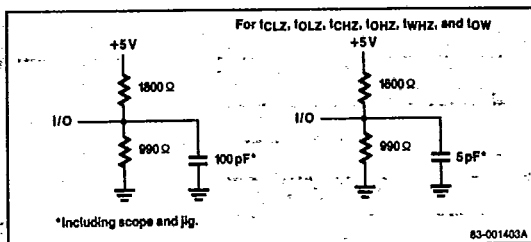
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	$I_{cc}$
H	X	X	Not selected	Hi-Z	Standby
L	H	H	Not selected	Hi-Z	Active
L	L	H	Read	$D_{OUT}$	Active
L	X	L	Write	$D_{IN}$	Active

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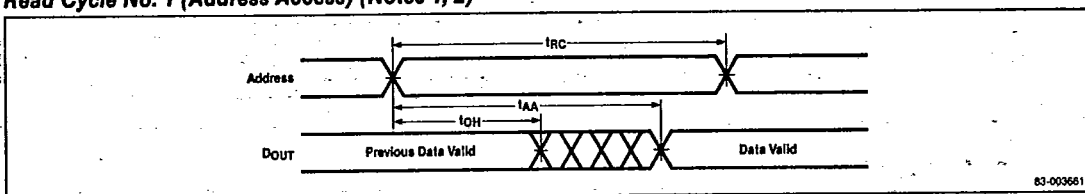
**μPD43256**

**AC Test Circuits**

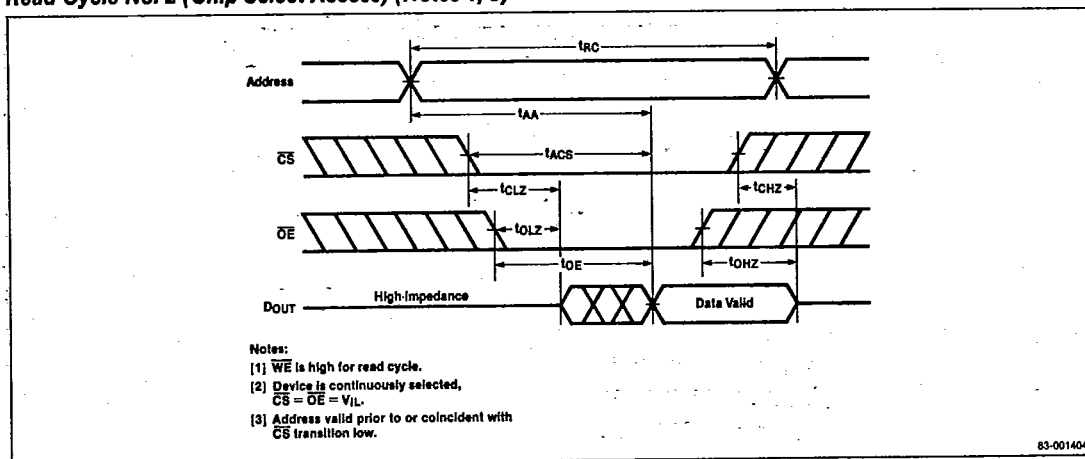


**Timing Waveforms**

**Read Cycle No. 1 (Address Access) (Notes 1, 2)**



**Read Cycle No. 2 (Chip Select Access) (Notes 1, 3)**



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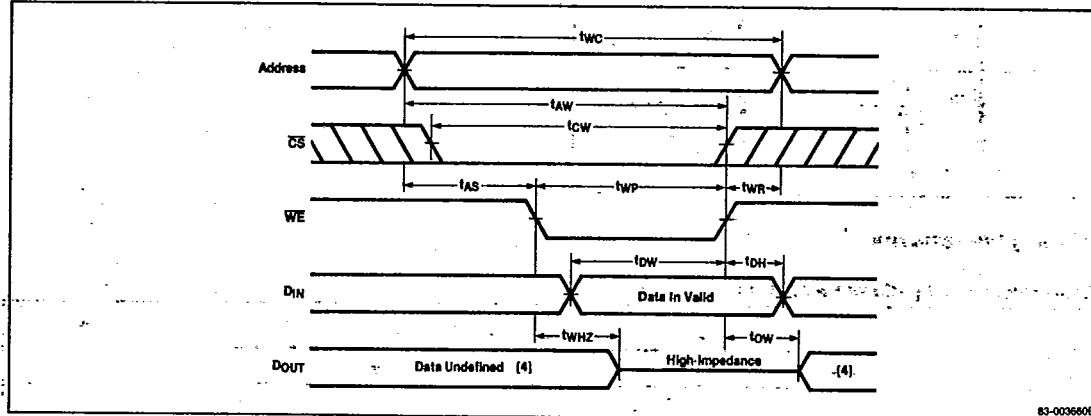
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$\mu$ PD43256

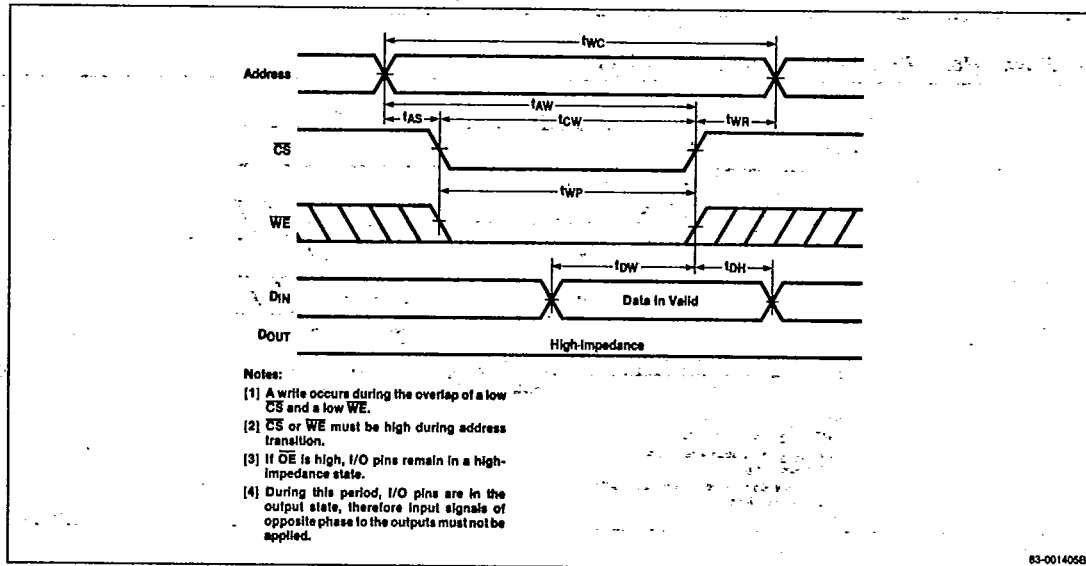
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**Timing Waveforms (Cont)**

**Write Cycle No. 1 ( $\overline{WE}$  Controlled) (Notes 1, 2, 3)**



**Write Cycle No. 2 ( $\overline{CS}$  Controlled) (Notes 1, 2)**



- Notes:
- [1] A write occurs during the overlap of a low CS and a low WE.
  - [2] CS or WE must be high during address transition.
  - [3] If  $\overline{OE}$  is high, I/O pins remain in a high-impedance state.
  - [4] During this period, I/O pins are in the output state, therefore input signals of opposite phase to the outputs must not be applied.



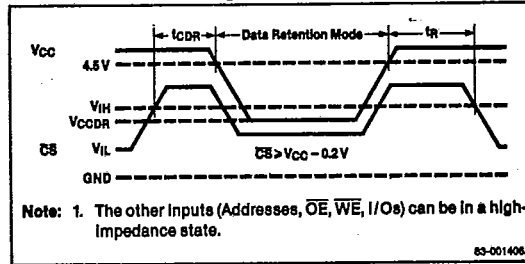
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$\mu$ PD43256

**Low V<sub>CC</sub> Data Retention Characteristics**  
 T<sub>A</sub> = 0 to 70°C for  $\mu$ PD43256-10L/12L/15L

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Data retention supply voltage	V <sub>CCDR</sub>	2.0		5.5	V	CS > V <sub>CC</sub> - 0.2V
Data retention supply current	I <sub>CCDR</sub>		1	50	$\mu$ A	V <sub>CC</sub> = 3.0V, CS > V <sub>CC</sub> - 0.2V
Chip deselection to data retention mode	t <sub>CDR</sub>	0			ns	
Operation recovery time	t <sub>R</sub>	t <sub>RC</sub>			ns	

**Data Retention Timing Chart**



Note: 1. The other inputs (Addresses,  $\overline{OE}$ ,  $\overline{WE}$ , I/Os) can be in a high-impedance state.

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