MSM58292B

5-DIGIT STATIC LCD DRIVER

GENERAL DESCRIPTION

The OKI MSM58292BGS is a 7-segment static LCD driver LSI which is fabricated by low power CMOS metal gate technology. This LSI ocnsists of 32-bit shift register, 32-bit latch, 5 sets of 7-segment decoder and LCD drivers.

It receives the serial display data from the microcomputer etc, converts it to a parallel data, then output to the 7-segment LCD panel.

The input code for each digit is a 4-bit binary code. The input codes are decoded into digits 0 ~ 9 and alphabetic letters A ~ F, to display hexadecimal numbers. The expansion of display can be easily made by using another MSM58292BGS in cascade connection.

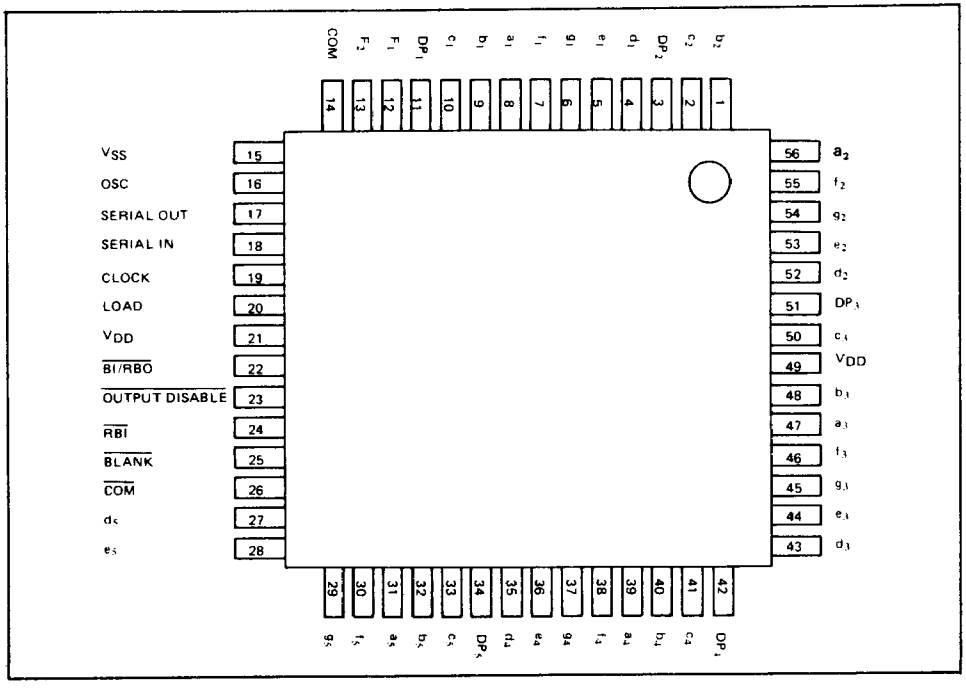
The MSM58292BGS can directly drive the LCD panel, as the AC driving circuit is integrated on the chip.

FEATURES

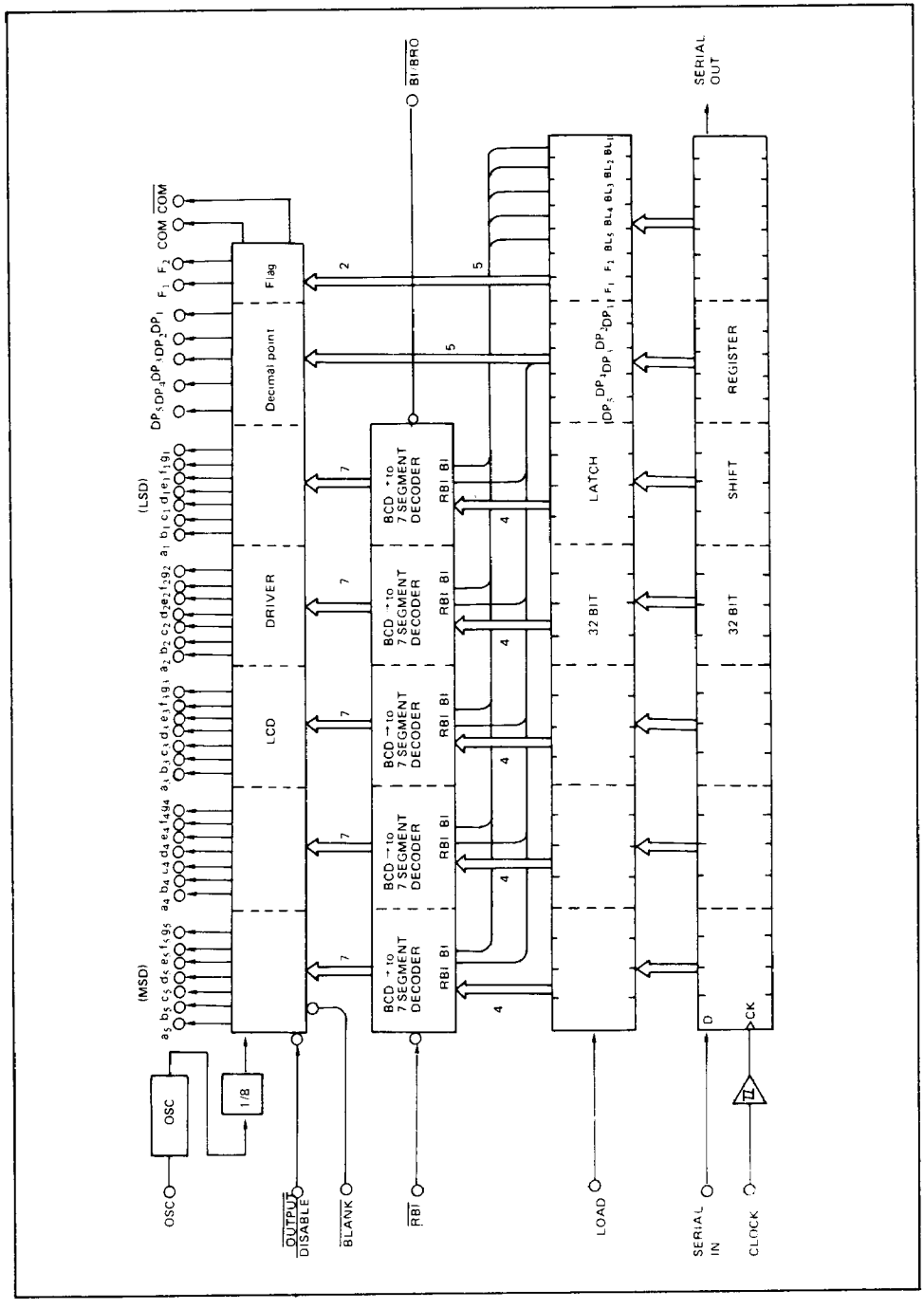
- 5 digit 7-segment LCD display
- Serial input from the microcomputer etc.
- Expansion of display by cascade connection
- Supply voltage: 4 ~ 7V
- 56 pin (s) plastic QFP (QFP56-P-910)
- 56 pin (s) plastic QFP (QFP56-P-910-K)

PIN CONFIGURATION

(Top view) 56 pin (s) plastic QFP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V_{DD}	T_a = 25°C	−0.3 ~ 7	V
Input voltage	V_I		−0.3 ~ V_{DD}	V
Storage temperature	Tstg	—	−55 ~ +150	°C

OPERATING RANGE

Parameter		Symbol	Condition	Limits	Unit
Supply voltage		V_{DD}	–	4 ~ 7	V
Operating temperature		T_{OP}	–	−30 ~ +85	°C
Fan out	$\overline{BI/RBO}$	N	MOS load	1	–
	SERIAL OUT	N	MOS load	40	–
			TTL load	1	–

DC CHARACTERISTICS

(V_{DD} = 5V ± 5%, T_a = −30 ~ +85°C)

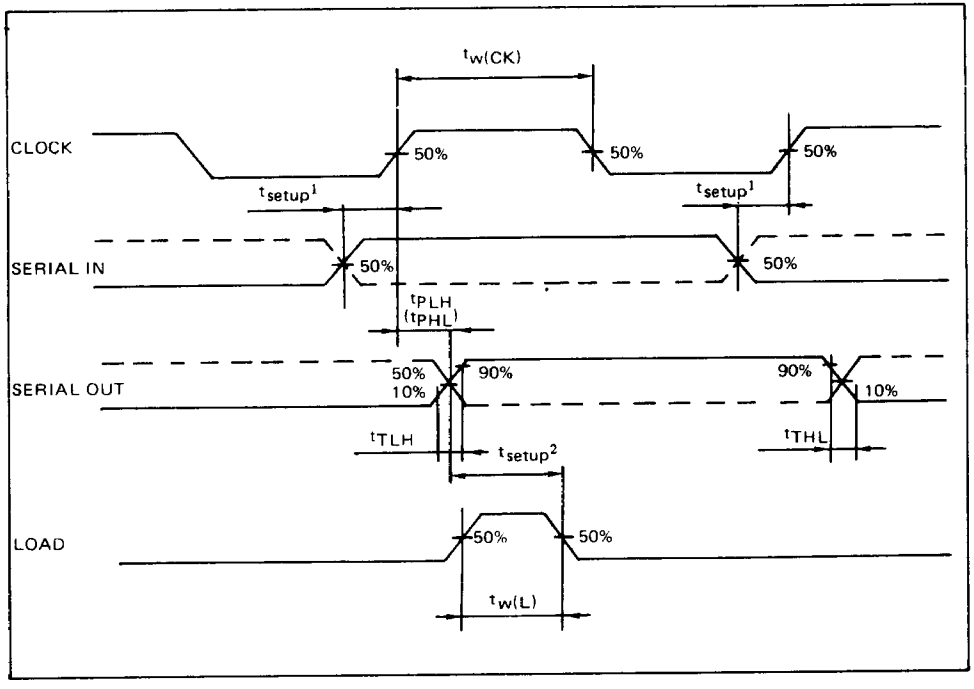
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input voltage	V_{IH}	–	3.6	–	–	V
"L" Input voltage[6]	V_{IL}	–	–	–	0.8 0.05	V V
"H" Output voltage[1]	V_{OH}	I_O = −5 μA	4.95	–	–	V
"L" Output voltage[1]	V_{OL}	I_O = 5 μA	–	–	0.05	V
"H" Output voltage[2]	V_{OH}	I_O = −40 μA	4.2	–	–	V
"L" Output voltage[2]	V_{OL}	I_O = 1.6mA	–	–	0.4	V
"H" Output voltage[3]	V_{OH}	I_O = −500 μA	4.5	–	–	V
"L" Output voltage[3]	V_{OL}	I_O = 500 μA	–	–	0.5	V
"H" Output voltage[4]	V_{OH}	I_O = −250 μA	4.5	–	–	V
"L" Output voltage[4]	V_{OL}	I_O = 250 μA	–	–	0.5	V
Input current[5]	I_{IH}/I_{IL}	$V_I = V_{DD}/V_I$ = 0V	–	–	1/−1	μA
Output current[1]	I_{OH}/I_{OL}	V_O = 0V /V_O = V_{DD}	−0.2/ 0.2	–	–	mA
Output current[2]	I_{OH}/I_{OL}	V_O = 2.5V/V_O = 0.4V	−0.2/ 1.6	–	–	mA
$\overline{BI/RBO}$ short-circuit current	I_{OH}/I_{OL}	V_O = 0V /V_O = V_{DD}	−10/ 10	–	−500/ 500	μA
Dynamic current consumption	I_{DD}	$f_{(OSC)}$ = 360Hz no load	–	–	500	μA

Note 1: Applied to the output pins excluding the SERIAL OUT, $\overline{BI/RBO}$, $\overline{COM}$ and COM Pins.
Note 2: Applied to the SERIAL OUT pin.
Note 3: Applied to the COM pin.
Note 4: Applied to the COM pin.
Note 5: Applied to the input pins excluding the OSC pin.
Note 6: Applied to the $\overline{BI/RBO}$ PIN.

SWITCHING CHARACTERISTICS

(V_{DD} = 5V, T_a = 25°C, CL = 15pF)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Propagation delay time (for a shift in the shift register)	t_{PHL} t_{PLH}	–	–	–	1000	nS
SERIAL OUT rise/fall time	t_{THL} t_{TLH}	–	–	–	300	nS
Maximum clock frequency	$f_{(CK)\ max}$	–	1	–	–	MHz
Minimum clock pulse width	$t_{w(CK)}$	–	–	–	500	nS
Minimum load pulse width	$t_{w(L)}$	–	–	–	500	nS
Data setup time SERIAL IN → CLOCK	t_{setup}^{1}	–	–	–	250	nS
Data setup time SERIAL OUT → LOAD	t_{setup}^{2}	–	–	–	500	nS



FUNCTION TABLE

Hexadecimal digit	$\overline{RBI}$	$\overline{BI/RBO}$	SEGMENT OUT (Note 1)							Display
			a	b	c	d	e	f	g	
*	*	L	L	L	L	L	L	L	L	(Note 3)
0	*	(Note 2)	L	L	L	L	L	L	L	(Note 4)
0	*	H	H	H	H	H	H	H	L	
1	*	H	L	H	H	L	L	L	L	
2	*	H	H	H	L	H	H	L	H	
3	*	H	H	H	H	H	L	L	H	
4	*	H	L	H	H	L	L	H	H	
5	*	H	H	L	H	H	L	H	H	
6	*	H	H	L	H	H	H	H	H	
7	*	H	H	H	H	L	L	L	L	
8	*	H	H	H	H	H	H	H	H	
9	*	H	H	H	H	H	L	H	H	
A	*	H	H	H	H	L	H	H	H	
B	*	H	L	L	H	H	H	H	H	
C	*	H	H	L	L	H	H	H	L	
D	*	H	L	H	H	H	H	L	H	
E	*	H	H	L	L	H	H	H	H	
F	*	H	H	L	L	L	H	H	H	

Note 1: The H indicates that the segment is displayed, and the L indicates that the segment is not displayed. The H is an antiphase output of the COM output, and the L is an in-phase output of the COM output.

Note 2: The $\overline{RI/RBO}$ pin goes to low level only when the $\overline{RBI}$ pin is at a low level and all the digit are 0 (the display is blank).
If the $\overline{BI/RBO}$ pin is forcibly turned to high level, 0 at LSD is displayed.

Note 3: If the $\overline{BI/RBO}$ pin is forcibly turned to low level, the LSD is made blank.

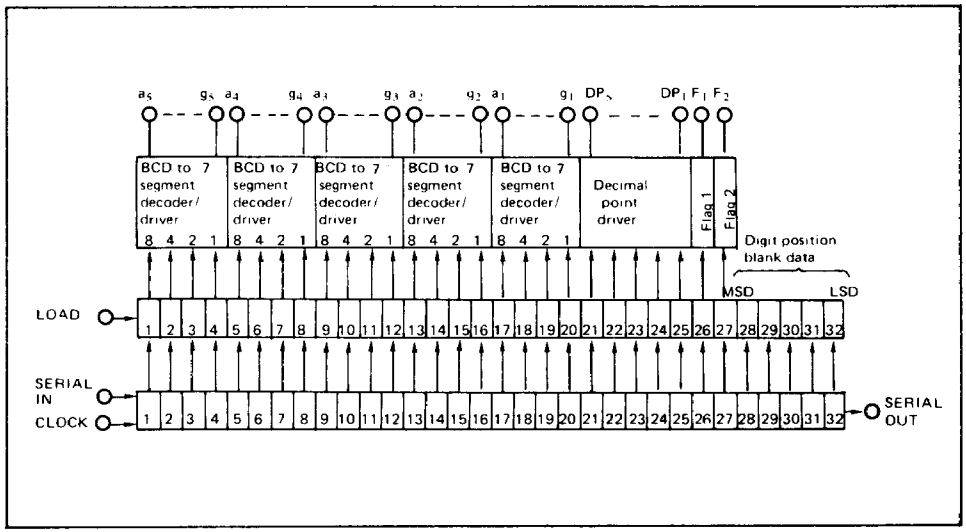
Note 4: If the $\overline{RBI}$ pin is turned to low level, the display is placed in the leading zero blanking status, in which the contiguous 0s preceding the MSD are made blank.

FUNCTIONAL DESCRIPTION

- **SERIAL IN**

  The SERIAL IN pin is a shift register data input pin. The display data are input to this pin synchronized with the clock pulses. The data are input in the order of blank data, flag data, decimal point data, then numeric data (beginning with the LSB) (positive logic).

< Data input procedure >



- **SERIAL OUT**

  The SERIAL OUT pin is a shift register serial output pin. The data input to the SERIAL IN pin is output from this pin synchronised with the clock pulses, with a delay of the total bit count of the shift register (32 bits). This pin is used for extension of digit display capacity.

- **CLOCK**

  The CLOCK pin is a synchronizing pulse input pin used for data input to the shift register or data output from the shift register. The data is shifted at the rising edge (low to high) of each clock pulse. A Schmitt trigger circuit is employed as the CLOCK input circuit (the hysteresis is approximately 0.5V).

- **LOAD**

  The LOAD pin is an input pin for latching the shift register contents. When this pin is at high level, the shift register contents are transferred to the decoders, and when this pin is at low level, the last data to be transferred from the shift register when this pin was at high level is held, so that the display contents are not changed with the change of the shift register contents.

- **$\overline{RBI}$**

  The $\overline{RBI}$ PIN is an input pin for suppressing the display of leading Os. When this pin is at high level, the leading Os, if any, are displayed; when this pin is at a low level, contiguous Os preceding the MSD are not displayed. The $\overline{RBI}$ pin is connected to the decoder circuit for the MSD.

  Note: The DP_1 through DP_5 are not made blank.

- **$\overline{BI}/\overline{RBO}$**

  The $\overline{BI}/\overline{RBO}$ pin is used for both input and output. As an input pin, the input level can forcibly be set to GND regardless of the output level, since the output resistance is treat.

  1 For use as an output pin $\overline{RBO}$

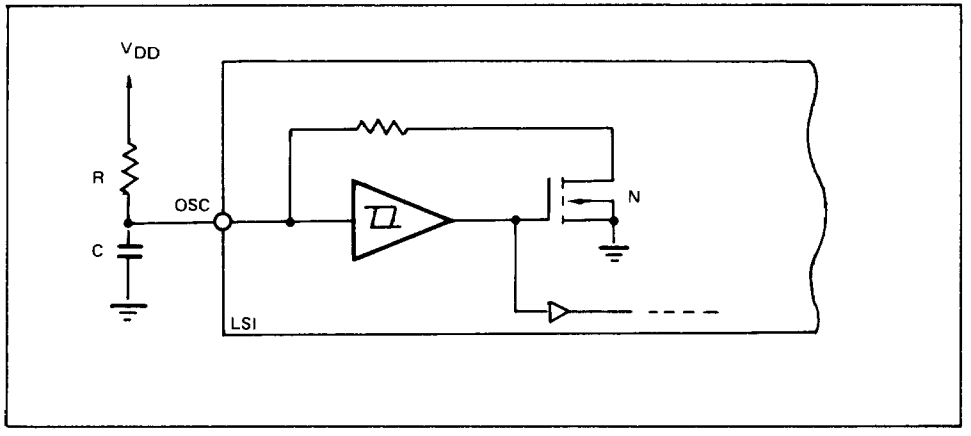
  When the $\overline{RBI}$ pin is turned to GND level, if all the digits are Os, the display is made blank and the $\overline{RBO}$ pin is turned to GND level. if the $\overline{RBI}$ pin is at VDD level or a number including some significant digits is displayed, the $\overline{RBO}$ pin is turned to VDD level. If two MSM58592BGS chips are connected for extension of the digit display capacity, the $\overline{RBO}$ pin of the first chip is connected to the $\overline{RBI}$ pin of the second chip, which connects to the MSD of the second chip, so that all the contiguous Os preceding the MSD are made blank.

2 For use as an input pin $\overline{BI}$
The $\overline{BI}$ pin is connected to the decoder circuit for the LSD. Therefore, if this pin is turned to GND level, only the LSD digit is made blank. Since this pin is also used as an output pin $\overline{ROB}$, some current indicated in the rating flows when this pin is set to GND level.
The $\overline{BI}$ pin may be open when not used.
Note: The DP_1 through DP_5 are not made blank.

- **SEGMENT OUT (a_1–g_5, DP_1–DP_5, F_1, F_2)**
The SEGMENT OUT pins are output pins for driving the seven segments of digits (a_1 – g_5), decimal points (DP_1–DP_5), and flags (F_1 and F_2) on the display device.
The seven segment outputs (a – g) for each digit are used to display a digit 0–9 or an alphabetic letter A – F.

- **OSC**
The OSC pin is an input pin for a signal generator circuit which outputs AC signals required for driving a LCD panel. The oscillator starts to generate AC signals only by connecting a resistor and a capacitor to the OSC pin as shown in the figure below.

$f_{(OSC)}$ = 360 Hz when the V_{DD} = 5V, C = 0.047μF, and R = 100kΩ



- **COM, $\overline{COM}$**
The COM pin is an output pin for sending an anti-phase signal of the seven segment outputs required for AC-driving the LCD panel. The COM output drives the COMMON pin on the LCD panel.
The $\overline{COM}$ pin is an output pin for sending an in-phase signal of the seven segment outputs (antiphase of the COM pin). This pin is not necessary in general display.
Both the COM and $\overline{COM}$ pins output square waves whose frequency is one eighth of the oscillator output appearing at the OSC pin (with a duty factor of 50%).

- **$\overline{OUTPUT\ DISABLE}$**
The $\overline{OUTPUT\ DISABLE}$ pin is an input pin for control of the COM pin. Setting this pin to high level places the COM pin in the normal status (the COM pin is used as an ordinary output pin), and setting this pin to low level makes the COM pin impedance high, so that the COM pin can be used as an input pin.
When two MSM58292BGS chips are interconnected in a cascade, the $\overline{OUTPUT\ DISABLE}$ pin of the second chip is set to low level and the COM pin is used as an input pin.

- **$\overline{\text{BLANK}}$**
  The $\overline{\text{BLANK}}$ pin is an input pin for making the display blank. Setting this pin to high level makes normal display, and setting this pin to low level makes the entire display blank.

- **Blanking a specific digit position**
  Any given digit position of the 5 digit display can be made blank by setting the MSM58292BGS to ON. A specific digit position can be made blank by setting a bit of the shift register bits 28-32, as shown in the table below.

Shift register bit setting	Digit position which is made blank
Set bit 28 to 1	Digit position with segments $a_5 - g_5$ (MSD)
Set bit 29 to 1	Digit position with segments $a_4 - g_4$
Set bit 30 to 1	Digit position with segments $a_3 - g_3$
Set bit 31 to 1	Digit position with segments $a_2 - g_2$
Set bit 32 to 1	Digit position with segments $a_1 - g_1$ (LSD)

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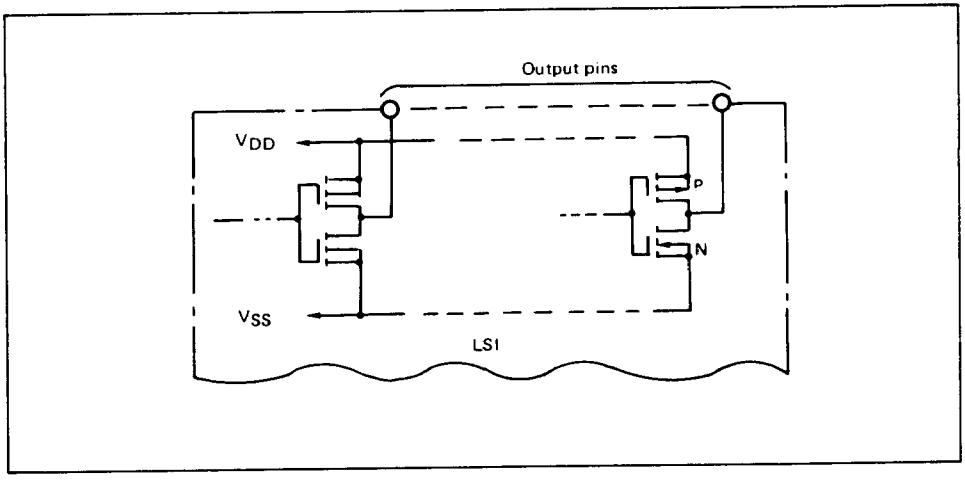
- **Decimal points**
  A digit position for which a decimal point has been specified is not subject to zero blanking even though that digit position contains the value 0. A decimal point can be used as a flag by setting the blank bit corresponding to that digit position to 1 to suppress the a – g segment display of that digit position (when the $\overline{\text{RBI}}$ pin is at low level).

- **Output circuit**
  Each output pin consists of a CMOS FET, and the $\overline{\text{BI}}/\overline{\text{RBO}}$ pin and SERIAL OUT pin output signals at high or low level.
  The output pins for display (for segments, decimal points, and flags) output pulse signals which are antiphase of the COM pin output when displaying, and output pulse signals which are in-phase of the COM pin output when not displaying. The output pins for display can directly drive the LCD panel.



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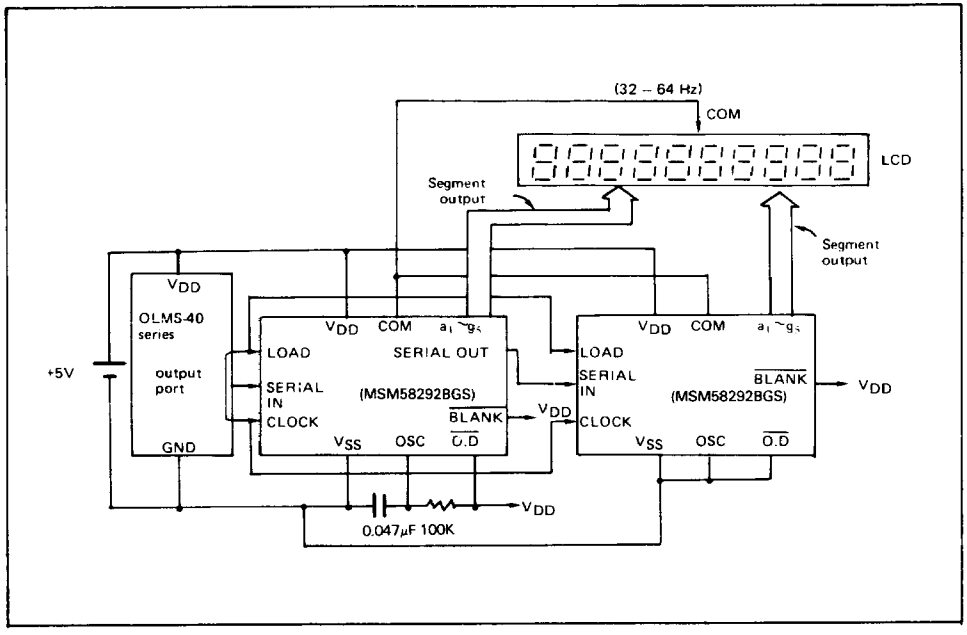
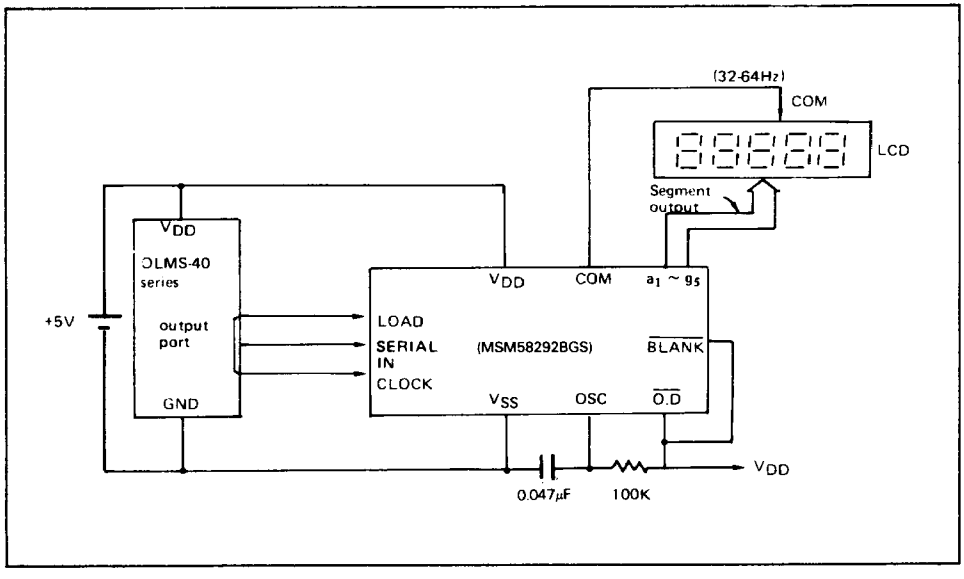
- **APPLICATIOIN CIRCUIT**

I. 10 digit display (using two MSM58292BGSs, cascade connection)



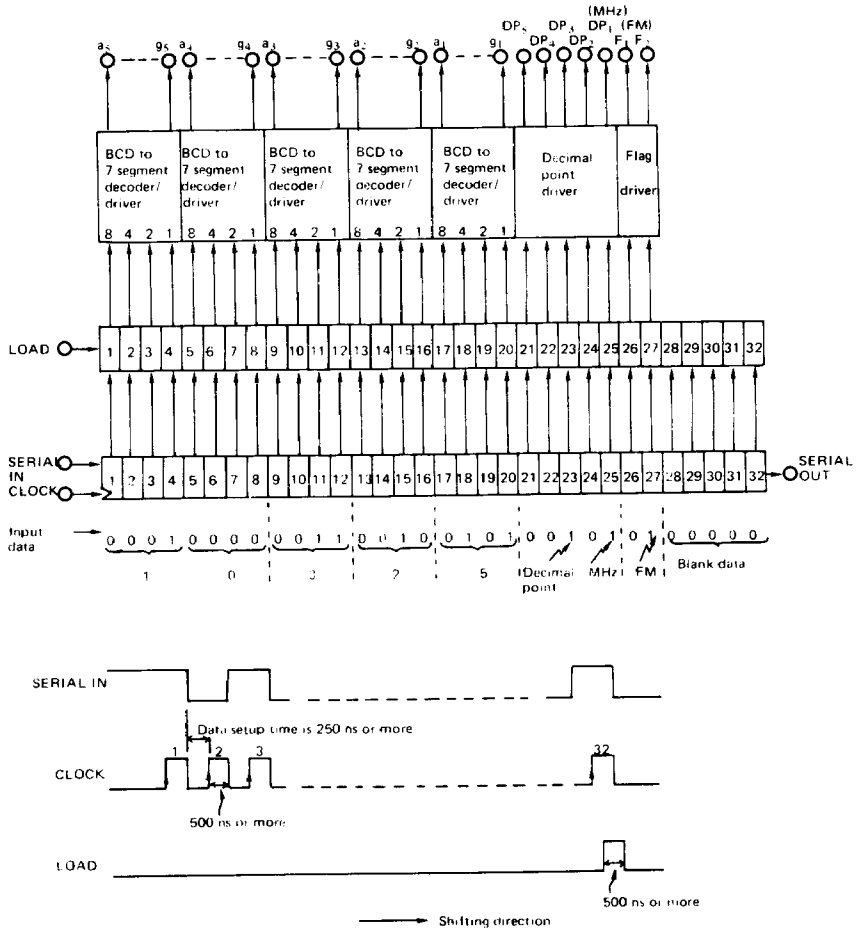
Note: $\overline{\text{O.D}}$ is the abbreviation of $\overline{\text{OUTPUT DISABLE}}$.

II. 5 digit display



Note: $\overline{\text{O.D}}$ the abbreviation of $\overline{\text{OUTPUT DISABLE}}$.

- **DATA INPUT EXAMPLE (FM 103.25 MHz)**



Example of interconnection with LCD