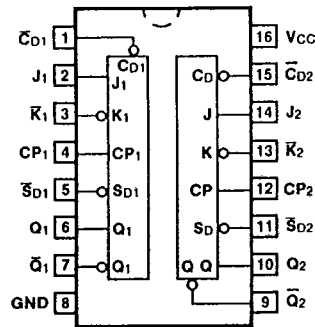


54S/74S109 54LS/74LS109

DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The '109 consists of two high speed, completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop (refer to '74 data sheet) by connecting the J and K inputs together. The '109 is functionally equivalent to the 9024.

CONNECTION DIAGRAM PINOUT A

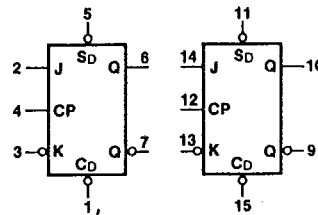


TRUTH TABLE		
INPUTS		OUTPUTS
@ t_n		@ t_{n+1}
J	K	Q Q
L	H	No Change
L	L	L H
H	H	H L
H	L	Toggles

Asynchronous Inputs:
 LOW input to \bar{S}_D sets Q to HIGH level
 LOW input to \bar{C}_D sets Q to LOW level
 Clear and Set are independent of clock
 Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH

t_n = Bit time before clock pulse.
 t_{n+1} = Bit time after clock pulse.
 H = HIGH Voltage Level
 L = LOW Voltage Level

LOGIC SYMBOL



VCC = Pin 16
 GND = Pin 8

ORDERING CODE: See Section 9

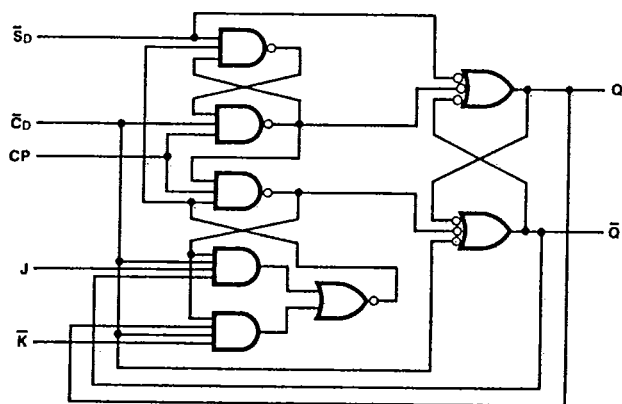
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	74S109PC, 74LS109PC		9A
Ceramic DIP (D)	A	74S109DC, 74LS109DC	54S109DM, 54LS109DM	6A
Flatpak (F)	A	74S109FC, 74LS109FC	54S109FM, 54LS109FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J ₁ , J ₂ , \bar{K}_1 , \bar{K}_2	Data Inputs	1.25/1.25	0.5/0.25
CP ₁ , CP ₂	Clock Pulse Inputs (Active Rising Edge)	2.5/2.5	1.0/0.5
\bar{C}_D1 , \bar{C}_D2	Direct Clear Inputs (Active LOW)	5.0/5.0	1.0/1.0
\bar{S}_D1 , \bar{S}_D2	Direct Set Inputs (Active LOW)	2.5/2.5	1.0/0.5
Q ₁ , Q ₂ , \bar{Q}_1 , \bar{Q}_2	Outputs	25/12.5	10/5.0 (2.5)

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LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I _{CC}	Power Supply Current	52		8.0		mA	V _{CC} = Max, V _{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		CL = 15 pF RL = 280 Ω		CL = 15 pF			
		Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	75		30		MHz	Figs. 3-1, 3-8
t _{PLH} t _{PHL}	Propagation Delay CP _n to Q _n or Q̄ _n	9.0 11		25 35		ns	Figs. 3-1, 3-8
t _{PLH} t _{PHL}	Propagation Delay C̄D _n or S̄D _n to Q _n or Q̄ _n	6.0 12		15 35		ns	V _{CP} ≥ 2.0 V Figs. 3-1, 3-10
t _{PLH} t _{PHL}	Propagation Delay C̄D _n or S̄D _n to Q _n or Q̄ _n	6.0 12		15 24		ns	V _{CP} ≤ 0.8 V Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t _s (H) t _s (L)	Setup Time J _n or K̄ _n to CP _n	6.0		18		ns	Fig. 3-6
t _h (H) t _h (L)	Hold Time J _n or K̄ _n to CP _n	0		0		ns	
t _w (H) t _w (L)	CP _n Pulse Width	7.0 6.5		20 13.5		ns	Fig. 3-8
t _w (L)	C̄D _n or S̄D _n Pulse Width LOW	6.0		15		ns	Fig. 3-10