

# Serial Quad I/O (SQI) Flash Memory

## SST26VF016 / SST26VF032



*The SST26VF016 / SST26VF032 Serial Quad I/O™ (SQI™) flash device utilizes a 4-bit multiplexed I/O serial interface to boost performance while maintaining the compact form factor of standard serial flash devices. Operating at frequencies reaching 80 MHz, the SST26VF016 / SST26VF032 enables minimum latency execute-in-place (XIP) capability without the need for code shadowing on an SRAM. The device's high performance and small footprint make it the ideal choice for mobile handsets, Bluetooth® headsets, optical disk drives, GPS applications and other portable electronic products. Further benefits are achieved with SST's proprietary, high-performance CMOS SuperFlash® technology, which significantly improves performance and reliability, and lowers power consumption for high bandwidth, compact designs.*

## Features

- **Single Voltage Read and Write Operations**

- 2.7-3.6V

- **Serial Interface Architecture**

- Nibble-wide multiplexed I/O's with SPI-like serial command structure

- Mode 0 and Mode 3

- Single-bit, SPI backwards compatible

- Read, High-Speed Read, and JEDEC ID Read

- **High Speed Clock Frequency**

- 80 MHz

- 320 Mbit/s sustained data rate

- **Burst Modes**

- Continuous linear burst

- 8/16/32/64 Byte linear burst with wrap-around

- **Index Jump**

- Jump to address index within 256 Byte Page

- Jump to address index within 64 KByte Block

- Jump to address index in another 64 KByte Block

- **Superior Reliability**

- Endurance: 100,000 cycles

- Greater than 100 years data retention

- **Low Power Consumption:**

- Active Read current: 12 mA (typical @ 80 MHz)

- Standby current: 8  $\mu$ A (typical)

- **Fast Erase and Byte-Program:**

- Chip-Erase time: 35 ms (typical)

- Sector-/Block-Erase time: 18 ms (typical)

- **Page-Program**

- 256 Bytes per page

- Fast Page Program time in 1 ms (typical)

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### **End-of-Write Detection**

– Software polling the BUSY bit in status register

#### **• Flexible Erase Capability**

- Uniform 4 KByte sectors
- Four 8 KByte top parameter overlay blocks
- Four 8 KByte bottom parameter overlay blocks
- Two 32 KByte overlay blocks (one each top and bottom)
- Uniform 64 KByte overlay blocks
- SST26VF016 – 30 blocks
- SST26VF032 – 62 blocks

#### **• Write-Suspend**

– Suspend program or Erase operation to access another block/sector

#### **• Software Reset (RST) mode**

#### **• Software Write Protection**

- Block-Locking
- 64 KByte blocks, two 32 KByte blocks, and eight 8 KByte parameter blocks

#### **• Security ID**

- One-Time Programmable (OTP) 256 bit, Secure ID
- 64 bit Unique, factory pre-programmed identifier
- 192 bit user-programmable

#### **• Temperature Range**

– Industrial: -40°C to +85°C

#### **• Packages Available**

- 8-contact WSON (6mm x 5mm)
- 8-lead SOIC (200 mil)

#### **• All devices are RoHS compliant**

## **Product Description**

The Serial Quad I/O™ (SQI™) family of flash-memory devices features a 4-bit, multiplexed I/O interface that allows for low-power, high-performance operation in a low pin-count package. System designs using SQI flash devices occupy less board space and ultimately lower system costs.

All members of the 26 Series, SQI family are manufactured with SST proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

The SST26VF016/032 significantly improve performance and reliability, while lowering power consumption. These devices write (Program or Erase) with a single power supply of 2.7-3.6V. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies.

SST26VF016/032 are offered in both 8-contact WSON (6 mm x 5 mm), and 8-lead SOIC (200 mil) packages. See Figure 2 for pin assignments.