

Control integrated Power System (CIPOS™)

Reconstruction of the CIPOS™
IKCS12F60AA Evaluation Board for
CIPOS™ IKCS12F60F2A

AN-Eval-IKCS12F60AA-3

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Never stop thinking

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1 Introduction

For users, who intend to use the original CIPOS™ IKCS12F60AA evaluation board to evaluate CIPOS™ IKCS12F60F2A, there are some necessary modifications to be done with the original evaluation board, because one pin of CIPOS™ IKCS12F60F2A is differently defined from IKCS12F60AA.

2 Difference between CIPOS™ IKCS12F60F2A and IKCS12F60AA

The major difference between CIPOS™ IKCS12F60F2A and IKCS12F60AA is the different definition of the pin 24 as shown in the Figure 1 below. The pin 24 of IKCS12F60AA is defined as EN for enable function. In case of any failure, microcontroller may disable the CIPOS™ through this pin. Another function of this pin is to read out the temperature near the gate driver IC. An internal divider is built to realize this function.

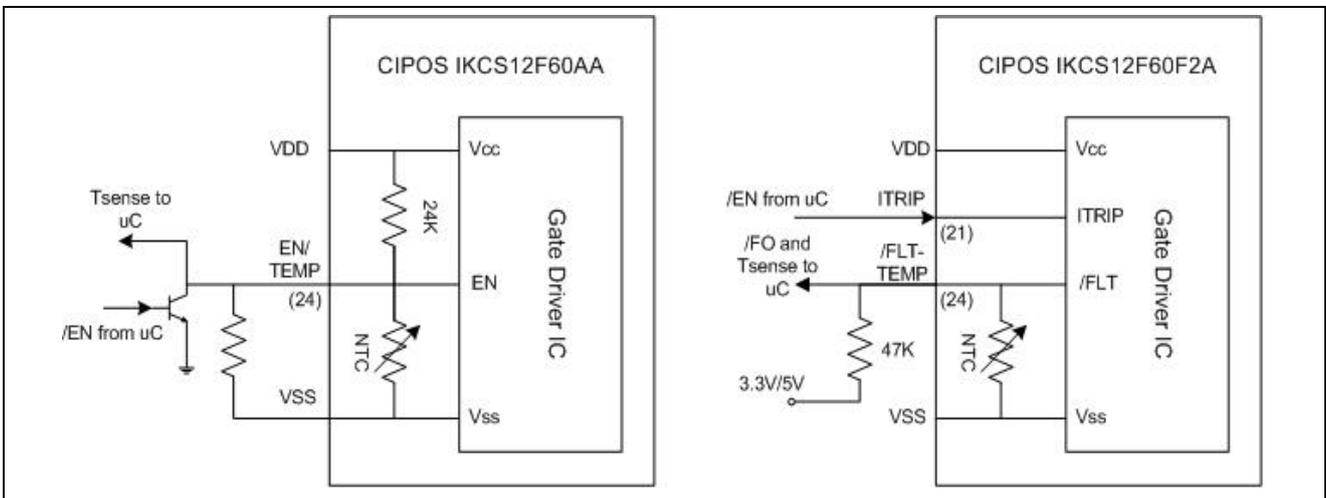


Figure 1: The different pin 24 definition between CIPOS™ IKCS12F60AA and IKCS12F60F2A

By contrast, the pin 24 of IKCS12F60F2A is defined as /FLT-TEMP, not only for the temperature monitoring, but also for indication of a fault signal from CIPOS internally. This pin is used normally for reading out the temperature near gate driver IC while the CIPOS™ works correctly. In case of any failure like UVLO or over-current, the pin is used as /FLT and will output a logic low level as a failure signal. Meanwhile, the temperature monitoring function is disabled. The advantage of adding the /FLT function to the pin 24 is to save an external comparator for generating the /FLT signal.

To disable the CIPOS™ in case of any failure, the pin of ITRIP (pin 21) must be used. Furthermore, an external pull up resistor (47KΩ recommended) to microcontroller power supply (+5V/3.3V) is needed to build up a divider.

3 Necessary Modifications on the Evaluation Board

The necessary modifications which must be done on the evaluation board are described as following:

Modification 1	For temperature monitoring function	<ul style="list-style-type: none"> • Cut off the original copper track from transistor T2 to the pin 24 to break the connection. (Step 1) • Connect pin 24 of IKCS12F60F2A with a wire directly to the a10 pin (Tsense) of the connector K3 (connection to microcontroller board). (Step 2) • Remove the resistor R35 (jumper, 0Ω). (Step 3)
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Modification 2	For disable function	<ul style="list-style-type: none"> Connect the pin 21(ITRIP) of IKCS12F60F2A with a wire directly to the b1 pin (/EN) of the connector K3. (Step 4)
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Note: The modifications on the demo board are just temporary to make an instant evaluation possible. In fact, the /FLT-TEMP pin of CIPOS™ IKCS12F60F2A is designed to save the expense of an external comparator for generating the fault signal for micro-controller. Thus, it is recommended for users to connect the /FLT-TEMP pin directly to both the /FO pin (b2) and Tsense pin (a10) of the connector K3. To disable the CIPOS, the shunt voltage signal will be directly sent to the ITRIP pin. This function demonstration will be realized in the next generation of the demo board.

And the modifications sketched on the layout are shown as following:

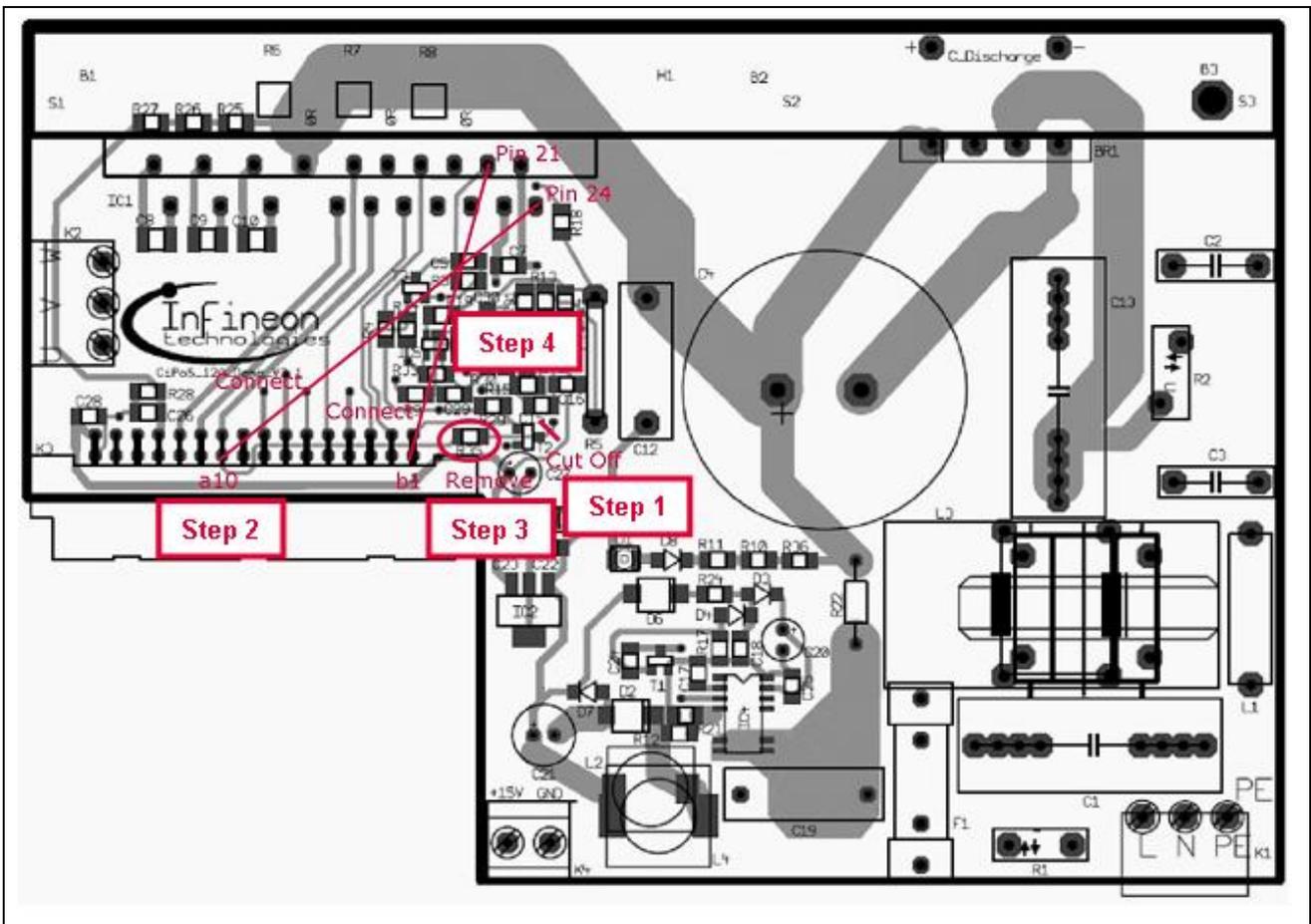


Figure 2: Necessary Modifications on the Layout of CIPOS™ IKCS12F60AA Demo Board

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