MAX16150

nanoPower Pushbutton On/Off Controller and Battery Freshness Seal

General Description

The MAX16150 is an extremely low-power, pushbutton, on/off controller with a switch debouncer and built-in latch. This device accepts a noisy input from a mechanical switch and produces a clean, latched output, as well as a one-shot interrupt output, in response to a switch closure exceeding the debounce period at $\overline{\text{PB\_IN}}$. A switch closure longer than shutdown period at $\overline{\text{PB\_IN}}$ results in a longer one-shot interrupt output. The MAX16150 family has two set of devices, one in which a longer switch closure greater than the shutdown period deasserts the latched output, and another in which the latched output stays asserted. See Table 1 for more information.

The MAX16150 operates from a supply range of +1.3V to +5.5V and consumes less than 20nA of supply current to ensure minimal battery drain in low-power applications, as well as to allow use as a battery "freshness seal". The robust switch input ($\overline{\text{PB\_IN}}$) accepts up to ±60V levels and is ±15kV ESD-protected for use in harsh environments. The latched output can serve as a logic signal to control a regulator, or it can serve as a switch to connect the load directly to the power supply when load current is low, providing 20mA of output current with less than 100mV voltage drop. A separate $\overline{\text{INT}}$ output provides a system interrupt whenever a valid pushbutton signal is detected. An asynchronous $\overline{\text{CLR}}$ input allows an external signal to force the latched output to the off state.

The MAX16150 operates over the -40°C to +125°C temperature range and is available in a 1mm x 1.5mm, 6-bump wafer-level package (WLP) and a 6-pin, thin SOT23 package.

Applications

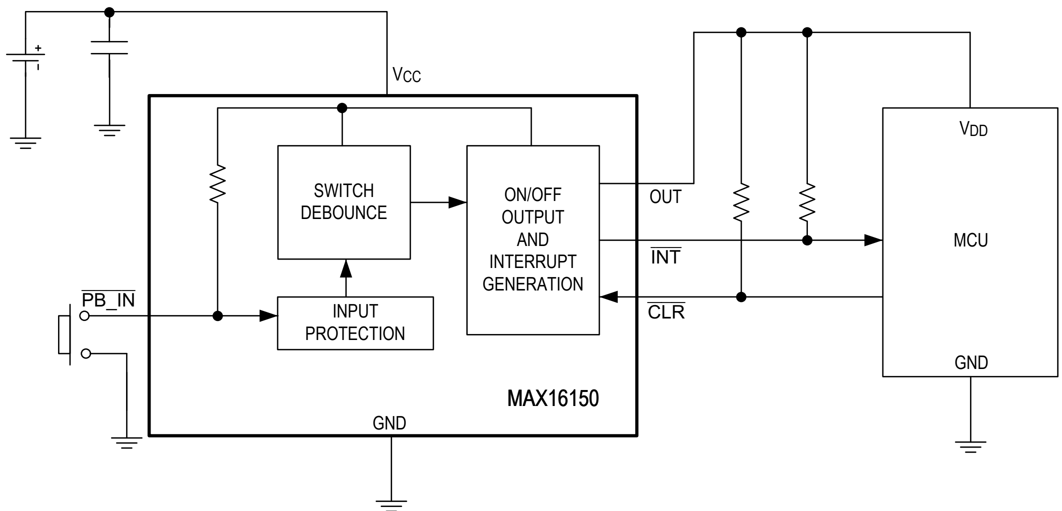
- Portable Instruments
- Handheld Consumer Electronics
- Industrial Equipment
- Disposable Low-Power Electronics

Benefits and Features

- Low Power
  - 20nA (max) Standby Current (ISB)
- Debounces Noisy Switches
  - 50ms and 2s Debounce Timing Options
  - 8s and 16s Shutdown Timing Periods
- Latched Output Supplies 20mA Load Current with Less Than 100mV Drop
- One-Shot $\overline{\text{INT}}$ Output on Each Switch Closure
- 8ms, 32ms, 64ms, and 128ms $\overline{\text{INT}}$ Timing Options
- Pushbutton Input Handles up to ±60V
- ±15kV HBM ESD Protection
- 6-pin SOT23 and 1mm x 1.5mm, 6-bump WLP

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit



SWITCH DEBOUNCER/FRESHNESS SEAL PROVIDING POWER DIRECTLY TO LOW-CURRENT LOAD

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Absolute Maximum Ratings

V_{CC} to GND .... -0.3V to +6V
PB_IN to GND .... -60V to +60V
$\overline{CLR}$, $\overline{INT}$, OUT to GND .... -0.3V to +6V
Continuous Power Dissipation (Multilayer Board)
6 SOT23 (T_A = +70°C, derate 8.70mW/°C above +70°C) 696mW
WLP (T_A = +70°C, derate 10.50mW/°C above +70°C) .840mW
Operating Temperature Range .... -40°C to +125°C
Junction Temperature .... +150°C
Storage Temperature Range .... -40°C to +150°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

6 SOT23

Package Code	U6+1
Outline Number	21-0058
Land Pattern Number	90-0175
Thermal Resistance, Single Layer Board:	
Junction to Ambient (θ_{JA})	N/A
Junction to Case (θ_{JC})	80°C/W
Thermal Resistance, Four Layer Board:	
Junction to Ambient (θ_{JA})	115°C/W
Junction to Case (θ_{JC})	80°C/W

6 WLP

Package Code	W60C1+2
Outline Number	21-100258
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	95.15°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{CC} = V_{MIN} to V_{MAX}, T_A = -40°C to +125°C, Limits over the operating temperature range and relevant supply voltage range are guaranteed by production and/or characterization. Typical values are at T_A = +25°C and V_{CC} = +3.3V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		1.3		5.5	V

Electrical Characteristics (continued)

(V_{CC} = V_{MIN} to V_{MAX}, T_A = -40°C to +125°C, Limits over the operating temperature range and relevant supply voltage range are guaranteed by production and/or characterization. Typical values are at T_A = +25°C and V_{CC} = +3.3V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{SB}	V_{CC} = 5V, OUT not asserted, $\overline{\text{PB\_IN}}$ not connected. -40°C ≤ T_A ≤ +70°C			20	nA
		V_{CC} = 5V, OUT not asserted, $\overline{\text{PB\_IN}}$ not connected. -40°C ≤ T_A ≤ +85°C		10	40	
	I_{CC}	During $\overline{\text{PB\_IN}}$ detection or $\overline{\text{INT}}$ assertion		15	30	µA
	I_{SB_UVLO}	V_{CC} < 1.3V, I_{OUT} = 0, $\overline{\text{PB\_IN}}$ not connected, $\overline{\text{CLR}}$ not asserted		2	5	uA
Timing Accuracy		Deviation from nominal value of debounce time (t_{DB}), shutoff time (t_{SO}), and interrupt time (t_{INT})	-20	±5	+20	%
Input High Voltage	V_{IH}	$\overline{\text{CLR}}$ and $\overline{\text{PB\_IN}}$, V_{CC} = 2.7V to 5.5V	70			$\%V_{CC}$
		$\overline{\text{CLR}}$ and $\overline{\text{PB\_IN}}$, V_{CC} = 1.3V to 2.7V	80			
Input Low Voltage	V_{IL}	$\overline{\text{CLR}}$ and $\overline{\text{PB\_IN}}$			30	$\%V_{CC}$
Minimum Input High Time Detected		PB_IN		600		µs
$\overline{\text{PB\_IN}}$ Hysteresis				100		mV
$\overline{\text{PB\_IN}}$ Pullup Resistance		0 < $V_{\overline{PB\_IN}}$ < V_{CC}	1200	1400	2000	kΩ
$\overline{\text{PB\_IN}}$ Input Current	I_{IN}	$V_{\overline{PB\_IN}}$ = ±60V	-170		+170	µA
$\overline{\text{PB\_IN}}$ Voltage Range		Continuous; 0V ≤ V_{CC} ≤ 5.0V	-60		+60	V
		Transient; 0V ≤ V_{CC} ≤ 5.5V	-60		+60	
$\overline{\text{CLR}}$ Input Current	I_{CLR}		-10	±1	+10	nA
$\overline{\text{CLR}}$ Falling Edge to OUT Low Propagation Delay	t_{CO}	R_L = 10kΩ, C_L = 100pF		200		ns
$\overline{\text{CLR}}$ Lockout Time		Period following rising edge of OUT during which transitions on $\overline{\text{CLR}}$ are ignored	1.6 x t_{INT}	2 x t_{INT}	2.4 x t_{INT}	ms
OUT Output Voltage	V_{OL}	V_{CC} = 3.3V, I_{SINK} = 1.6mA			0.4	V
		V_{CC} = 1.3V, I_{SINK} = 200µA			0.2	
	V_{OH}	V_{CC} = 3.3V, I_{SOURCE} = 20mA	V_{CC} - 0.1			
		V_{CC} = 2.0V, I_{OUT} = 2mA	V_{CC} - 0.02			
		V_{CC} = 1.3V, I_{SOURCE} = 500uA	V_{CC} - 0.02			
$\overline{\text{INT}}$ Output Voltage	V_{OL_INT}	V_{CC} = 3.3V, I_{SINK} = 1mA			0.2	V
		V_{CC} = 1.3V, I_{SINK} = 200µA			0.2	
$\overline{\text{INT}}$ Leakage Current			-10	±1	+10	nA
Interrupt Pulse Duration	t_{INT}	Beginning at t_{DB}	25.6	32	38.4	ms
		Beginning at the end of t_{SO}	102.4	128	153.6	

Electrical Characteristics (continued)

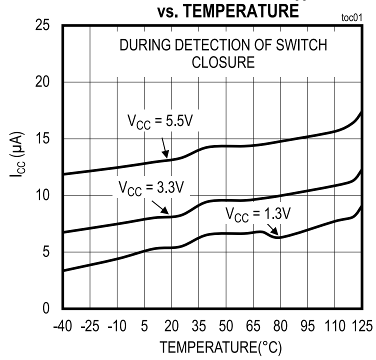
(V_{CC} = V_{MIN} to V_{MAX}, T_A = -40°C to +125°C, Limits over the operating temperature range and relevant supply voltage range are guaranteed by production and/or characterization. Typical values are at T_A = +25°C and V_{CC} = +3.3V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{PB\_IN}}$ ESD Protection		Human Body Model		±15		kV

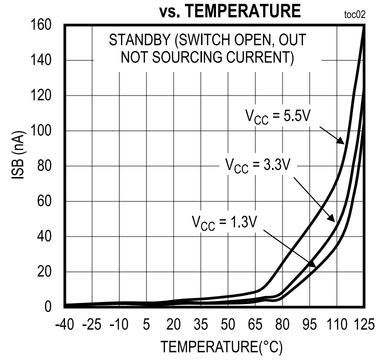
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

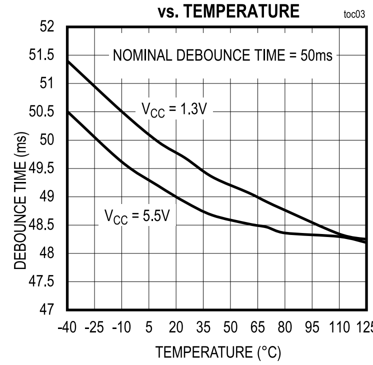
SUPPLY CURRENT(I_{CC}) vs. TEMPERATURE



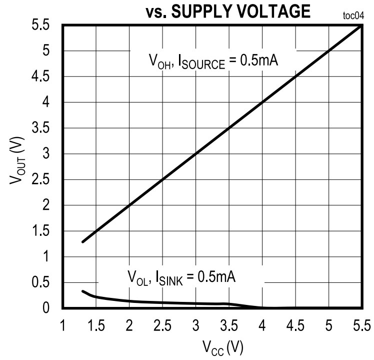
SUPPLY CURRENT (ISB) vs. TEMPERATURE



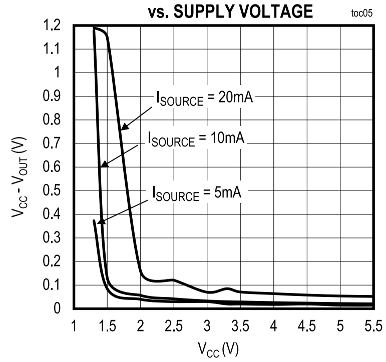
DEBOUNCE TIME vs. TEMPERATURE



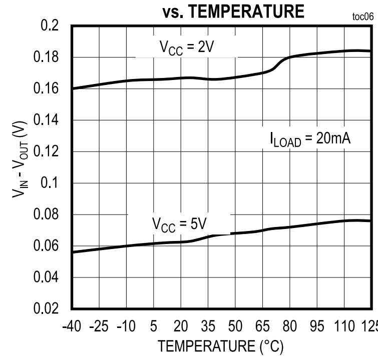
OUTPUT LOGIC LEVEL vs. SUPPLY VOLTAGE



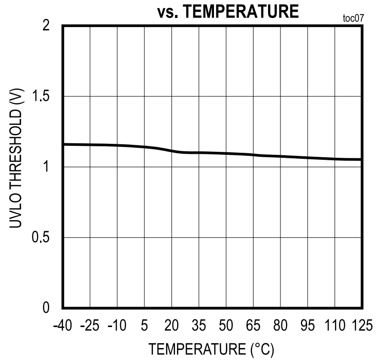
OUTPUT VOLTAGE DROP vs. SUPPLY VOLTAGE



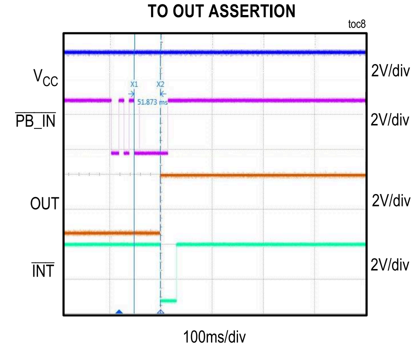
OUT VOLTAGE DROP vs. TEMPERATURE



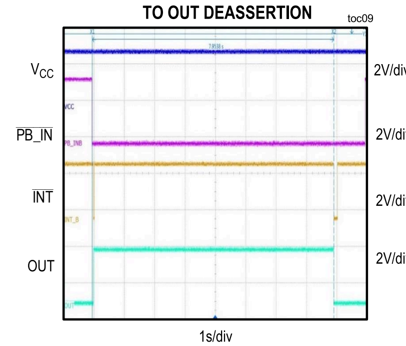
UVLO THRESHOLD vs. TEMPERATURE



MAX16150A SWITCH DEBOUNCE TO OUT ASSERTION

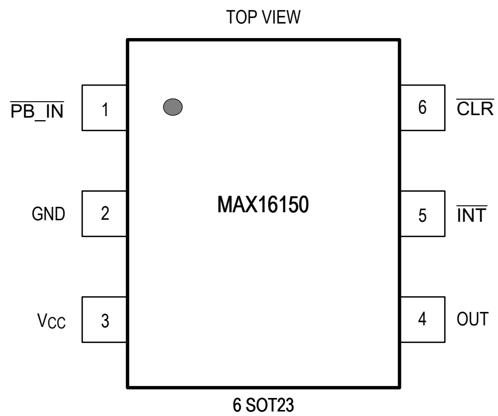


MAX16150 SWITCH DEBOUNCE TO OUT DEASSERTION

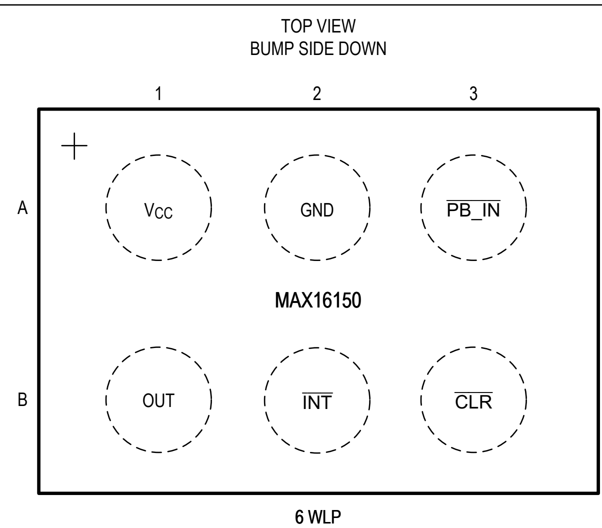


Pin Configurations

6 SOT23



6 WLP



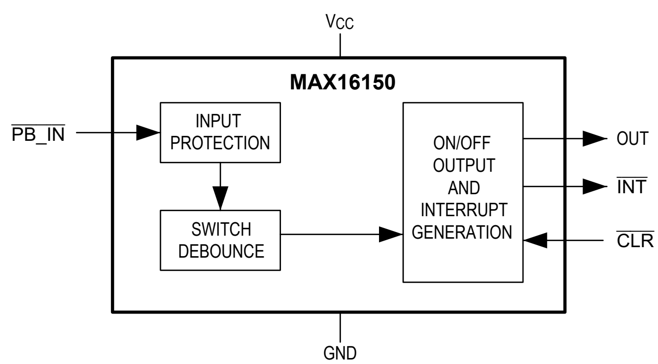
Pin Description

PIN		NAME	FUNCTION
6 SOT23	6 WLP		
1	A3	$\overline{\text{PB\_IN}}$	Pushbutton Input. $\overline{\text{PB\_IN}}$ is internally pulled up to V_{CC}. Holding $\overline{\text{PB\_IN}}$ low for a period greater than the debounce time (t_{DB}) forces OUT to latch high and generates a one-shot pulse at $\overline{\text{INT}}$. For the MAX16150, a $\overline{\text{PB\_IN}}$ switch closure longer than the shutdown period results in a longer one-shot pulse at INT. The MAX16150A deasserts the latched output when the switch closure period exceeds the shutdown period, while the MAX16150B/MAX16150C do not deassert the latched output.
2	A2	GND	Ground
3	A1	V_{CC}	Power Supply Input. Bypass with a 0.1μF capacitor to ground.

Pin Description (continued)

PIN		NAME	FUNCTION
6 SOT23	6 WLP		
4	B1	OUT	Active-High, Push-Pull Latched Output. OUT is connected to V_{CC} when high.
5	B2	$\overline{\text{INT}}$	Active-Low, Open-Drain Interrupt/Reset Output. $\overline{\text{INT}}$ is a one-shot output pulse. $\overline{\text{INT}}$ asserts for the interrupt timeout period when $\overline{\text{PB\_IN}}$ is held low for a period greater than the debounce time (t_{DB}). $\overline{\text{INT}}$ is high-impedance when deasserted, even when pulled above V_{CC}.
6	B3	$\overline{\text{CLR}}$	Clear Input. Pulling $\overline{\text{CLR}}$ low deasserts the latched OUT signal. If OUT is already deasserted when $\overline{\text{CLR}}$ is pulled low, the state of OUT is unchanged.

Block Diagram



Detailed Description

The MAX16150 is a pushbutton on/off controller with a switch debouncer and latched output for controlling system power. A switch closure that pulls $\overline{PB\_IN}$ low and is stable for a period greater than or equal to the debounce time (t_{DB}) causes OUT to assert high. Driving $\overline{CLR}$ low causes OUT to deassert. The MAX16150 family has two sets of devices: one in which a longer switch closure greater than the shutdown period deasserts the latched output, and another in which the latched output stays asserted. Each debounced switch closure also initiates a one-shot $\overline{INT}$ output. See Table 1 for details on the values of t_{DB}, t_{SO}, and other timing intervals.

Table 1. MAX16150 Input Timing Characteristics

VERSION*	DEBOUNCE TIME (t_{DB})	SHUTDOWN PERIOD (t_{SO})	INTERRUPT PERIOD (SWITCH CLOSURE > t_{DB})	INTERRUPT PERIOD (SWITCH CLOSURE > t_{SO})	SWITCH CLOSURE > t_{SO}
MAX16150A	50ms	8s	32ms	128ms	OUT deasserts
MAX16150B	2s	16s	32ms	128ms	OUT stays asserted
MAX16150C	50ms	16s	32ms	128ms	OUT stays asserted

*Versions with different combinations of timing parameters are available. Contact factory for availability.

Operation

The MAX16150 operates from supply voltages between +1.3V and +5.5V, consuming less than 20nA of supply current when OUT is in the deasserted state and $\overline{PB\_IN}$ is unconnected. Whenever OUT is deasserted, the state of $\overline{CLR}$ is ignored. After asserting OUT, $\overline{CLR}$ continues to be ignored for a period of 2x the $\overline{INT}$ period. For low-power applications (up to about 20mA output current), OUT can drive the load directly with minimal voltage drop. Each debounced switch closure causes $\overline{INT}$ to assert. A switch closure longer than t_{SO} results in $\overline{INT}$ asserting for a period that is 4x longer than the nominal $\overline{INT}$ period. This longer $\overline{INT}$ can be used to signal the system to perform a specific function, or to initiate a shutdown process. Closing the switch for a time longer than this extended $\overline{INT}$ period will not cause $\overline{INT}$ to be reasserted or the $\overline{INT}$ period to be extended.

The MAX16150 family has two sets of devices: one in which a longer switch closure greater than the shutdown period deasserts the latched output, and another in which the latched output stays asserted. A $\overline{PB\_IN}$ switch closure longer than the shutdown period results in a longer one-shot pulse at $\overline{INT}$.

Note that, when V_{CC} is first applied (for example, when the battery is initially installed), use either the $\overline{PB\_IN}$ or $\overline{CLR}$ input to set OUT to its initial state.

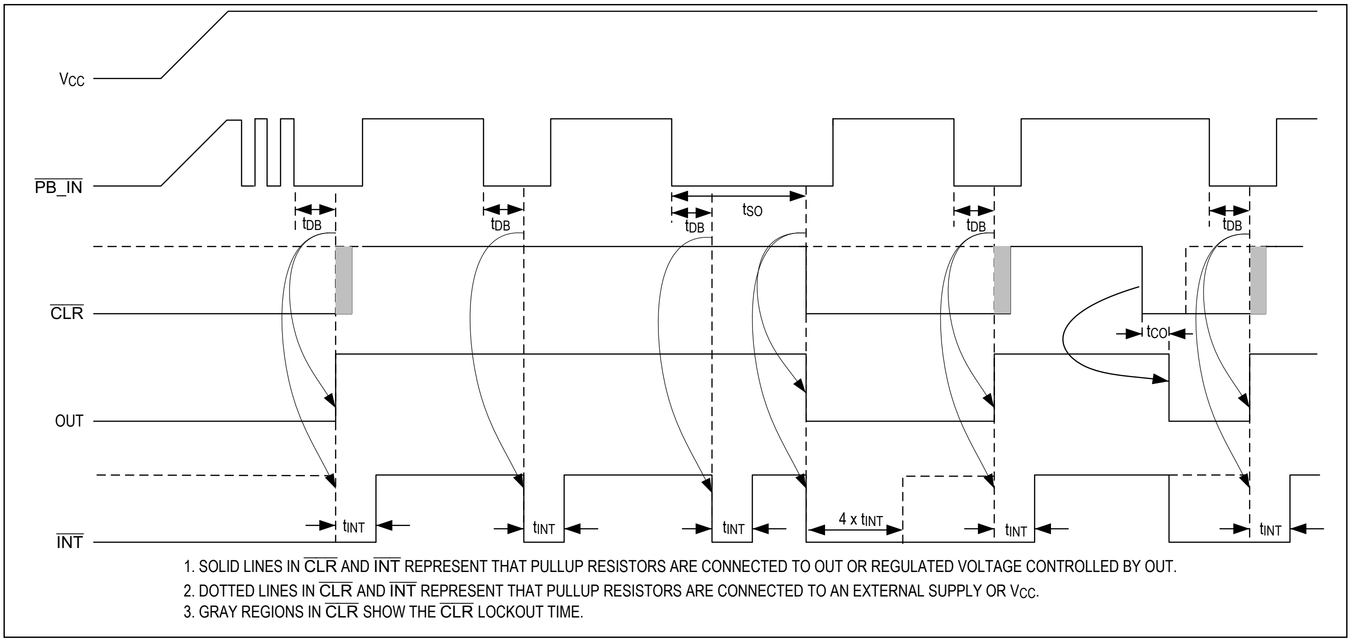


Figure 1. MAX16150 Timing Diagram with Long Pushbutton (t_{SO}) Causes Out to Deassert

Very brief high periods (less than approximately 600µs) at $\overline{\text{PB\_IN}}$ are ignored so that fast switch bounces do not interrupt the debounce logic, while valid short presses and releases cause the debouncer to reset. Figure 1 shows the timing diagram of the MAX16150A. A switch closure of a duration greater than t_{DB} causes OUT to assert. A switch closure of a duration greater than t_{SO} causes OUT to deassert and an extended interrupt at $\overline{\text{INT}}$. Typically, $\overline{\text{INT}}$ and $\overline{\text{CLR}}$ are pulled up either to OUT or to a regulated voltage controlled by OUT as depicted in Figure 1. As such, $\overline{\text{INT}}$ and $\overline{\text{CLR}}$ are pulled low while OUT is deasserted. If pulled up to a constant supply voltage, $\overline{\text{INT}}$ and $\overline{\text{CLR}}$ will behave as shown by the horizontal dashed lines while OUT is deasserted.

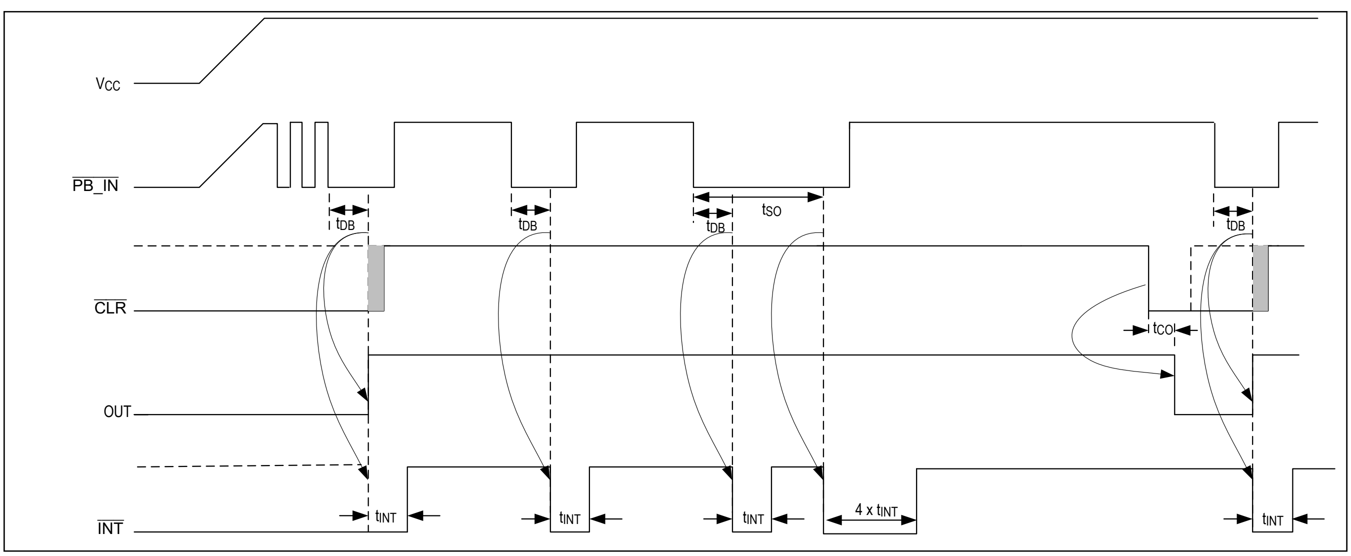


Figure 2. MAX16150 Timing Diagram with Long Pushbutton (t_{SO}) Keeps OUT Asserted

Figure 2 shows the timing diagram for the MAX16150B/MAX15150C. A switch closure of a duration greater than t_{DB}

causes OUT to assert. A switch closure of a duration greater than t_{SO} does not cause OUT to deassert, but it causes an extended interrupt. Typically, $\overline{INT}$ and $\overline{CLR}$ are pulled up either to OUT or to a regulated voltage controlled by OUT as depicted in Figure 2. As such, $\overline{INT}$ and $\overline{CLR}$ are pulled low while OUT is deasserted. If pulled up to a constant supply voltage, $\overline{INT}$ and $\overline{CLR}$ will behave as shown by the horizontal dashed lines while OUT is deasserted.

Robust Switch Input

The switch input ($\overline{PB\_IN}$) has overvoltage clamping diodes to protect against damaging fault conditions. Switch input voltages can safely swing ±60V relative to ground.

±15kV ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The MAX16150 has extra protection against static electricity to protect against ESD of ±15kV at the switch input without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. A design advantage of these devices is that they continue working without latchup after an ESD event, which eliminates the need to power-cycle the device. ESD protection can be tested in various ways; this product is characterized for protection to ±15kV using the Human Body Model.

Human Body Model

Figure 3 shows the Human Body Model, while Figure 4 shows the current waveform it generates when discharged into a low-impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

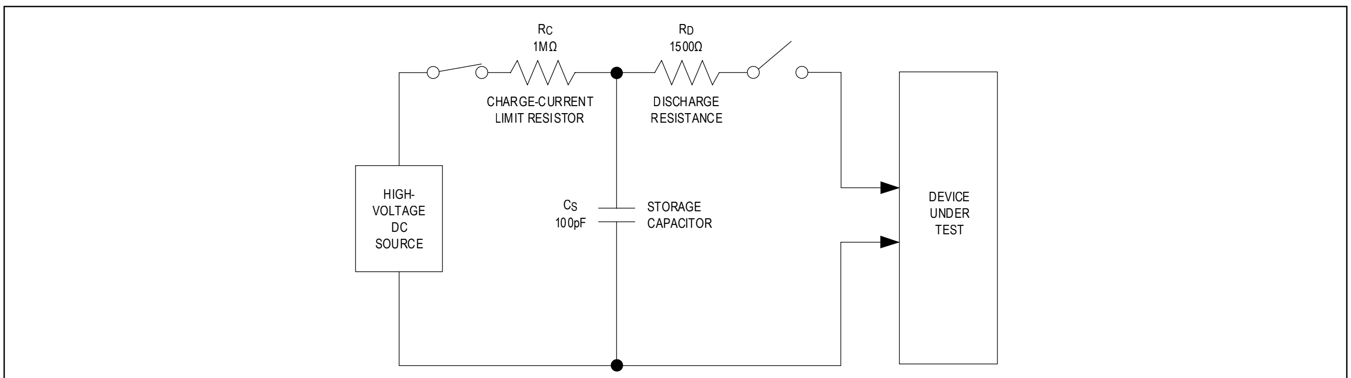


Figure 3. Human Body ESD Test Model

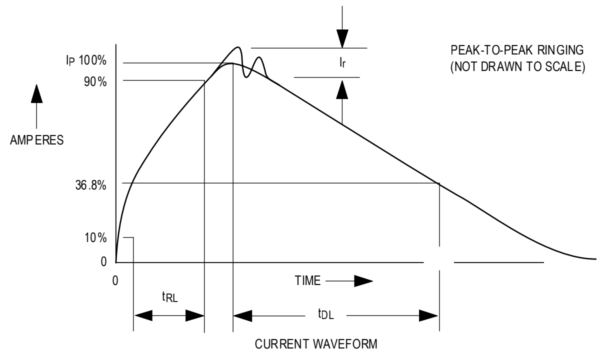


Figure 4. Human Body Current Waveform

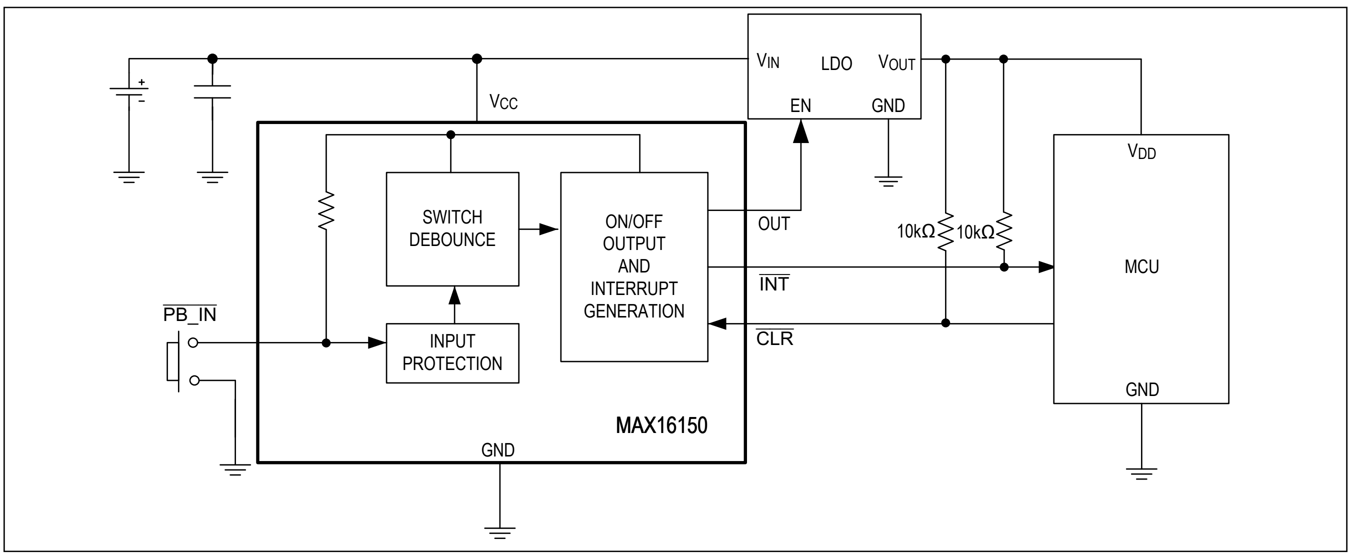
Applications Information

Powering the Load

OUT is capable of driving light loads. When the supply current of circuitry is less than about 20mA, the voltage drop from V_{CC} to OUT is less than 100mV. The *Typical Application Circuit*, located at the beginning of this document, shows OUT providing power directly to the load.

Some systems require higher power supply current than the output of the MAX16150 can provide. For those cases, OUT can be used as an enable signal for the voltage regulator powering the system. This *Typical Application Circuit* shows an LDO providing power to the load. The LDO's enable input is driven by OUT. A debounced pushbutton at $\overline{\text{PB\_IN}}$ of the MAX16150 causes OUT to assert high, thereby enabling the LDO.

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX16150AWT+T	-40ºC to +125°C	6 WLP
MAX16150AUT+T	-40ºC to +125°C	6 SOT23
MAX16150BWT+T	-40ºC to +125°C	6 WLP
MAX16150BUT+T	-40ºC to +125°C	6 SOT23
MAX16150CWT+T	-40ºC to +125°C	6 WLP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/19	Initial release	—
1	9/19	Updated *Ordering Information*	12
2	2/20	Updated *Ordering Information*	12
3	5/20	Updated *Benefits and Features*, *Typical Application Circuit*, *Electrical Characteristics* table, *Pin Configurations*, PB_IN Pin Description, *Block Diagram*, Table 1 note, Figure 1, and Figure 2	1, 2, 4, 7, 8, 9, 10, 11
4	1/21	Added MAX16150C, updated *Ordering Information*	8, 9, 10, 13