

## C<sup>2</sup>MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC40H192P/F TC40H193P/F

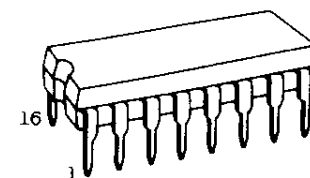
- TC40H192 SYNCHRONOUS BCD UP/DOWN COUNTER  
(DUAL CLOCK WITH CLEAR)  
TC40H193 SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER  
(DUAL CLOCK WITH CLEAR)

The TC40H192 and the TC40H193 are synchronous type 4-bit up/down counters.

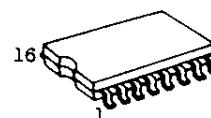
CLEAR input is active at "H" level, and PRESET input at "L" level, respectively. Both of them perform asynchronous operation.

The UP COUNT input and DOWN COUNT input of CLOCK are independent, and perform COUNT operation at the rising edge of pulse, respectively.

The TC40H192 and the TC40H193 are compatible in function and pin assignment with the TTL74192/74193.



DIP16 (3D16A-P)

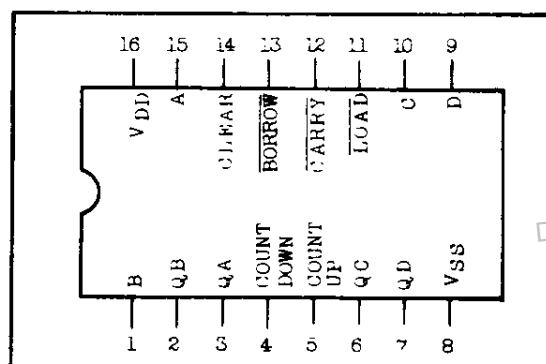


MFP16 (F16GC-P)

### MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	V <sub>SS</sub> -0.5 ~ V <sub>SS</sub> +10	V
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.5 ~ V <sub>DD</sub> +0.5	V
Output Voltage	V <sub>OUT</sub>	V <sub>SS</sub> -0.5 ~ V <sub>DD</sub> +0.5	V
Input Current	I <sub>IN</sub>	±10	mA
Power Dissipation	P <sub>D</sub>	300 (DIP) / 180 (MFP)	mW
Storage Temperature	T <sub>stg</sub>	-65 ~ 150	°C
Lead Temp./Time	T <sub>sol</sub>	260°C • 10 sec	

### PIN CONNECTION



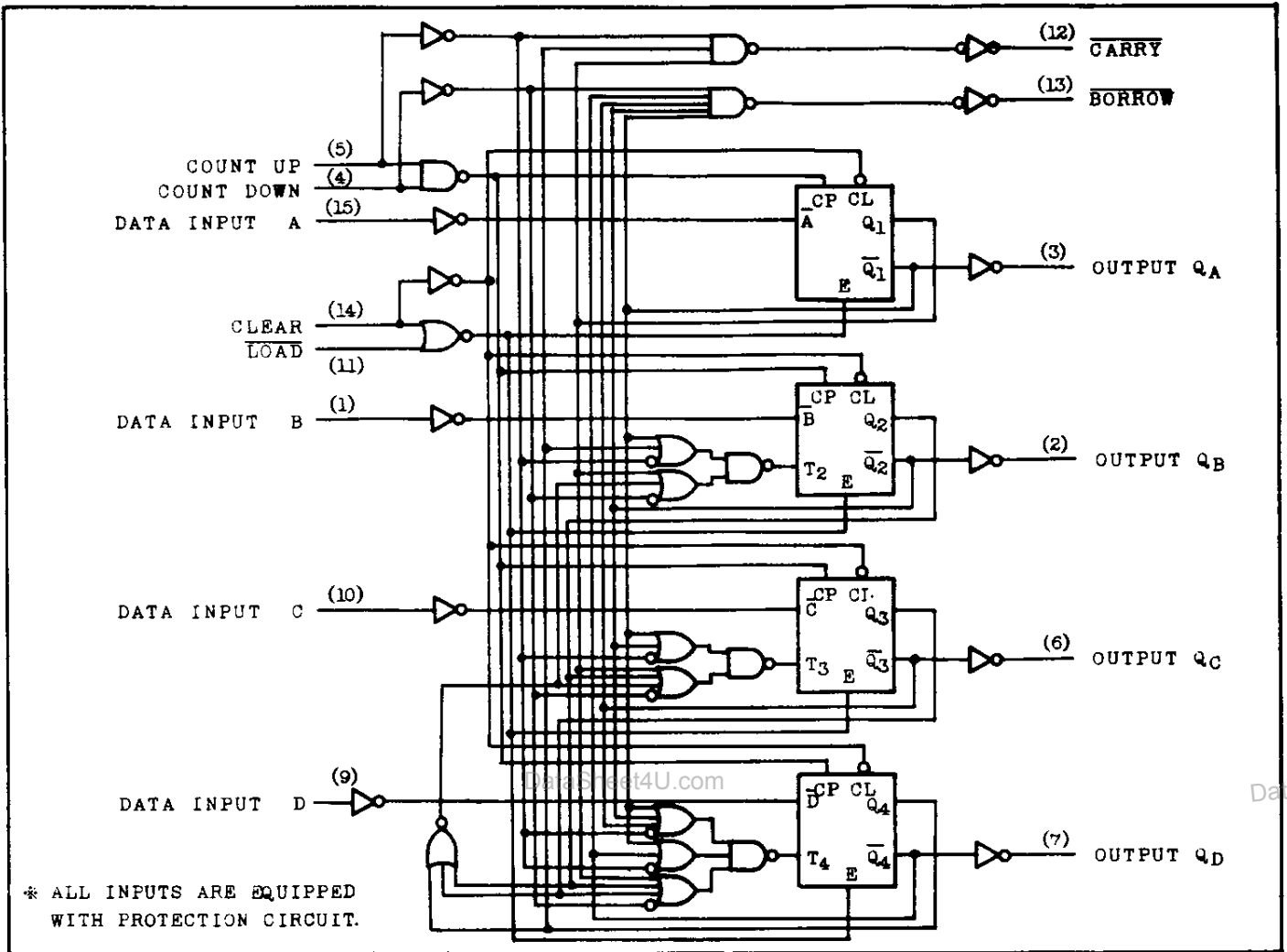
### TRUTH TABLE

TC40H192 / 193					TC40H192					TC40H193				
COUNT UP	COUNT DOWN	LOAD	CLEAR	ACTION	COUNT	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	COUNT	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
	H	H	L	COUNT UP	0	L	L	L	L	0	L	L	L	L
	H	H	L	NO COUNT	1	H	L	L	L	1	H	L	L	L
H		H	L	COUNT DOWN	2	L	H	L	L	2	L	H	L	L
H		H	L	NO COUNT	3	H	H	L	L	3	H	H	L	L
*	*	L	L	PRESET	4	L	L	H	L	4	L	L	H	L
*	*	*	H	RESET	5	H	L	H	L	5	H	L	H	L
					6	L	H	H	L	6	L	H	H	L
					7	H	H	H	L	7	H	H	H	L
					8	L	L	L	H	8	L	L	L	H
					9	H	L	L	H	9	H	L	L	H
					A	L	H	L	H	A	L	H	L	H
					B	H	H	L	H	B	H	H	L	H
					C	L	L	H	H	C	L	L	H	H
					D	H	L	H	H	D	H	L	H	H
					E	L	H	H	H	E	L	H	H	H
					F	H	H	H	H	F	H	H	H	H

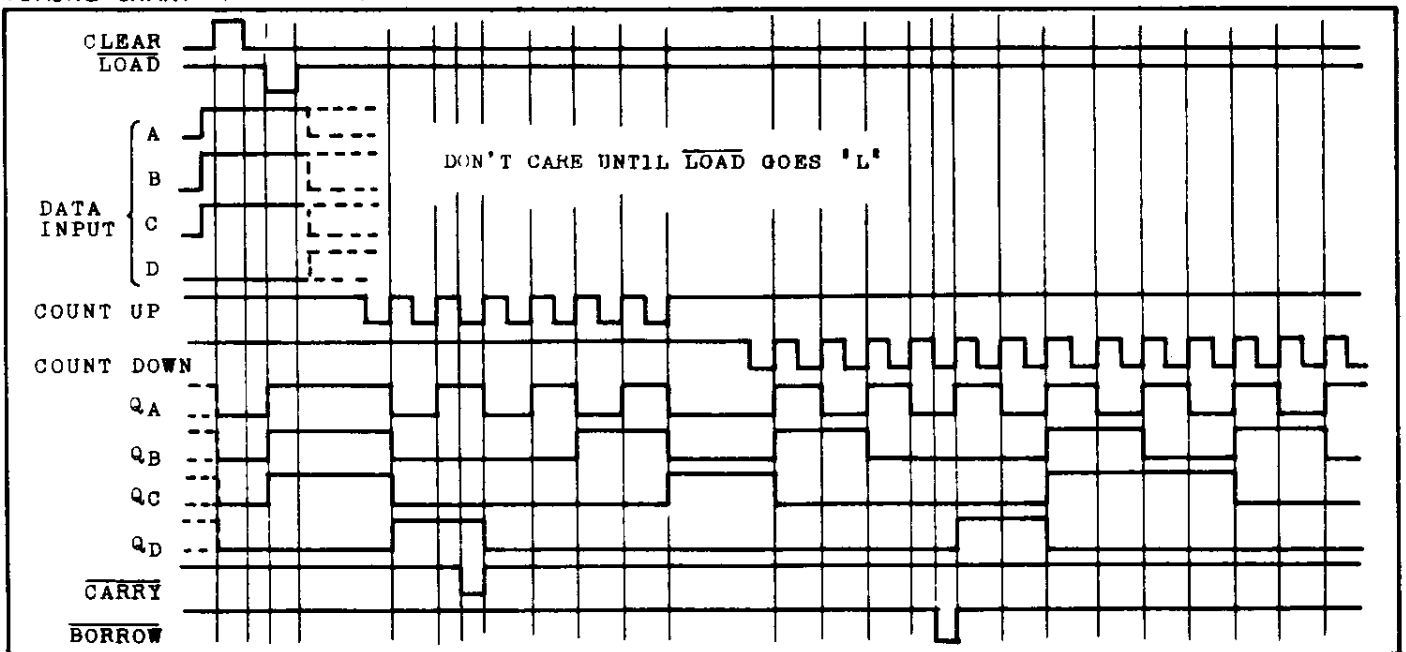
\* Don't care

# TC40H192P/F TC40H193P/F

LOGIC DIAGRAM (TC40H192)

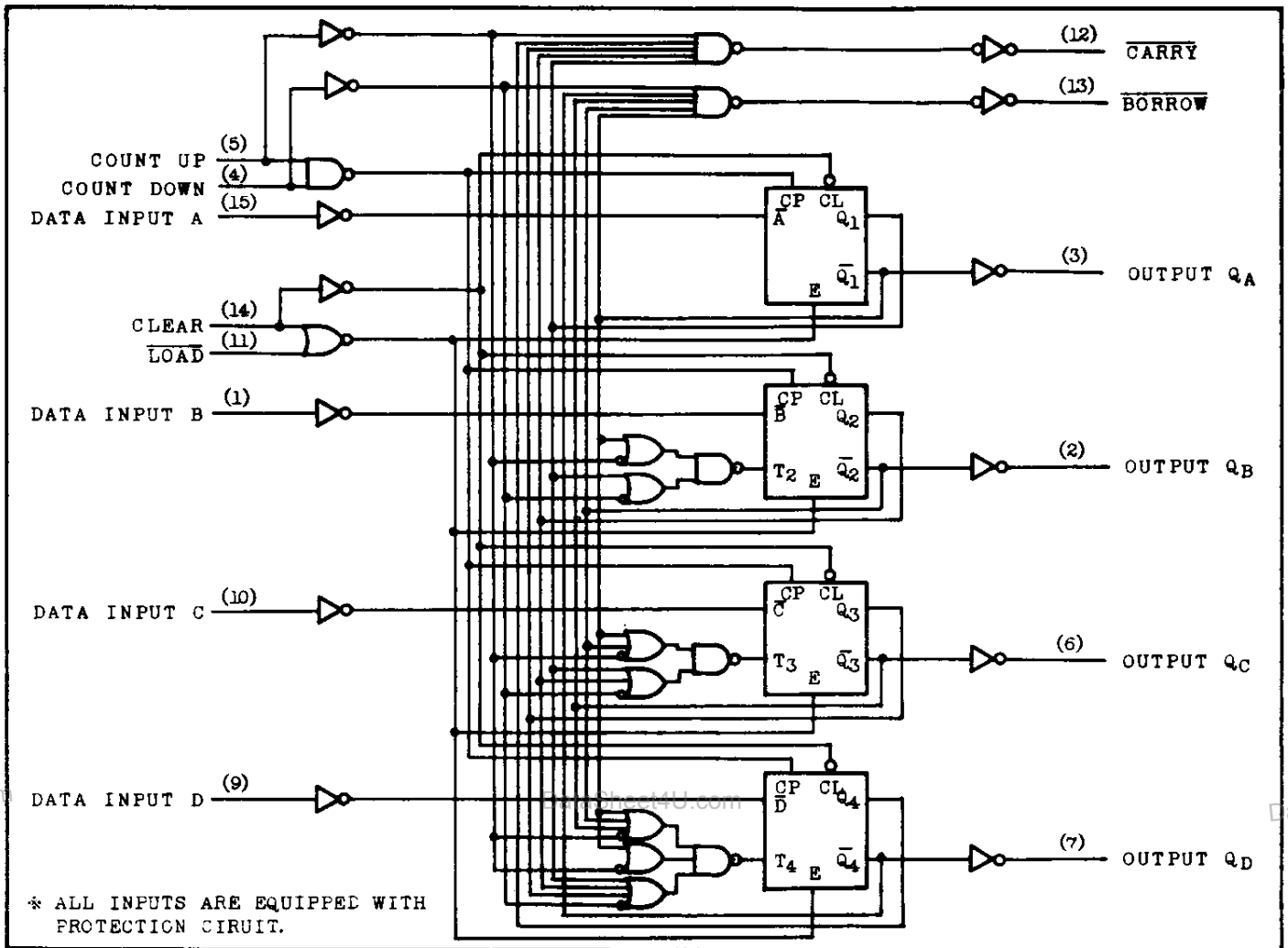


TIMING CHART (TC40H192)

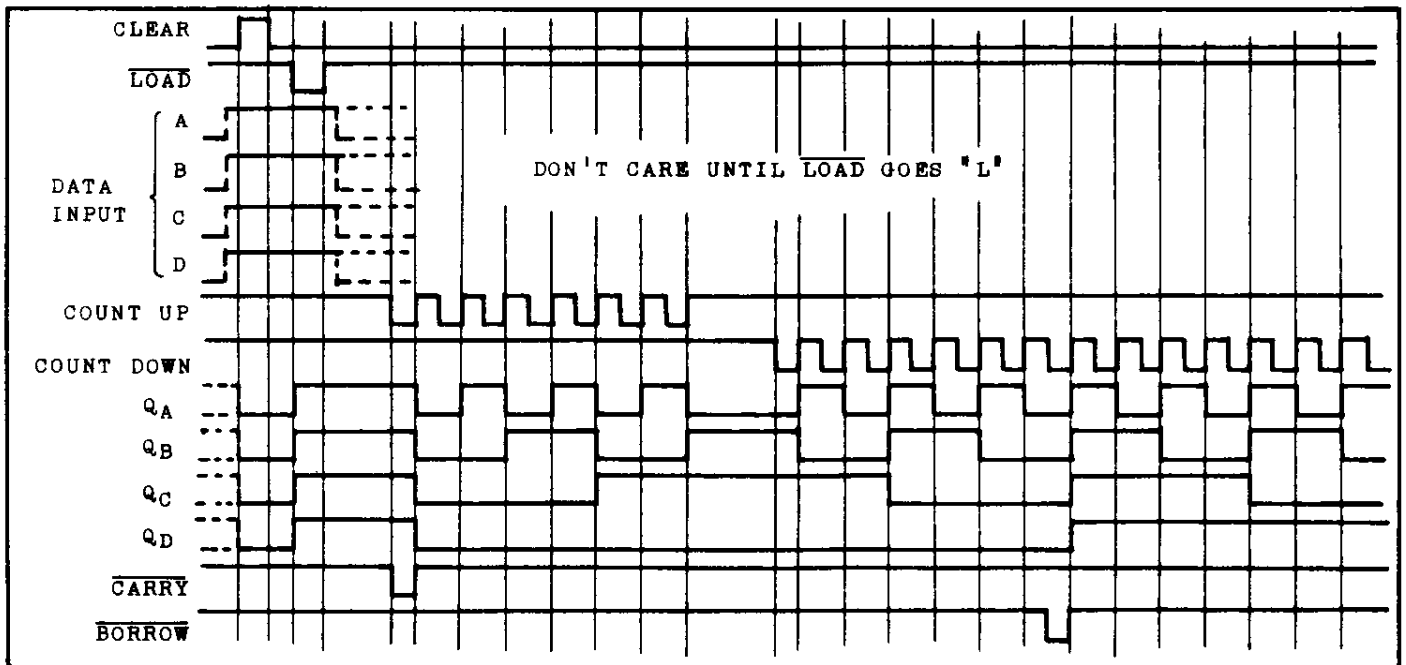


# TC40H192P/F TC40H193P/F

LOGIC DIAGRAM (TC40H193)



TIMING CHART (TC40H193)



# TC40H192P/F

# TC40H193P/F

## RECOMMENDED OPERATING CONDITIONS (V<sub>SS</sub>=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V <sub>DD</sub>	-	2	-	8	V
Input Voltage	V <sub>IN</sub>	-	0	-	V <sub>DD</sub>	V
Operating Temperature	T <sub>opr</sub>	-	-40	-	85	°C

## ELECTRICAL CHARACTERISTICS (V<sub>SS</sub>=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V <sub>DD</sub> (V)	-40°C		25°C			85°C		UNIT
				MIN.	TYP.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V <sub>OH</sub>	I <sub>OUT</sub>   < 1μA V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V <sub>OL</sub>	I <sub>OUT</sub>   < 1μA V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current	I <sub>OH</sub>	V <sub>OH</sub> =4.6V V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current	I <sub>OL</sub>	V <sub>OL</sub> =0.4V V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	1.4	-	1.1	-	-	0.8	-	mA
Input Voltage	"H" Level V <sub>IH</sub>	I <sub>OUT</sub>   < 1μA V <sub>OUT</sub> =0.5V	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level V <sub>IL</sub>	V <sub>OUT</sub> =4.5V	5	-	1.0	-	-	1.0	-	1.0	V
Input Current	"H" Level I <sub>IH</sub>	V <sub>IH</sub> =8.0V	8	-	0.3	-	10 <sup>-5</sup>	0.3	-	1.0	μA
	"L" Level I <sub>IL</sub>	V <sub>IL</sub> =0.0V	8	-	-0.3	-	-10 <sup>-5</sup>	-0.3	-	-1.0	μA
Quiescent Supply Current	I <sub>DD</sub>	*V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	-	12.5	-	0.005	12.5	-	75	μA

\* All valid input combinations.

## SWITCHING CHARACTERISTICS (T<sub>a</sub>=25°C, V<sub>SS</sub>=0.0V, V<sub>DD</sub>=5.0V, C<sub>L</sub>=15pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t <sub>or</sub>	-	-	22	40	ns
Output Fall Time	t <sub>of</sub>		-	16	30	
Propagation Delay Time	t <sub>pLH</sub>	CLOCK - Q	-	80	135	ns
	t <sub>pHL</sub>		-	55	90	
Propagation Delay Time	t <sub>pLH</sub> , t <sub>pHL</sub>	CLOCK - $\overline{\text{CARRY BORROW}}$	-	45	83	ns
	t <sub>pLH</sub> , t <sub>pHL</sub>	$\overline{\text{LOAD}}$ - $\overline{\text{CARRY BORROW}}$	-	90	150	
	t <sub>pLH</sub> , t <sub>pHL</sub>	LOAD - Q	-	75	135	
	t <sub>pHL</sub>	CLEAR - Q	-	70	105	
	t <sub>pLH</sub> , t <sub>pHL</sub>	CLEAR - $\overline{\text{CARRY BORROW}}$	-	90	150	
Data Hold Time	t <sub>hold</sub>	$\overline{\text{LOAD}}$ - DATA	-	0	10	ns
Data Setup Time	t <sub>setup</sub>	$\overline{\text{LOAD}}$ - DATA	-	8	20	ns
Min. Clear Removal Time	t <sub>rem</sub>	CLEAR - CLOCK	-	33	50	ns
Min. Load Removal Time	t <sub>rem</sub>	$\overline{\text{LOAD}}$ - CLOCK	-	53	80	ns

# TC40H192P/F TC40H193P/F

## SWITCHING CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Min. Preset Width of Pulse	$t_w$	LOAD	-	38	70	ns
Min. Clear Width of Pulse	$t_w$	CLEAR	-	30	53	ns
Max. Clock Rise Time	$t_{r\phi}$	-	1.0	50	-	$\mu$ s
Max. Clock Fall Time	$t_{f\phi}$	-	-	-	-	-
Max. Clock Frequency	$f_{MAX}$	-	5	10	-	MHz
Input Capacitance	$C_{IN}$	-	-	5	-	pF

## SWITCHING TIME TEST CIRCUIT WAVEFORM

### TEST CIRCUIT

TEST NO.	CLEAR	LOAD	COUNT UP	COUNT DOWN	DATA n
1	L	H	PG1	H	L
1	L	H	H	PG1	L
2	L	PG1	L	L	PG2
3	PG1	PG2	L	L	H

### WAVEFORM 1

TEST No. 1

### WAVEFORM 2

TEST No. 2

### WAVEFORM 3

TEST No. 3

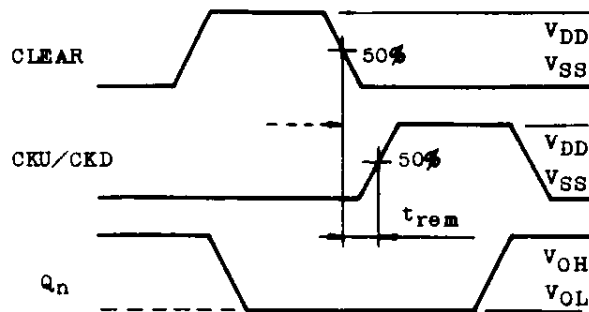
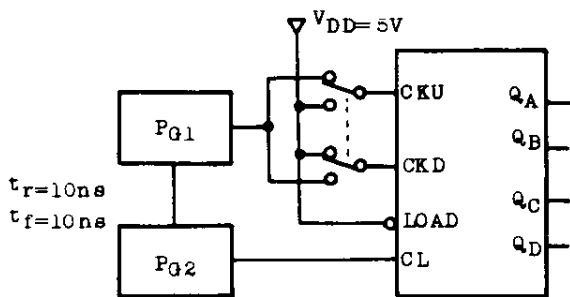
### WAVEFORM 4

TEST No. 4

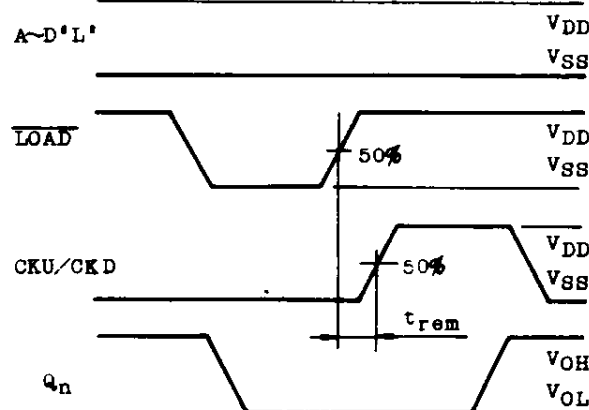
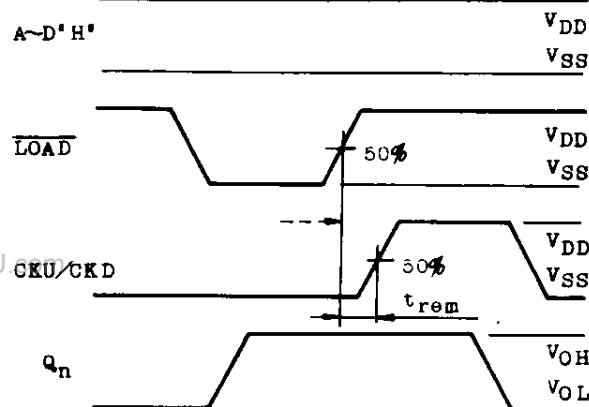
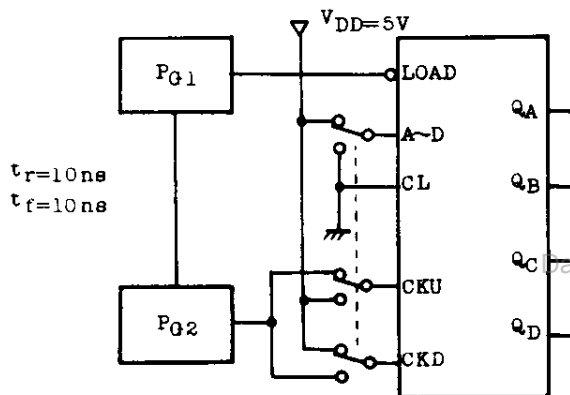
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## SWITCHING TIME TEST CIRCUIT & WAVEFORM

Minimum Clear Removal Time Test Circuit

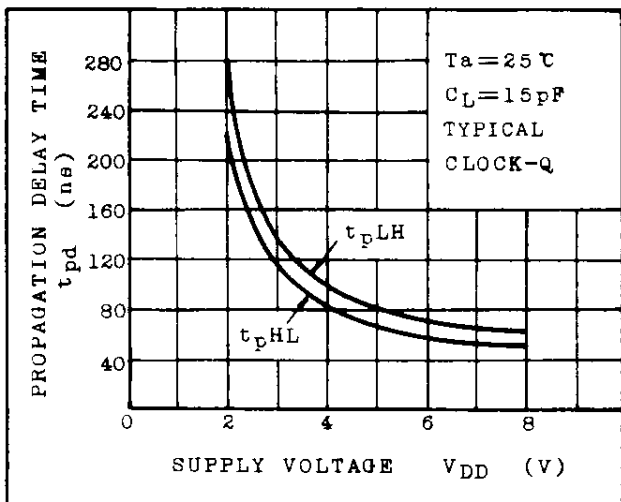


Minimum Load Removal Time Test Circuit

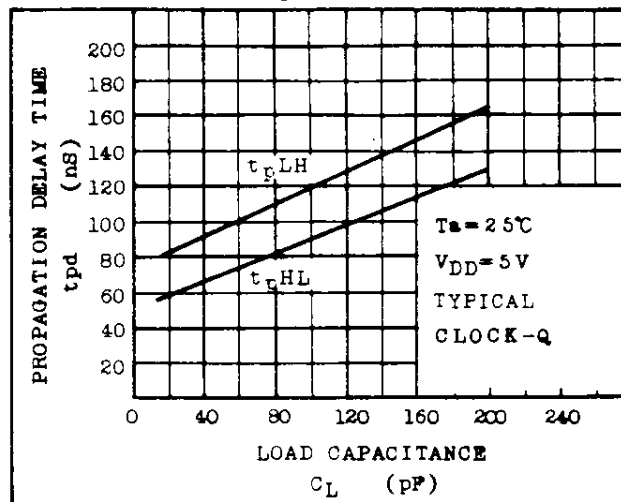


# TC40H192P/F TC40H193P/F

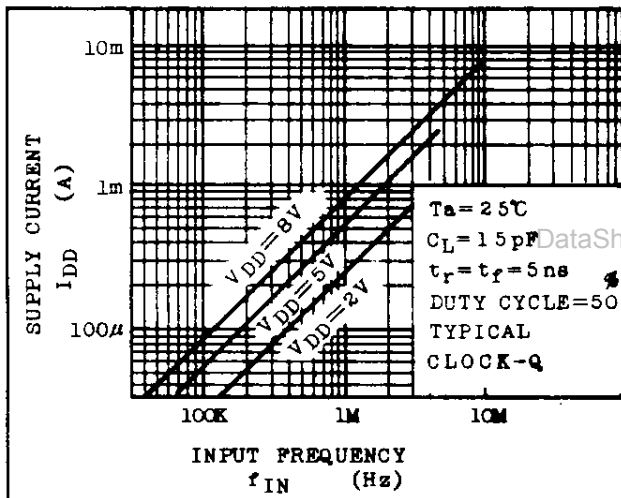
$t_{pd} - V_{DD}$



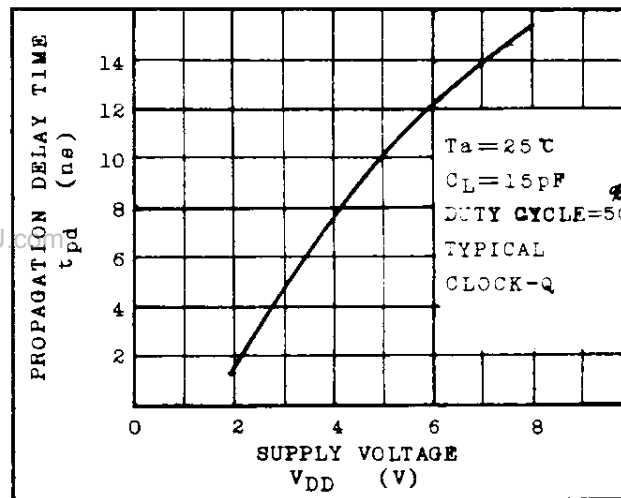
$t_{pd} - C_L$



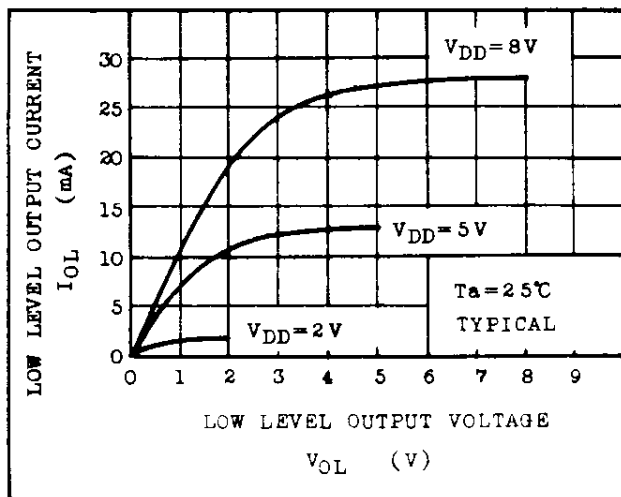
$I_{DD} - f_{IN}$



$t_{pd} - V_{DD}$



$I_{OL} - V_{OL}$



$I_{OH} - (V_{DD} - V_{OH})$

