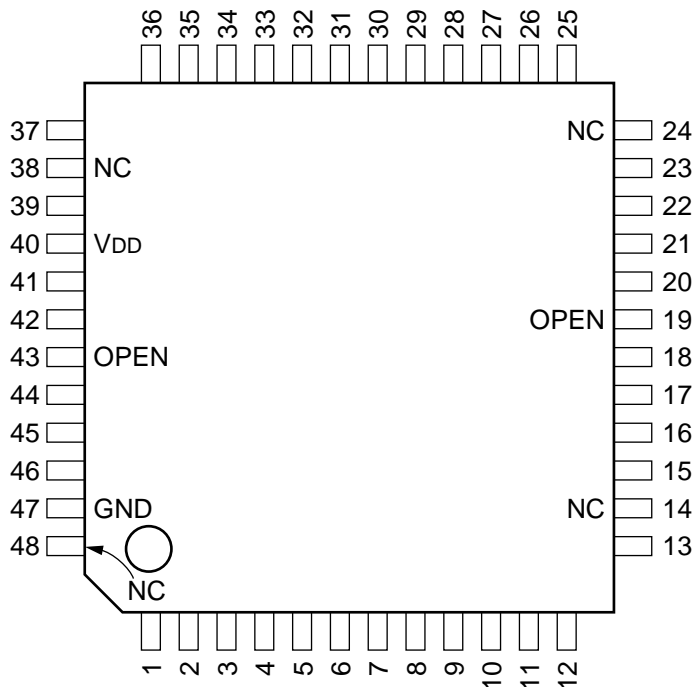


## C-MOS DUAL SERIAL DATA TRANSMITTER / RECEIVER UNIT

—TOP VIEW—



NC ; NON CONNECT TERMINAL (OPEN)

OPEN ; NEVER CONNECT TERMINAL

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I/O	DB4	17	O	TRNRDY2	33	I	CLOCK
2	I/O	DB5	18	I/O	SYNC/BRK2	34	I	RST
3	I/O	DB6	19	—	OPEN	35	I	DSR1
4	I/O	DB7	20	I	CTS2	36	O	RTS1
5	I	TRNCLK1	21	O	TRNEMP2/ST1-2	37	I	DTR1
6	I	W	22	O	TRNDT2	38	—	NC
7	I	CS1	23	O	DSR2	39	I	RCVCLK1
8	I	RSLCT0	24	—	NC	40	—	VDD
9	I	R	25	O	RTS2	41	I/O	DB0
10	O	RCVRDY1	26	O	DTR2	42	I/O	DB1
11	I	RSLCT1	27	I	RCVCLK2	43	—	OPEN
12	I	CS2	28	O	TRNRDY1	44	I/O	DB2
13	I	RCVDT2	29	I/O	SYNC/BRK1	45	I/O	DB3
14	—	NC	30	I	CTS1	46	I	RCVDT1
15	I	TRNCLK2	31	O	TRNEMP1/ST1-1	47	—	GND
16	O	RCVRDY2	32	O	TRNDT1	48	—	NC

**INPUT**

CLOCK ; CLOCK (4,9152 MHz) FOR REFERENCE OF TIMING  
 CSn ; CHIP SELECT OF CHANNELn. (n = 1 OR 2)  
 CTSn ; CLEAR TO SEND OF CHANNELn. (n = 1 OR 2)  
 DSRn ; DATA SET READY OF CHANNELn. (n = 1 OR 2)  
 R ; READ ENABLE  
 RCVCLKn ; RECEIVER CLOCK OF CHANNELn. (n = 1 OR 2)  
 RCVDn ; RECEIVE DATA OF CHANNELn. (n = 1 OR 2)  
 RSLCTn ; REGISTERS SELECT LINEn. (n = 0 AND 1)  
 RST ; RESET PULSE  
 TRNCLKn ; TRANSMITTER CLOCK OF CHANNELn. (n = 1 OR 2)  
 W ; WRITE ENABLE

**OUTPUT**

DTRn ; DATA TERMINAL READY OF CHANNELn. (n = 1 OR 2)  
 RCVRDYn ; RECEIVER READY OF CHANNELn. (n = 1 OR 2)  
 RTSn ; REQUEST TO SEND OF CHANNELn. (n = 1 OR 2)  
 TRNDn ; TRANSMIT DATA OF CHANNELn. (n = 1 OR 2)  
 TRNEMPn/ST1-n ; TRANSMITTER EMPTY / BAUD RATE CLOCK OUT  
 OF CHANNELn. (n = 1 OR 2)  
 TRNRDYn ; TRANSMIT READY OF CHANNELn. (n = 1 OR 2)

**INPUT/OUTPUT**

DBn ; DATA BUS LINEn. (n = 0 TO 7)  
 SYNC/BRKn ; SYNCHRONIZATION CHARACTER / BREAK CODE DETECT  
 OF CHANNELn. (n = 1 OR 2)  
 NC ; NON CONNECT TERMINAL (OPEN)  
 OPEN ; NEVER CONNECT TERMINAL

