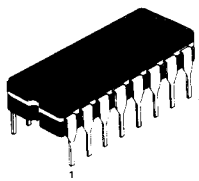
COMBO CODECS

The KT8554 and KT8557 are single-chip PCM encoders and decoders (PCM CODECs) and PCM line filters. These devices provide all the functions required to interface a full-duplex voice telephone circuit with a time-division-multiplexed (TDM) system.
These devices are designed to perform the transmit encoding and receive decoding as well as the transmit and receive filtering functions in PCM system. They are intended to be used at the analog termination of a PCM line or trunk.
These devices provide the bandpass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signaling and supervision information.

16 CERDIP



FEATURES

- **Complete CODEC and filtering system**
- **Meets or exceeds AT&T D3/D4 and CCITT specifications**
  μ-Law: KT8554, A-Law: KT8557
- **On-chip auto zero, sample and hold, and precision voltage references**
- **Low power dissipation: 60mW (operating)**
  3mW (standby)
- **±5V operation**
- **TTL or CMOS compatible**
- **Automatic power down**

ORDERING INFORMATION

Device	Package	Operating Temperature
†KT8554N	Plastic	−25~+125°C
†KT8557N	Plastic	
KT8554J	Ceramic	
KT8557J	Ceramic	

† Under Development

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BLOCK DIAGRAMS

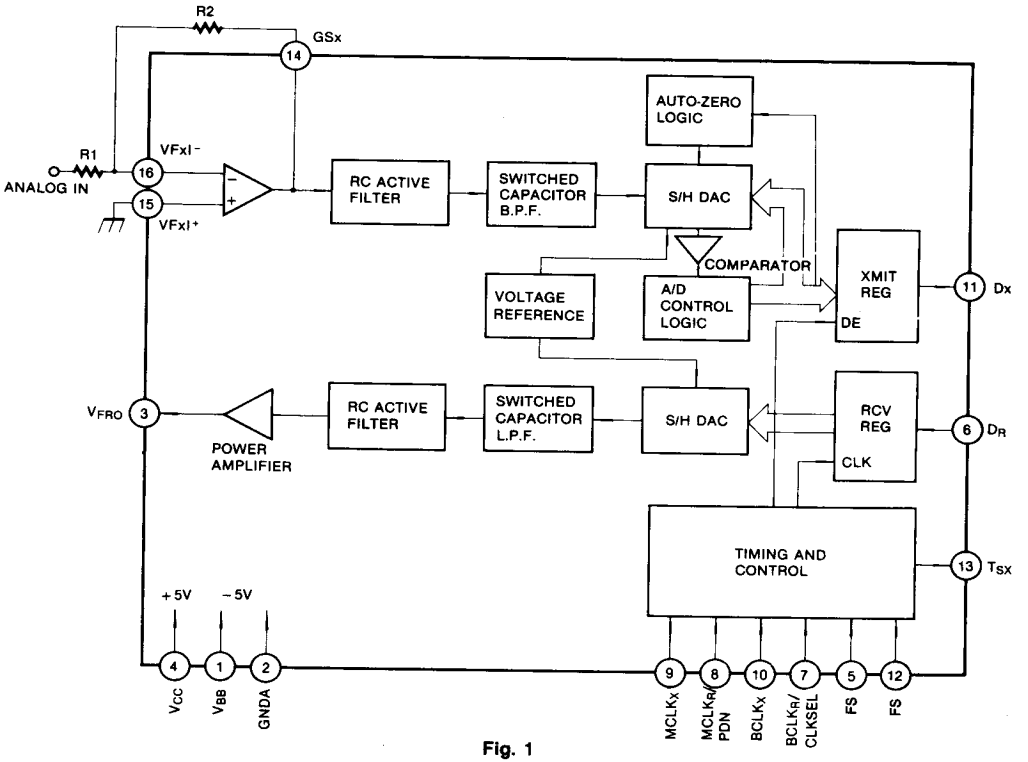

Fig. 1

ABSOLUTE MAXIMUM RATINGS

Characteristic.	Symbol	Value	Unit
V_{CC} to GNDA	V_{CC}	7	V
V_{BB} to GNDA	V_{BB}	−7	V
Voltage at Any Analog Input or Output	AI/O	$V_{CC}+0.3$ to $V_{BB}-0.3$	V
Voltage at Any Digital Input or Output	DI/O	$V_{CC}+0.3$ to GNDA − 0.3	V
Operating Temperature Range	Ta	−25 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (Soldering, 10 secs)	T_L	300	°C

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ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, GNDA = 0V, Ta = 0°C to 70°C; typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, Ta = 25°C; all signals referenced to GNDA.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Power Dissipation						
Power-Down Current	$I_{CC}0$	No Load		0.5	1.5	mA
Power-Down Current	$I_{BB}0$	No Load		0.05	0.3	mA
Active Current	$I_{CC}1$	No Load		6.0	9.0	mA
Active Current	$I_{BB}1$	No Load		6.0	9.0	mA
Digital Interface						
Input Low Voltage	V_{IL}				0.6	V
Input High Voltage	V_{IH}		2.2			V
Input Low Current	I_{IL}	$GNDA \leq V_{IN} \leq V_{IL}$, all digital inputs	−10		10	μA
Input High Current	I_{IH}	$V_{IH} \leq V_{IN} \leq V_{CC}$	−10		10	μA
Output Low Voltage	V_{OL}	D_X, $I_L = 3.2mA$ SIG_R, $I_L = 1.0mA$ $\overline{TS}_X$, $I_L = 3.2mA$, open drain			0.4 0.4 0.4	V V V
Output High Voltage	V_{OH}	D_X, $I_H = -3.2mA$ SIG_R, $I_H = -1.0mA$	2.4 2.4			V V
Output Current in High Impedance State (TRI-STATE)	I_{OZ}	D_X, $GNDA \leq V_O \leq V_{CC}$	−10		10	μA
Analog Interface with Receive Filter						
Output Resistance	R_ORF	Pin VF_RO		1	3	Ω
Load Resistance	R_LRF	$VF_RO = \pm 2.5V$	600			Ω
Load Capacitance	C_LRF				500	pF
Output DC Offset Voltage	VOS_RO		−200		200	mV
Analog Interface with Transmit Input Amplifier						
Input Leakage Current	I_IXA	$-2.5V \leq V \leq +2.5V$, VF_XI+ or VF_XI-	−200		200	nA
Input Resistance	R_IXA	$-2.5V \leq V \leq +2.5V$, VF_XI+ or VF_XI-	10			MΩ
Output Resistance	R_OXA	Closed loop, unity gain		1	3	Ω
Load Resistance	R_LXA	GS_X	10			KΩ
Load Capacitance	C_LXA	GS_X			50	pF
Output Dynamic Range	V_OXA	GS_X, $R_L \leq 10K\Omega$	±2.8			V
Voltage Gain	A_VXA	VF_XI+ to GS_X	5,000			V/V
Unity Gain Bandwidth	F_UXA		1	2		MHz
Offset Voltage	$V_{OS}XA$		−20		20	mV
Common-Mode Voltage	$V_{CM}XA$	CMRRXA > 60dB	−2.5		2.5	V
Common-Mode Rejection Ratio	CMRRXA	DC Test	60			dB
Power Supply Rejection Ratio	PSRRXA	DC Test	60			dB

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TIMING CHARACTERISTICS

(Unless otherwise noted, $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, GNDA = 0V, Ta = 0°C to 70°C; typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, Ta = 25°C; all signals referenced to GNDA.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency of Master Clocks	$1/t_{PM}$	Depends on the device used and the $BCLK_R$/CLKSEL Pin. $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
Rise Time of Bit Clock	t_{RB}	$t_{PB} = 488ns$			50	ns
Fall Time of Bit Clock	t_{FB}	$t_{PB} = 488ns$			50	ns
Holding Time from Bit Clock Low to Frame Sync	t_{HBFL}	Long frame only	0			ns
Holding Time from Bit Clock High to Frame Sync	t_{HOLD}	Short frame only	0			ns
Set-Up Time from Frame Sync to Bit Clock Low	t_{SFB}	Long frame only	80			ns
Delay Time from $BCLK_X$ High to Data Valid	t_{DBD}	Load = 150pF plus 2 LSTTL loads	0		180	ns
Delay Time to $\overline{TS_X}$ Low	t_{XDP}	Load = 150pF plus 2 LSTTL loads			140	ns
Delay Time from $BCLK_X$ Low to Data Output Disabled	t_{DZC}		50		165	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	t_{DZF}	$C_L = 0pF$ to 150pF	20		165	ns
Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low	t_{SDB}		50			ns
Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	t_{HBD}		50			ns
Delay Time from $BCLK_{R/X}$ Low to SIG_R Valid	t_{DFSSG}	Load = 50pF plus 2 LSTTL loads			300	ns
Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	t_{SF}	Short frame sync pulse (1 or 2 bit clock periods long) (Note 1)	50			ns
Width of Master Clock High	t_{WMH}	$MCLK_X$ and $MCLK_R$	160			ns
Width of Master Clock Low	t_{WML}	$MCLK_X$ and $MCLK_R$	160			ns
Rise Time of Master Clock	t_{RM}	$MCLK_X$ and $MCLK_R$			50	ns
Fall Time of Master Clock	t_{FM}	$MCLK_X$ and $MCLK_R$			50	ns
Set-Up Time from $BCLK_X$ High (and FS_X In Long Frame Sync Mode) to $MCLK_X$ Falling Edge	t_{SBFM}	First bit clock after the leading edge of FS_X				
Period of Bit Clock	t_{PB}		485	488	15,725	ns
Width of Bit Clock High	t_{WBH}	$V_{IH} = 2.2V$	160			ns
Width of Bit Clock Low	t_{WBL}	$V_{IL} = 0.6V$	160			ns

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TIMING CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	t_{HF}	Short frame sync pulse (1 or 2 bit clock periods long) (Note 1)	100			ns
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	t_{HBFI}	Long frame sync pulse (from 3 to 8 bit clock periods long)	100			ns
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64K bit/s operating mode	160			ns

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

TIMING DIAGRAM

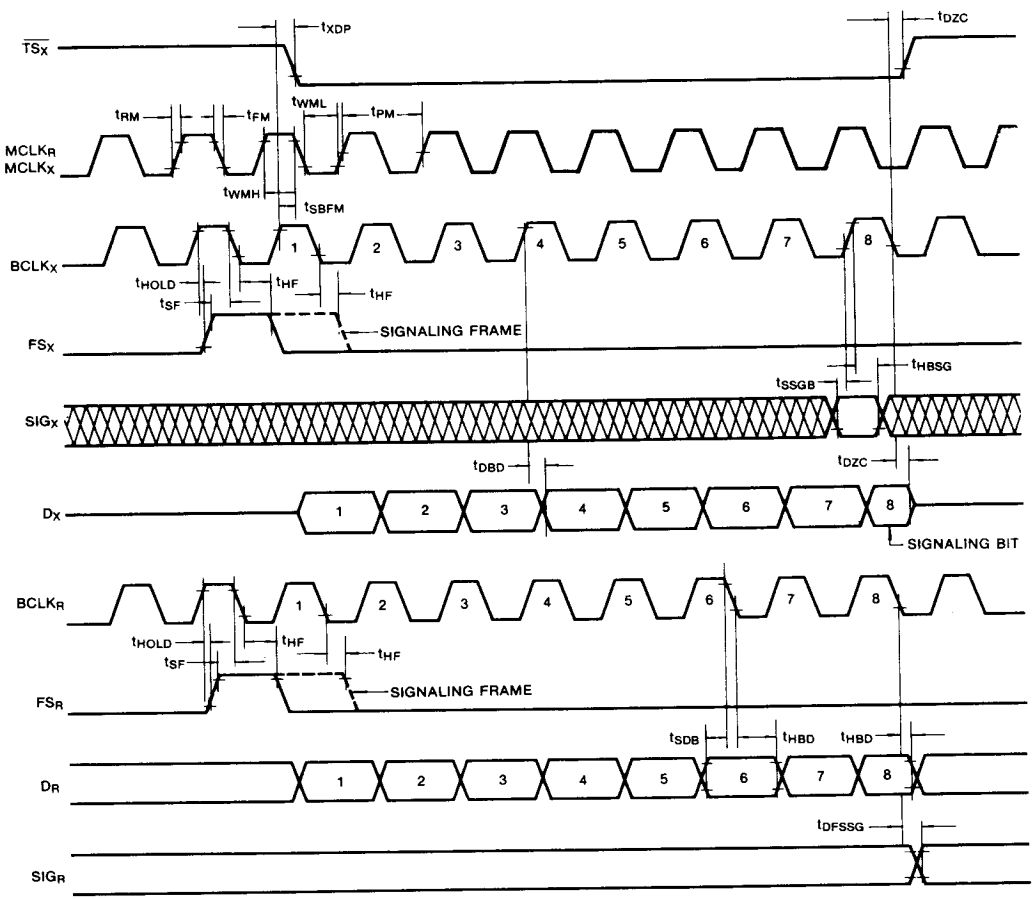

Fig. 2. Short Frame Sync Timing

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TIMING DIAGRAM (Continued)

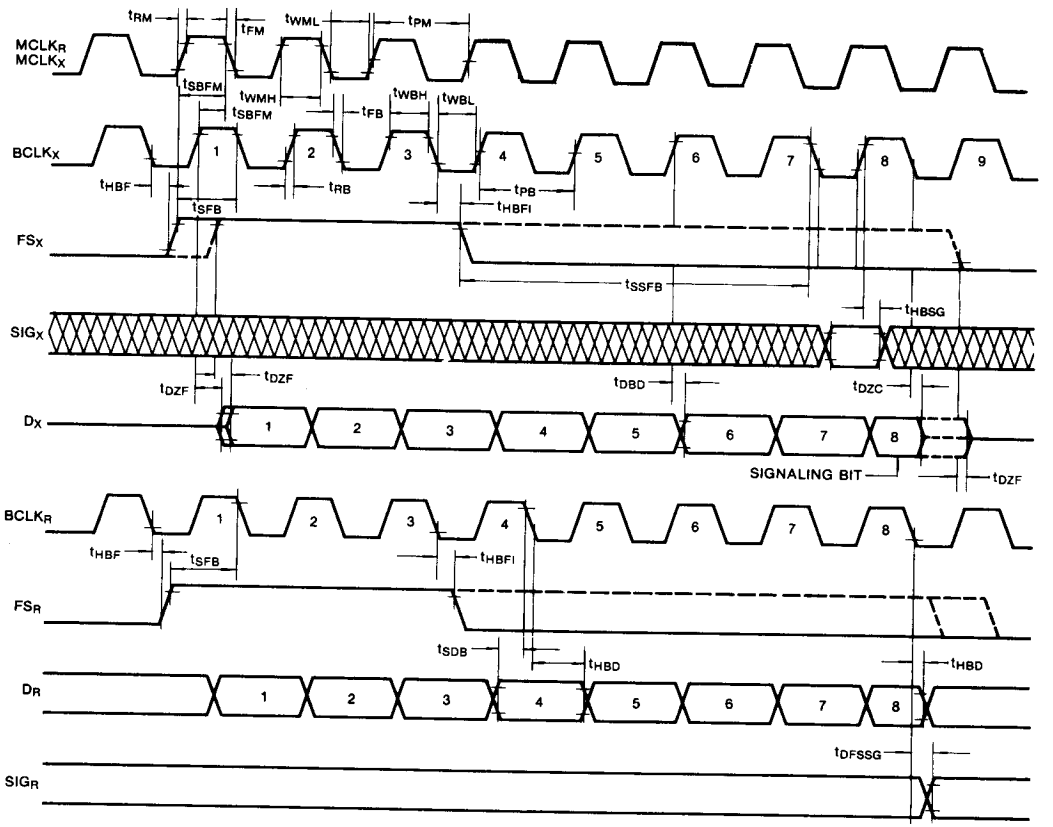

Fig. 3 Long Frame Sync Timing

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TRANSMISSION CHARACTERISTICS

(Unless otherwise specified: Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, GNDA = 0V, f = 1.02KHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity-gain non-inverting.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Amplitude Response						
Receive Gain, Absolute	G_{RA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = −5V Input = Digital code sequence for 0dBm0 signal at 1020Hz	−0.15		0.15	dB
Receive Gain, Relative to G_{RA}	G_{RR}	f = 0Hz to 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz	−0.15 −0.35 −0.7		0.15 0.05 0 −14	dB dB dB dB
Absolute Receive Gain Variation with Temperature	G_{RAT}	Ta = 0°C to 70°C			±0.1	dB
Absolute Receive Gain Variation with Supply Voltage	G_{RAV}	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%			±0.05	dB
Receive Gain Variations with Level	G_{RRL}	Sinusoidal test method; reference input PCM code corresponds to an ideally encoded −10dBm0 signal PCM level = −40dBm0 to +3dBm0 PCM level = −50dBm0 to −40dBm0 PCM level = −55dBm0 to −50dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
Receive Output Drive Level	V_{RO}	R_L = 600Ω	−2.5		2.5	V
Absolute Levels	A_L	Nominal 0dBm0 level is 4dBm (600Ω) 0dBm0		1.2276		V_{rms}
Max Overload Level	t_{MAX}	Max overload level (3.17dBm0): KT8554 Max overload level (3.14dBm0): KT8557		2.501		V_{PK}
Transmit Gain, Absolute	G_{XA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = −5V Input at GS_X = 0dBm0 at 1020Hz	−0.15		0.15	dB
Transmit Gain, Relative to G_{XA}	G_{XR}	f = 16Hz f = 50Hz f = 60Hz f = 200Hz f = 300Hz − 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up, measure response from 0Hz to 4000Hz	 −1.8 −0.15 −0.35 −0.7		−40 −30 −26 −0.1 0.15 0.05 0 −14 −32	dB dB dB dB dB dB dB dB dB
Absolute Transmit Gain Variation with Temperature	G_{XAT}	Ta = 0°C to 70°C			±0.1	dB
Absolute Transmit Gain Variation with Supply Voltage	G_{XAV}	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%			±0.05	dB
Transmit Gain Variations with Level	G_{XRL}	Sinusoidal test method Reference level = −10dBm0 VF_XI+ = −40dBm0 to +3dBm0 VF_XI+ = −50dBm0 to −40dBm0 VF_XI+ = −55dBm0 to −50dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB

4

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TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Envelope Delay Distortion with Frequency						
Receive Delay, Absolute	D_{RA}	f = 1600Hz		180	200	μs
Receive Delay, Relative to D_{RA}	D_{RR}	f = 500Hz – 1000Hz f = 1000Hz – 1600Hz f = 1600Hz – 2600Hz f = 2600Hz – 2800Hz f = 2800Hz – 3000Hz	– 40 – 30	– 25 – 20 70 100 145	 90 125 175	μs μs μs μs μs
Transmit Delay, Absolute	D_{XA}	f = 1600Hz		290	315	μs
Transmit Delay, Relative to D_{XA}	D_{XR}	f = 500Hz – 600Hz f = 600Hz – 800Hz f = 800Hz – 1000Hz f = 1000Hz – 1600Hz f = 1600Hz – 2600Hz f = 2600Hz – 2800Hz f = 2800Hz – 3000Hz		195 120 50 20 55 80 130	220 145 75 40 75 105 155	μs μs μs μs μs μs μs
Noise						
Receive Noise, C Message Weighted	N_{RC}	PCM code equals alternating positive and negative zero, KT8554		8	11	dBmc0
Receive Noise, P Message Weighted	N_{PP}	PCM code equals, positive zero, KT8557		– 82	– 79	dBm0p
Transmit Noise, C Message Weighted	N_{XC}	KT8554		12	15	dBmc0
Transmit Noise, P Message Weighted	N_{XP}	KT8557		– 74	– 67	dBm0p
Noise, Single Frequency	N_{RS}	f = 0KHz to 100KHz, loop around measurement, $VF_XI+ = 0V_{rms}$			– 53	dBm0
Positive Power Supply Rejection, Transmit	$PPSR_X$	$VF_XI+ = 0V_{rms}$, $V_{CC} = 5.0V_{DC} + 100mV_{rms}$ f = 0KHz – 50KHz	30	35		dBC
Negative Power Supply Rejection, Transmit	$NPSR_X$	$VF_XI+ = 0V_{rms}$, $V_{BB} = -5.0V_{DC} + 100mV_{rms}$ f = 0KHz – 50KHz	40	45		dBC
Positive Power Supply Rejection, Receive	$PPSR_R$	PCM code equals positive zero $V_{CC} = 5.0V_{DC} + 100mV_{rms}$ f = 0Hz – 4000Hz f = 4KHz – 25KHz f = 25KHz – 50KHz	 35 35 35			 dBC dB dB
Negative Power Supply Rejection, Receive	$NPSR_R$	PCM code equals positive zero $V_{BB} = -5.0V_{DC} + 100mV_{rms}$ f = 0Hz – 4000Hz f = 4KHz – 25KHz f = 25KHz – 50KHz	 40 40 36			 dBC dB dB

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TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious Out-of-Band Signals at the Channel Output	SOS	Loop around measurement, 0dBm0, 300Hz – 3400Hz input applied to VF_XI+, Measure individual image signals at VF_RO 4600Hz – 7600Hz 7600Hz – 8400Hz 8400Hz – 100,000Hz			 – 32 – 40 – 32	 dB dB dB
Distortion						
Signal to Total Distortion	STD_X	Sinusoidal test method				
Transmit or Receive Half-Channel	STD_R	Level = 3.0dBm0 = 0dBm0 to 30dBm0 = – 40dBm0 XMT RCV = – 55dBm0 XMT RCV	33 36 29 30 14 15			dBC dBC dBC dBC dBC dBC
Single Frequency Distortion, Transmit	SFD_X				– 46	dB
Single Frequency Distortion, Receive	SFD_R				– 46	dB
Intermodulation Distortion	IMD	Loop around measurement, VF_X+ = – 4dBm0 to – 21dBm0, two frequencies in the range 300Hz – 3400Hz			– 41	dB
Crosstalk						
Transmit to Receive Crosstalk, 0dBm0 Transmit Level	$CT_{X\text{-}R}$	f = 300Hz – 3400Hz D_R = Steady PCM code		– 90	– 75	dB
Receive to Transmit Crosstalk, 0dBm0 Receive Level	$CT_{R\text{-}X}$	f = 300Hz – 3400Hz, VF_XI = 0V		– 90	– 70 (Note 1)	dB

Note 1. $CT_{R\text{-}X}$ is measured with a – 40dBm0 activating signal applied at VF_XI+

ENCODING FORMAT AT Dx OUTPUT

	μ-Law KT8554	A-Law KT8557
V_{IN} (at GS_X) = + Full – Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_{IN} (at GS_X) = 0V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V_{IN} (at GS_X) = – Full – Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

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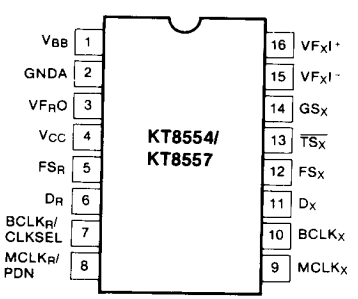
PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{BB}	Negative power supply. $V_{BB} = -5V \pm 5\%$.
2	GNDA	Analog ground. All signals are referenced to this pin.
3	VF_RO	Analog output of the receive filter.
4	V_{CC}	Positive power supply. $V_{CC} = +5V \pm 5\%$.
5	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8KHz pulse train.
6	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
7	$BCLK_R$/ CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. Many vary from 64KHz to 2.048MHz. Alternatively, may be a logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions.
8	$MCLK_R$/ PDN	Receive master clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continously low, $MCLK_R$ is selected for all internal timing. When $MCLK_R$ is connected continuously high the device is powered down.
9	$MCLK_X$	Transmit master clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_R$.
10	$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64KHz to 2.048MHz, but must be synchronous with $MCLK_X$.
11	D_X	The TRI-STATE PCM data output which is enabled by FS_X.
12	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8KHz pulse train.
13	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
14	GS_X	Analog output of the transmit input amplifier. Used to externally set again.
15	$V_{FXI}-$	Inverting input of the transmit input amplifier.
16	$V_{FXI}+$	Non-inverting input of the transmit input amplifier.

PIN CONNECTION



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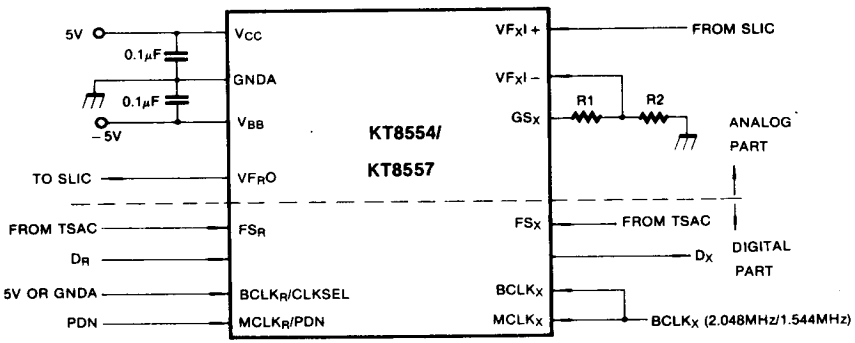
APPLICATION CIRCUITS



Note: XMIT gain $= 20 \times \log(\frac{R1 + R2}{R2})$, $(R1 + R2) > 10K\Omega$.

Fig. 4

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