YAMAR
Datasheet

DMX250 – DMX/RDM Over Powerline Transceiver

1. Overview

The DMX250 is a transceiver designed for DMX/RDM network communication over the Power line. The device operates at a speed of 250Kbit/s. It eliminates complex cabling and simplifies installation.
The DMX512 messages over the power line are error protected and modulated using narrow-band frequency. Up to eight independent DMX/RDM networks can operate in parallel on the same power line using different frequencies. A QFN32 5x5 mm package provides a small PCB footprint
A single capacitor couples the device to the DC power line. A simple high voltage interface (external) allows operation over AC power lines.

Main Features

- **DMX512/RDM Communication over DC power line**
- **Up to eight DMX networks sharing the same powerline**
- **251 selectable carrier frequencies (5MHz to 30MHz).**
- **Sleep mode for low power consumption**
- **Built-in Modem, Error Correction & Synchronization**

Main Benefits

- **Eliminates complex DMX cables**
- **Reduces weight and installation time**
- **Robust to power line noises**
- **Increase reliability**
- **Allows flexible networks designs**
- **Low-cost CMOS Implementation**

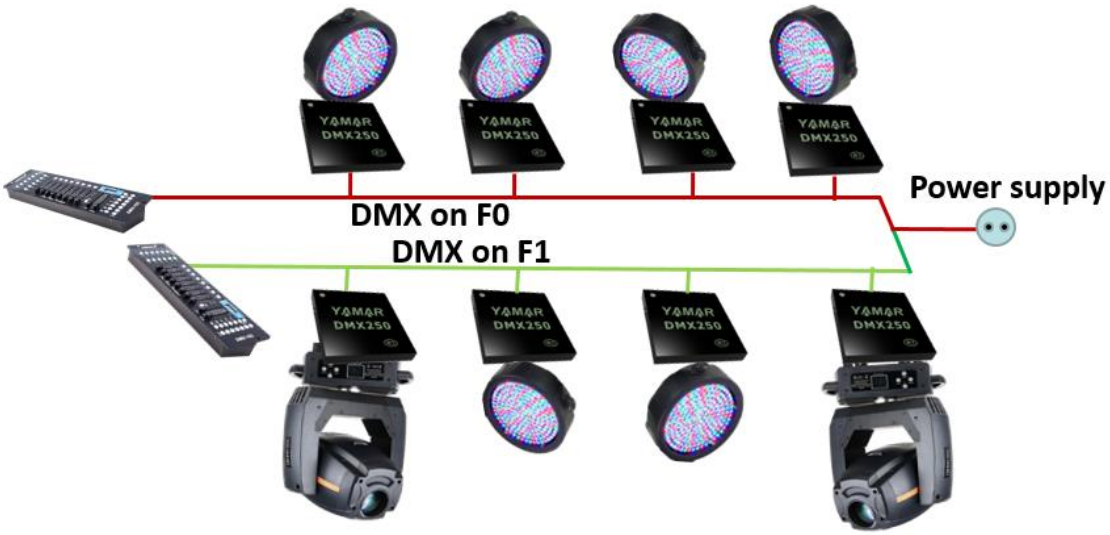

Figure 1 – DMX250 powerline networks sharing single powerline

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2. Description

2.1 The DMX250 network

The DMX250 operates as part of a powerline (DC-BUS) communication network consisting of multiple DMX250 devices. The DMX/RDM data is phase modulated by a sine wave at a user predefined carrier frequency with built-in error correction protection.
All network topologies (e.g. Star, ring, line, tree, etc.) are applicable, as long as the RX signal level at RXI is above minimal RXI_{lev} (see Table 16).
Users may create multiple DMX250 networks operating over a single powerline, where each network communicates using a different carrier frequency (channel).

2.2 DMX250 channel parameters

Carrier frequency:	251 selectable frequencies between 5MHz - 30MHz with 100 kHz spacing.
Powerline bitrate:	250Kbit/s
Powerline voltage:	Any, with proper powerline coupling interfacing (see 2.5.6)
Cable length:	Depends on the powerline loads AC signal-attenuation (100m is practicable)
Cable type:	Any cable.

2.3 Device architecture

Figure 2 depicts the DMX250 blocks.

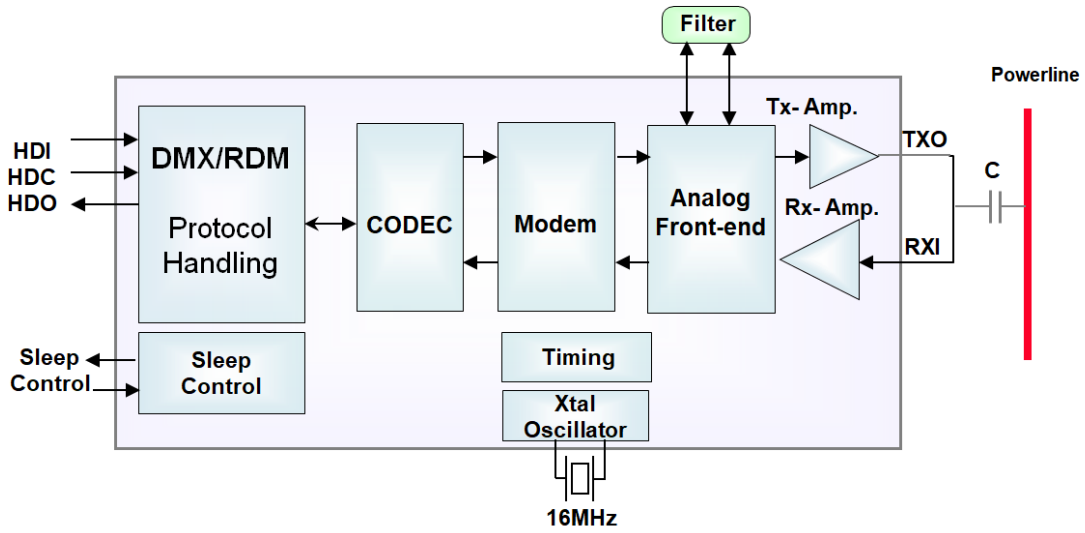


Figure 2 - DMX250 block diagram

The DMX250 main building blocks:

- **Protocol handling** - Interprets the DMX512 & RDM protocols.
- **CODEC** - Encodes/decodes the data.
- **Modem -** Phase modulates and demodulates the data to and from the DC-BUS powerline.
- **Sleep** - Ensures low power consumption during Sleep mode.

2.4 Pin configuration and function

2.4.1 Pinout diagram

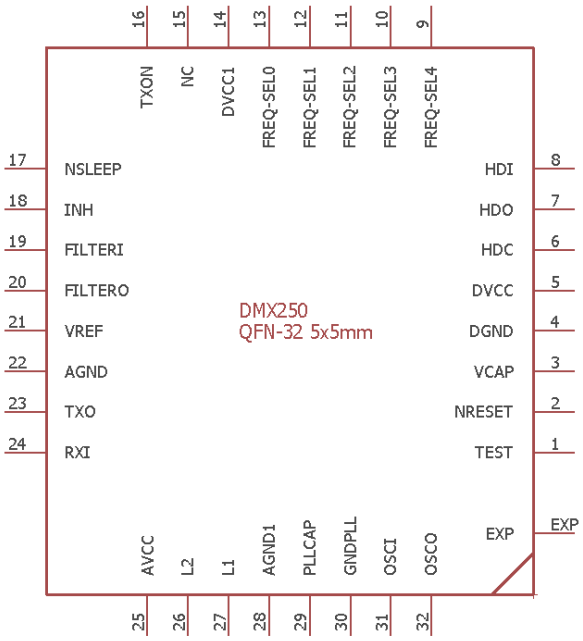


Figure 3 - DMX250 pinout diagram in QFN32 5x5mm package

2.4.2 Signals and Pinout description

Table 1 - Pinout description

Name	Pin #	Pin type	Internal PU/PD	Description
HDO	7	Output 12mA		Digital data output signal. Outputs the received data from the powerline or from internal registers to the DMX-controller.
HDI	8	Digital input	PU	Digital data input signal. Transfers data from the DMX-controller to the powerline or the internal registers.
HDC	6	Digital input	PU	Data / command input, enables read and write from/to DMX250 control registers (see section 5.10)
TEST	1	Digital Input	PD	Should be connected to GND.
NRESET	2	Digital Input	PU	Reset, active low.
NSLEEP	17	Digital Input		Sleep mode control input (see section 4.3). Should be pull-up to 3.3V when not in use.
FREQ_SEL4	9	Digital Input		Carrier Frequency selection inputs. See Table 7.
FREQ_SEL3	10			
FREQ_SEL2	11			
FREQ_SEL1	12			
FREQ_SEL0	13			
NC	15			Should be left floated.
INH	18	Digital Output 8mA		When high, DMX250 is in Normal mode When low, DMX250 is in Sleep mode
TXON	16	Output 12mA		TX_ON output - High when transmission onto the powerline is active.

<table>
<tr><th>Name</th><th>Pin #</th><th>Pin type</th><th>Internal PU/PD</th><th>Description</th></tr>
<tr><td>TXO</td><td>23</td><td>Analog Output
Max 66 mA</td><td></td><td>Powerline Transmit signal out
<table>
<tr><td>TXON State</td><td>REG_1[3]</td><td>TX level [V-p-p]</td><td>Impedance [Ω]</td></tr>
<tr><td rowspan="2">High</td><td>'0'</td><td>1</td><td rowspan="2">18 [1]</td></tr>
<tr><td>'1' (Default)</td><td>2</td></tr>
<tr><td>Low</td><td></td><td>High Z</td><td>5.3k [2]</td></tr>
</table>
[1]Series output impedance
[2]Input impedance referenced to VREF</td></tr>
<tr><td>RXI</td><td>24</td><td>Analog Input</td><td></td><td>Powerline receive Input</td></tr>
<tr><td>VREF</td><td>21</td><td>Analog Output</td><td></td><td>Analog out reference VCC/2 for filtering capacitor. Place 1uF between VREF to AGND. The VREF is used as a virtual ground for the external analog circuitry.</td></tr>
<tr><td>FILTERI</td><td>19</td><td>Analog,
Bi-directional</td><td></td><td>External filter I/O</td></tr>
<tr><td>FILTERO</td><td>20</td><td>Analog,
Bi-directional</td><td></td><td>External filter I/O</td></tr>
<tr><td>OSCO</td><td>32</td><td>Analog output</td><td></td><td>16MHz Crystal Output</td></tr>
<tr><td>OSCI</td><td>31</td><td>Analog Input</td><td></td><td>16MHz Crystal Input</td></tr>
<tr><td>L1</td><td>27</td><td>Analog Input</td><td></td><td>External inductor L1 (pin capacitance should be maximal 1pF), see 2.5.4.</td></tr>
<tr><td>L2</td><td>26</td><td>Analog Input</td><td></td><td>External inductors L2 (optional), see 2.5.4.</td></tr>
<tr><td>AVCC</td><td>25</td><td>Power</td><td></td><td>Analog 3.3V supply</td></tr>
<tr><td>AGND</td><td>22,28</td><td>Power</td><td></td><td>Analog ground</td></tr>
<tr><td>VCAP</td><td>3</td><td>Power</td><td></td><td>1.8V core supply output for filtering capacitor. Place 4.7uF between VCAP and DGND.</td></tr>
<tr><td>DGND</td><td>4</td><td>Power</td><td></td><td>Digital Ground</td></tr>
<tr><td>DVCC</td><td>5,14</td><td>Power</td><td></td><td>Digital 3.3V supply</td></tr>
<tr><td>GNDPLL</td><td>30</td><td>Power</td><td></td><td>Analog Ground</td></tr>
<tr><td>PLLCAP</td><td>29</td><td>Power</td><td></td><td>PLL 1.8V output to a filtering capacitor. Place 1uF between PLLCAP and GNDPLL.</td></tr>
<tr><td>EXP</td><td>33</td><td>Power</td><td></td><td>Expose pad, should be connected to DGND.</td></tr>
</table>

PD – Internal Pull-down resistor 50K ohm +/-%30
PU – Internal Pull-up resistor 50K ohm +/-%30

2.5 Implementation

2.5.1 DMX250 reference schematic

Figure 4 depicts a typical DMX250 schematic.

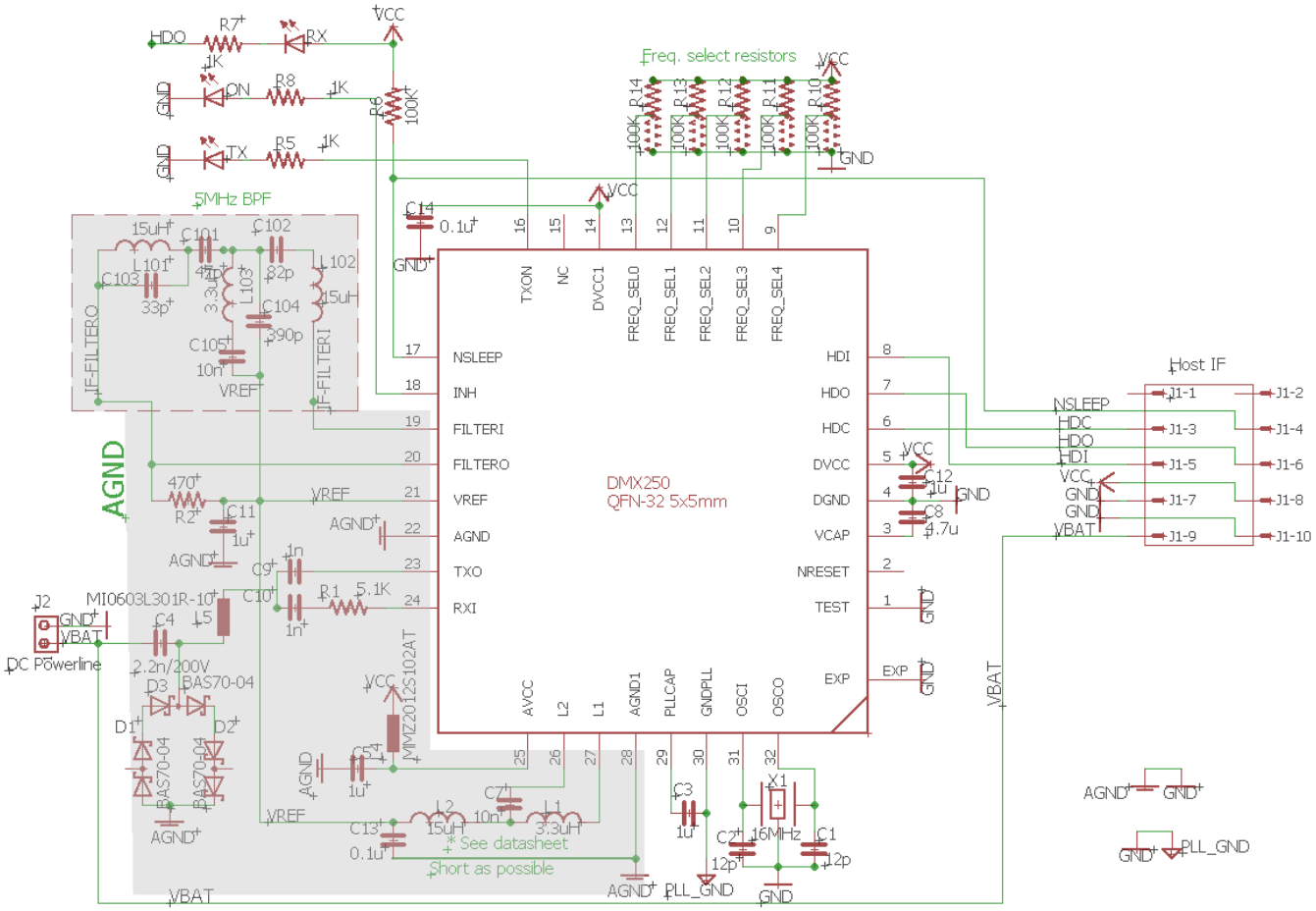


Figure 4 - DMX250 reference schematic

2.5.2 External filter (BPF)

The DMX250 operates using an external 5MHz bandpass filter. The minimum allowable bandwidth of the filters is +/-700 kHz @ 3dB. Narrower bandwidth limits the maximal bitrate.
Figure 5 depicts a recommended 5MHz discrete passive filter**.**

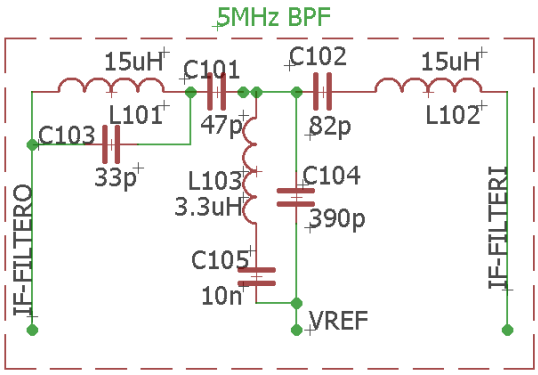


Figure 5- 5MHz bandpass filter

2.5.3 External Crystal

The device operates with a low cost, small size 16MHz crystal connected between OSCI and OSCO pins. Each of these pins should be connected to the DGND via a load capacitor. The load capacitors' values should be determined according to the crystal manufacturer's recommendations and the actual PCB layout. The PCB traces should be as short as possible.
The overall frequency tolerance should not exceed ± 50ppm.

2.5.3.1 Recommended Crystals

- NDK - NX2520SA-16MHz, SMD, 2.5x2 mm
- NDK - NX3225SA/GB-16MHz, SMD, 3.2x2.5mm
- NDK - NX2016GC-16MHz, SMD, 2.0x1.6mm
- ECS - ECS-160-12-37B-CTN-TR, SMD, 2.0x1.6mm

2.5.3.2 16MHz clock from an external source

It is possible to operate the device from an external 16HMz clock source that meets the requirements above.
Figure 6 depicts an external 16MHz clock connection to the device.

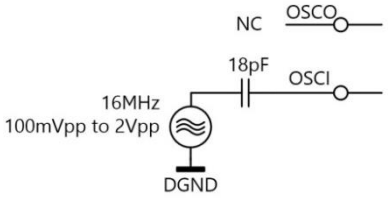


Figure 6 - External 16MHz clock connection

2.5.4 L1 and L2 inductors

The DMX250 requires one or two inductors for its operation, depending on the desired operating frequency.

- For full in-band operation, 5MHz - 30MHz:
  - L1 - 3.3uH
  - L2 - 15uH with 10nF series capacitor between L2 pin and L2 inductor.

- For low in-band operation, 5MHz -12MHz:
  - L1 - 18uH
  - L2 - NC

- For high in-band operation, 12MHz - 30MHz:
  - L1 - 3.3uH
  - L2 - NC

Figure 7 depicts the in-band operation inductors' connection to pins L1 and L2.

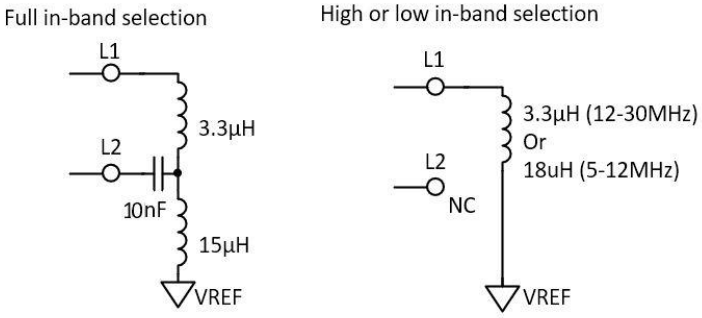


Figure 7 - L1 and L2 inductors connections

2.5.4.1 Recommended L1 & L2 inductors

Table 2 describes the recommended L1 and L2 inductors.

Table 2 - Recommended L1 and L2 manufacturers

Inductor	ABRACON	VISHAY	TDK
L1=3.3uH	815-AIML-0805-3R3K-T	ILSB0805ER3R3K	MLF2012A3R3JT000
L2=15uH	815-AIML-0805-150K-T	ILSB0805ER150K	MLF2012C150KT000
L1=18uH	815-AIML-0805-180K-T	ILSB0805ER180K	MLF2012C180KT000

2.5.5 Optional EMC chip-bead (L5)

For enhanced mitigation of high harmonics above 30MHz conducted over the powerline, it is recommended to add L5 in series to the coupling capacitor C4 (see Figure 4).

Table 3 describes the recommended EMC chip-beads.

Table 3 - Recommended L5 (optional)

LAIRD	MI0603L301R-10
LAIRD	HZ0603A222R-10
TDK	MMZ1608Q

2.5.6 TXO output level and drive control

The TXO pin output level and drive capability to the powerline are controlled by REG_*1[3]*, as described in Table 4.

Table 4 - TXO signal level

TXON State	REG_1[3]	TX level [V-p-p]
High	'0'	1
	'1' (Default)	2
Low (Rx)		High Z

Setting the TXO output drive capability is made by configuring REG_*1[0]*, as described in Table 5.

Table 5- TXO output drive control

TXON State	REG_1[0]	Output drive [A]	Impedance [Ω]
High	'0' (Default)	33mA	18 [1]
	'1'	66mA	
Low (Rx)		Disabled	5.3k [2]

[1]Series output impedance

[2]Input impedance referenced to VREF

2.5.7 Ceramic capacitors

Low ESR capacitors will provide better performance. X5R and X7R capacitors are recommended, especially for Vcap (C8) and PLLCAP (C3).

2.5.8 Powerline coupling interface

The DMX250 is coupled to the powerline through a single small footprint coupling capacitor that blocks the DC, typically 2.2nF. The $C_{coupling}$ voltage rating depends on the powerline voltage and its expected impulses.

2.5.8.1 External protection network

It is recommended to add an external diode protection network before the $C_{coupling}$, for protection from high powerline pulses (above 2 V-P-P). The protection network consists of three Schottky diodes serially connected (for both polarities), with low capacitance (< 10pF) and fast clipping (e.g. BAS70-04).

2.5.8.2 AC Powerline coupling interface

Figure 8 presents a possible high voltage AC and DC powerline interface. The DMX high-frequency carrier is coupled to the powerline via capacitors C7 and C8. D5, D6, and D7 are external protection networks that clip the residual high voltage impulses that may pass via C7 and C8.

It is the system designer's responsibility to check the local regulations for high voltage coupling.

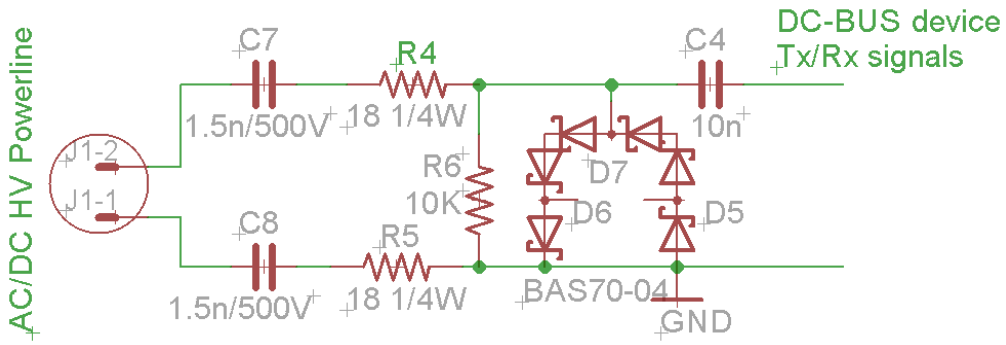


Figure 8 – Possible high voltage interface

2.5.9 Recommended connection to power-supply

Power-supplies usually require big filtering capacitors that may attenuate strongly the DMX250 carrier signal. It is recommended to add an inductor (>22uH) or ferrite bead (>100Ω @ 5MHz-30MHz) in series to the power supply connection to the DC powerline to avoid carrier signal attenuation.
Figure 9 depicts a typical DMX250 connection to a DC powerline and its power-supply.

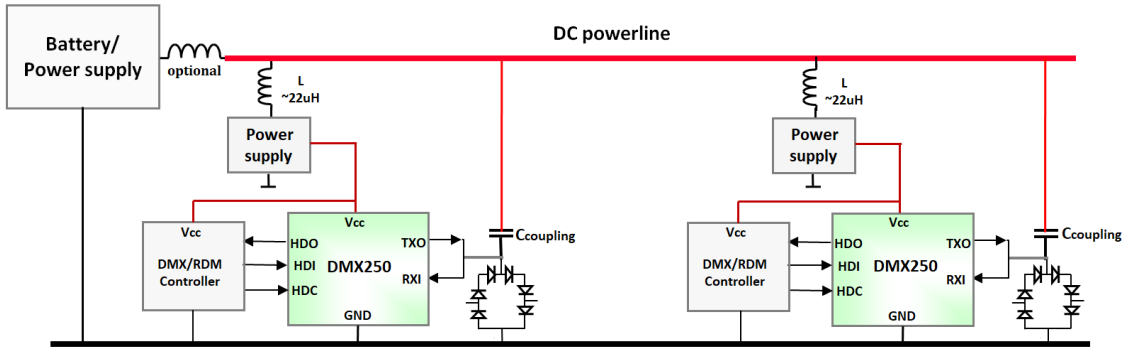


Figure 9 – DMX250 connection to 3.3V power-supply and powerline

3. DMX250 operation

3.1 Interfacing with DMX/RDM Controller

The DMX communication protocol uses four pins as described in Table 6.

Table 6- DMX/RDM interface pins

HDI	Data Input from the DMX-controller.
HDC	Data/Command select input. When pulled down, the DMX250 enters command mode, enabling access to DMX250 Control registers.
HDO	Data output to the DMX-controller

Figure 10 depicts a typical DMX250 to DMX/RDM controller interface connection.

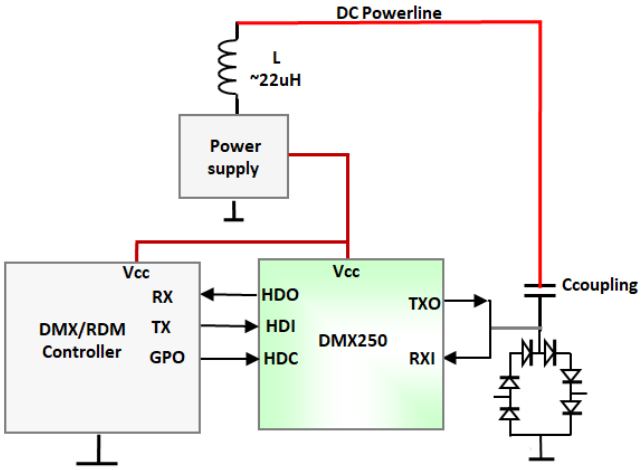


Figure 10 – Typical DMX250 to DMX/RDM controller interface

3.2 Interfacing to an existing DMX/RDM module

When interfacing to an existing DMX/RDM module that has already a built-in RS485 transceiver, an additional RS485 transceiver is required to translate the signals to Tx and Rx 3.3V logic.

Figure 11 depicts a typical DMX250 to RS485 transceiver interface connection.

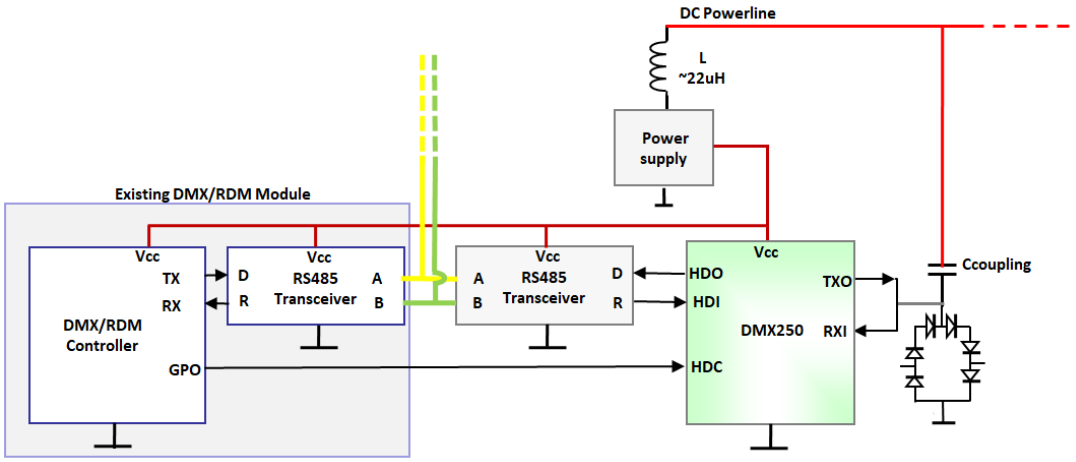


Figure 11 – Typical DMX250 to RS485 transceiver interface

3.3 DMX250 messages

3.3.1 Message structure

The DMX250 is DMX/RDM message-oriented device. The message is divided by the DMX250 into packets that are encoded against errors and constructed into modulated powerline message (frame).
A frame is constructed from a Start-frame consisting of a preamble and optionally an arbitration sequence (in RDM discovery process only), followed by packet/s of data bytes (at least 1 packet) and terminated with a "*Frame-End*" indicating the last packet of the frame.
When the RDM discovery process is activated by the DMX-controller, unique arbitration patterns are transmitted before the start-frame preamble pattern (see 3.3.4).

- Start of frame preamble length - **64usec**
- Arbitration pattern length (For RDM Discovery only) - **336 usec**.
- Packet length - **180usec**

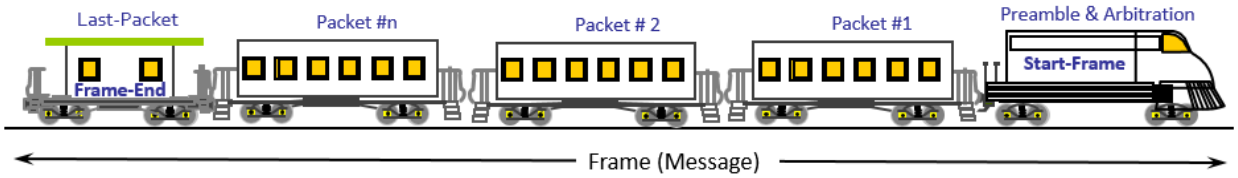


Figure 12 – Frame (Message) structure

3.3.2 Transmit flow

Upon detecting the DMX/RDM start of message on the HDI pin, the DMX250 initiates a new powerline frame containing the DMX/RDM message data bytes. A DMX/RDM frame contains a single DMX/RDM message sent from the DMX-controller.

3.3.3 Receive flow

Upon detecting a powerline frame, the frame is decoded back into the DMX/RDM original message and sent sequentially to the DMX-controller through the HDO pin.

3.3.4 Auto Arbitration mode (RDM Discovery)

The Arbitration mode is used to prioritize messages over the powerline when the RDM discovery process is activated by the DMX-controller. The arbitration mechanism is used to allow the message with higher priority (lower arbitration ID) to gain access and transmit its message over the DC-BUS. When an RDM discovery response message from an RDM slave is detected, the powerline frame will begin with an arbitration sequence to gain access to the powerline. In case the arbitration has passed successfully, then the DMX250 will proceed with data frame transmission, else, the DMX250 will abort the transmission and receive the message from another DMX250 device.

3.4 Carrier frequency settings

Users can define carrier frequency from 5MHz to 30MHz with a spacing of 100 kHz (A total of 251 selectable carriers). The active carrier frequency selection is made either by setting FREQ_SEL[4:0] pins or by configuring REG_*2* (see 5.2). After a power-up or hard-reset event, the carrier frequency is set according to FREQ_SEL[4:0] state (see Table 7). Then, the carrier frequency is updated according to either REG_2 configuration or FREQ_SEL[4:0] changed status. The last action prevails.

Upon completion of configuration, the DMX250 will update its operating carrier frequency within 1msec. During this 1msec period, the DMX250 is kept in Soft-reset and will not communicate with its DMX-controller nor detect new frames (messages) from the powerline.

When setting multiple DMX250 networks to operate over a single powerline, it is recommended to select carrier frequencies spaced more than 1.5MHz from each other.

Table 7 describes FREQ_SEL[4:0] frequency selection allocation.

Table 7 – FREQ_SEL[4:0] frequency selection

FREQ_SEL[4:0]	Carrier Frequency [MHz]
5'b00000	REG_2 last configuration (default 13MHz, after power-up/hard-reset event)
5'b00001	8
5'b00010	13
5'b00011	16
5'b00100	20
5'b00101	23
5'b00110	26
5'b00111	30
5'b01000	7
5'b01001	8
5'b01010	9
5'b01011	10
5'b01100	11
5'b01101	12
5'b01110	13
5'b01111	14
5'b10000	15
5'b10001	16
5'b10010	17
5'b10011	18
5'b10100	19
5'b10101	20
5'b10110	21
5'b10111	22
5'b11000	23
5'b11001	24
5'b11010	25
5'b11011	26
5'b11100	27
5'b11101	28
5'b11110	29
5'b11111	30

When configuration REG_2, the carrier-selected value is calculated as given in Definition of equation (1).

Definition of equation

REG_2 = (Carrier Freq. [MHz] - 5) * 10 **(1)**

EXAMPLE 1

- When setting the frequency to 14.1MHz:
  REG_2 = (14.1 - 5) * 10 = **0x5B**

EXAMPLE 2

- When Setting to 5MHz:
  REG_2 = (5 - 5) * 10 = **0x00**

3.5 DMX250 UUID

Each DMX250 device is hard-coded with a 48 bit universally unique identifier (UUID[47:0]).
The UUID is stored in REG_59 to REG_5E and can be retrieved using the READ-REG commands (see 5.4 to 5.95.9).

3.6 DMX interface typical set-up and operation

1. Interface HDI, HDO, and HDC (Optional) pins.
2. Select a carrier frequency (default 13MHz) (see 3.4).
3. Transmit data bytes via HDI pin to the powerline.
4. Receive data bytes from the powerline via HDO pin.

3.7 DMX Examples

3.7.1 DMX Example 1 - Typical communication flow

Figure 13 depicts a typical TX-RX DMX message flow. The DMX-controller starts a new message with a break signal, followed by start code and data bytes on DMX250 HDI. Upon detection of the break signal, the DMX250 initiates the DMX frame over the powerline. After a fixed latency of ~100usec, the DMX250 RX device output on HDO the break signal, followed by the start code and message received data bytes.

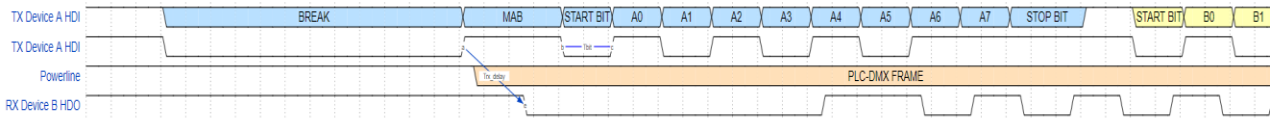


Figure 13 - DMX typical communication sequence

3.7.2 DMX Example 2 - *WRITE-REG* command

Figure 14 depicts a *WRITE-REG* command sequence. First, the HDC is pulled low and the device enters the Command mode. The DMX-controller sends the write command with the 1st byte of 0xF5, followed by the control register address byte (A[7:0]), and then the data byte to be written (B[7:0]). After completing the write sequence, the HDC pin is pulled high and the device returns to Normal mode.

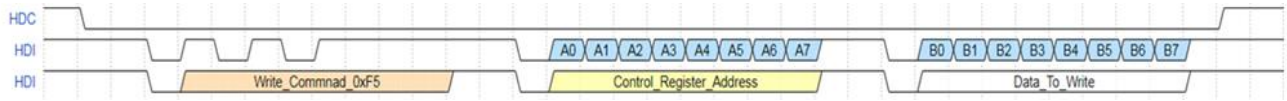


Figure 14- DMX Write Register command sequence

3.7.3 DMX Example 3 - *READ-REG* command

Figure 15 depicts a *READ-REG* command sequence. First, the HDC is pulled low and the device enters the Command mode. The user sends the read command with the 1st byte of 0xFD, followed by the control register address byte (A[7:0]). Then the DMX-controller receives the register internal value (B[7:0]). The HDC pulled back to high and the device returns to Normal mode.

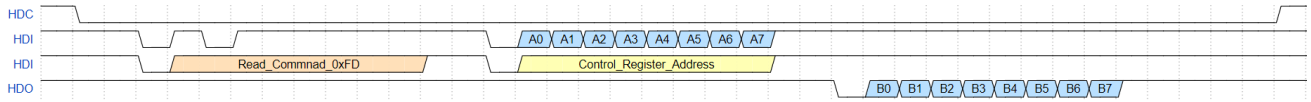


Figure 15 - DMX Read Register command sequence

4. Power operation modes

The DMX250 has three power operation modes; Normal, Standby, and Sleep.

4.1 Normal mode

In Normal mode, the DMX250 is either in RX mode, listening for a powerline message, or in TX mode, transmitting a message over the powerline.

4.2 Standby mode

The DMX250 enters Standby mode upon wake-up from Sleep mode, while the NSLEEP pin is still low. The DMX250 is kept in *Soft-reset*, whereas communication with the DMX-controller is suspended until the NSLEEP pin is set High.

4.3 Sleep modes (power-saving)

The DMX250 has four Sleep modes for best power consumption/performance during Sleep. During this mode, only a small amount of hardware is operational mainly to detect wake-up messages (*WUM*) from the powerline and returning to Normal mode operation.
Table 8 describes the DMX250 sleep modes.

Table 8 - Sleep modes description

Sleep mode	Description	Typical Power consumption [A]	Performance
Enhanced sleep (SLP1)	The device wakes-up every 32ms to sense the powerline for WUM detection.	120µ	Wake-up detection with-in 64mSec. Best detection in a noisy environment.
Fast wake-up (SLP2)	The device continuously monitors the powerline for WUM detection.	1000µ	Fast wake-up detection with-in 250uSec.
Low-power (SLP3)	The device wakes-up every 32ms to sense the powerline for WUM detection.	85µ	Wake-up Detection with-in 64mSec.
Deep Sleep (SLP4)	The device does NOT wake-up to sense for bus activity, staying in deep sleep. Wake-up only locally by the DMX-controller.	65µ	No bus wake-up detection.

The Sleep modes use four interface pins as described in Table 9.

Table 9- Sleep interface pins

NSLEEP	Digital input	High - Normal mode is active. Low - Sleep /Standby mode is active.
INH	Digital output	Output indication to Inhibit DMX-controller. High - Normal mode is active. Low - Sleep mode is active.
HDO	Digital output	**Normal mode** - data output to DMX-controller. **Sleep/Standby mode** - asserted low while the wake-up message is being detected/transmitted over the powerline.
HDC	Digital input	**Normal mode** - DMX-controller Command mode / chip select. **Sleep mode** - DMX-controller wakes-up the DMX250 locally by toggling the HDC high-low-high. The DMX250 then exits the Sleep mode to Standby mode (NSLEEP still asserted low), or Normal mode (NSLEEP is high).

4.3.1 Wake-up message (*WUM)*

When *Auto-WUM* is enabled (REG*[3]='1'*), upon the rise of the NSLEEP pin, the DMX250 transmits a broadcast *WUM* over the powerline, to wake-up all network-connected devices.
DMX-controller can configure the length of the WUM as described in Table 10.

Table 10 - Wake-up message length configuration

REG_3[2]	Wake-up message length
0	*SLP2* - 250usec / *SLP1, SLP3* - 75msec
1	*SLP2* - 1.5msec / *SLP1, SLP3* - 150msec

During WUM transmission, the HDO pin is asserted low until WUM transmission is completed, indicating to the DMX-controller the wake-up process status. DMX-controller shall wait for the HDO rise, before initiating new bytes transfer.

4.3.2 Entering Sleep mode

During Sleep mode, the device is kept in a Soft-reset state and will not transfer data bytes from the DMX-controller nor receive data frames from the powerline. When the device enters Sleep mode, the INH pin is asserted low.
There are two ways to enter Sleep mode;

4.3.2.1 Enter Sleep by NSLEEP

By asserting the NSLEEP pin low, the DMX250 will enter Sleep mode.

4.3.2.2 Enter Sleep by register setting

By setting REG_*3[7]* high, the DMX250 will enter Sleep mode, and reset automatically REG_*3[7]* to low.

4.3.3 Exiting Sleep mode

There are three ways to exit Sleep mode. When exiting Sleep mode, the INH pin is raised and the device switches to Standby or Normal mode.

4.3.3.1 Exit Sleep by *WUM* detection

Upon detection of a *WUM*, the device immediately exits Sleep mode, INH pin rises and the device enters Standby mode.
In case the NSLEEP pin is low, the device remains in Standby mode, where the device is kept in *Soft-reset*.
In case the NSLEEP pin is high, the device immediately switches to Normal mode.
During WUM reception, the HDO pin is asserted low until WUM reception is completed, indicating the DMX-controller on the wake-up process status. DMX-controller shall wait for HDO to rise, before initiating new bytes transfer.

4.3.3.2 Exit sleep by NSLEEP pin

Upon detection of NSLEEP pin rise, the device immediately exits Sleep mode, INH pin rises, and enters Normal mode. When *Auto-WUM is* enabled, a WUM is transmitted over the powerline (see 4.3.1).

4.3.3.3 Exit Sleep by toggling HDC

Upon detection of HDC pin toggle high-low-high, the device immediately exits Sleep mode, INH pin rises, and enters Standby mode.
In case the NSLEEP pin is still low, the device remains in Standby mode, where the device is kept in *Soft-reset*.
In case the NSLEEP pin is high, the device immediately switches to Normal mode.
In this case, the WUM will NOT be transmitted over the powerline.
DMX-controller shall use the HDC pin to exit Sleep mode when the NSLEEP pin is not connected.

4.3.4 Sleep modes description

DMX-controller can select between four Sleep modes (see 5.3).

4.3.4.1 Enhanced Sleep mode (*SLP1*)

By setting REG_*3[1:0] = '00'*, the enhanced Sleep mode (*SLP1*) is selected.
When entering*SLP1*, the device wakes-up every 32ms periodically to monitor (sense period) for activity on the powerline. If a WUM is detected, the device exit Sleep modes as described in section 4.3.3.1, otherwise the device return to Sleep mode until the next sense period, and so on...

4.3.4.2 Fast wake-up Sleep mode (*SLP2*)

By setting REG_*3[1:0] = '01'*, the Fast wake-up Sleep mode (*SLP2*) is selected. The device continuously monitors the powerline for WUM detection. It allows fast WUM detection within 250usec. When WUM is detected, the device exits Sleep mode as described in section 4.3.3.1.

4.3.4.3 Low-power Sleep mode (*SLP3*)

By setting REG_*3[1:0] = '10*', the low-power mode (*SLP3*) is selected. The device wakes-up every 32msec periodically to monitor (sense period) for activity on the powerline. If a WUM is detected, the device exit Sleep modes as described in section 4.3.3.1, otherwise the device return to Sleep mode until the next sense period.

4.3.4.4 Deep Sleep mode (*SLP4*)

By setting REG_*3[1:0] = '11'*, the Deep Sleep mode (*SLP4*) is selected. The device will NOT wake-up to monitor (sense) the powerline for activity, rather than stay in deep sleep, whereas all its analog resources are shut down to maintain the lowest power consumption.
The device can exit Deep Sleep mode locally only, either by the NSLEEP or by HDC pins (see 4.3.3.2 and 4.3.3.3).

4.3.5 Sleep modes Examples

4.3.5.1 Sleep Example 1 - Enter by NSLEEP, Exit Sleep mode by *NSLEEP & WUM*

Figure 16 depicts entering sleep by NSLEEP and exit sleep by NSLEEP pin (Node A) and WUM detection (Node B).
In this example, the DMX-controller wakes-up device Node A by raising the NSLEEP pin. Upon pull-up of the NSLEEP pin, the INH pin is raised and a WUM is transmitted over the powerline (*Auto-WUM* is enabled) to wake-up Node B.
While transmitting the WUM, device Node A asserts HDO pin low. After completion of WUM transmission, the HDO is raised again (can be used as signal/interrupt to DMX-controller). At the Node B side, during its sensing period (e.g. *SLP1),* the WUM is detected, and the INH rises while switching to Standby mode. Node B HDO pin is asserted low for the reaming duration of WUM reception. Then, DMX-controller Node B raises the NSLEEP pin, and the device switches to Normal mode.

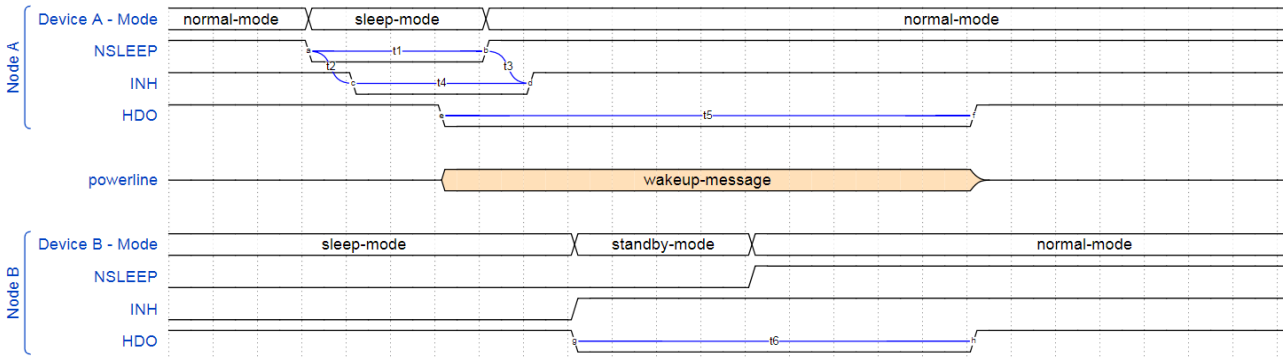


Figure 16 - Enter sleep by NSLEEP, Exit sleep by *NSLEEP & WUM*

4.3.5.1 Sleep Example 2 - Enter sleep by control register bit, exit sleep by HDC

Figure 17 depicts entering sleep by setting REG_*3[7]* high and exiting Sleep mode by toggling the HDC pin.
In this example, DMX-controller configured REG_*3[7]* high using Command mode (DMX interface), the device enters Sleep mode, and INH pin drops. After a while, DMX-controller toggle HDC pin low to high, and the device exits Sleep mode without transmitting the WUM, raising the INH pin and switching to Normal mode again.

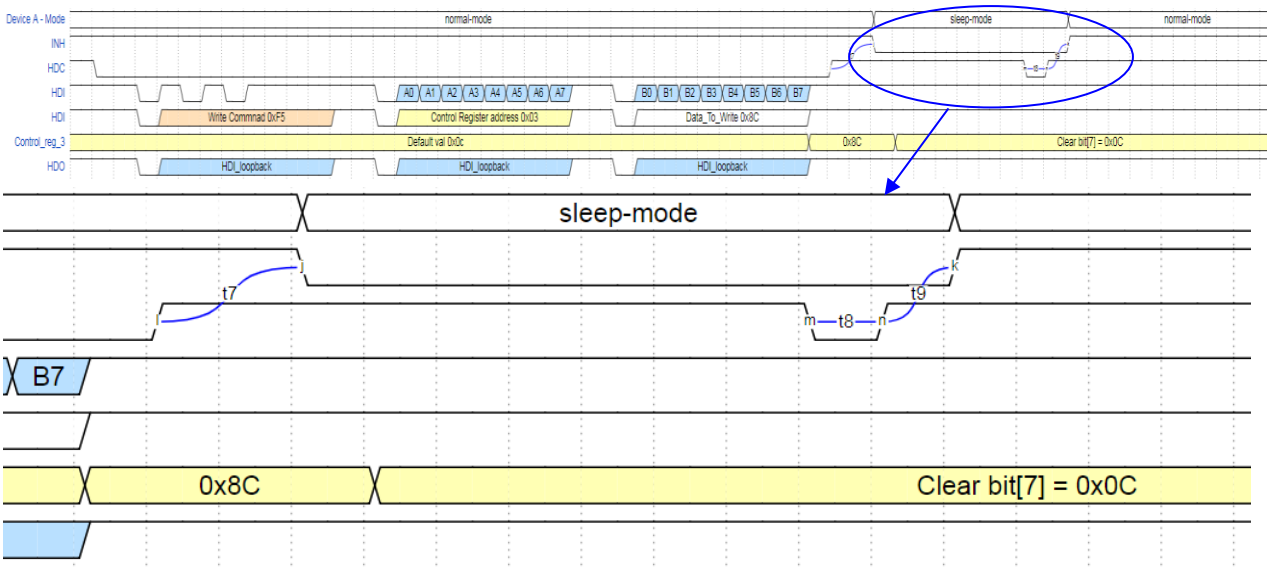


Figure 17 - Enter sleep by control register bit, Exit sleep by *HDC*

5. DMX250 Registers

The DMX250 contains internal registers for configuration and status checks. Each of these registers is accessible by the DMX-controller for *Read* and *Write* operations. The access to these registers is different for each interface protocol and described in the protocol interfaces sections. This section elaborates on the registers and their default values after power-up/reset.

Table 11 - Registers summary table

Register name	Addr.	Description
REG_1 - 'Device Control 1'	0x01	Transmit level control
REG_2 - 'Frequency Select'	0x02	Carrier frequency selection
Reg_3 - 'Sleep Control'	0x03	Sleep modes control
REG_59 – DMX250 UUID[47:40]	0x59	Read only - UUID[47:40]
REG_5A - DMX250 UUID[39:32]	0x5A	Read only - UUID[39:32]
REG_5B - DMX250 UUID[31:24]	0x5B	Read only - UUID[31:24]
REG_5C - DMX250 UUID[23:16]	0x5C	Read only - UUID[23:16]
REG_5D - DMX250 UUID[15:8]	0x5D	Read only - UUID[15:8]
REG_5E - DMX250 UUID[7:0]	0x5E	Read only - UUID[7:0]

5.1 REG_1 - 'Device Control 1' (Address 0x01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
[1]	[1]	[1]	[1]	R/W [1]	[0]	[0]	R/W [0]
1	1	1	1	TX signal level	0	0	Enable TXO high power

Bit [0] - Enable TXO high power. Set this bit to enable maximal TXO drive of 66mA, clear this bit for maximal TXO drive of 33mA (see section 2.5.6).
Bit [1] - '0'
Bit [2] - '0'
Bit [3] - TX signal level control at TXO pin: '0' = 1Vpp, '1'- 2Vpp (see section 2.5.6).
Bit [7:4] - '1111'

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

5.2 REG_2 - 'Frequency Select' (Address 0x02)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [1]	R/W [0]	R/W [1]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
Carrier Frequency Configuration							

Bits [7:0] - Carrier Frequency configuration from in-band. Default configuration is 13MHz
(See section 3.4 - Carrier frequency).

5.3 REG_3 - 'Sleep Control (Address 0x03)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W [0]	[0]	[0]	[0]	R/W [1]	R/W [1]	R/W [0]	R/W [0]
Enter Sleep mode	0	0	0	Auto WUM	Long WUM	Sleep modes selection	

Bit [1:0] - '00' - Enhanced Sleep mode [*SLP1*], '01' -Fast wake-up Sleep mode[*SLP2*], '10' - Low-power sleep mode [*SLP3*], '11' - Deep Sleep mode [*SLP4*] (see section 4.3).
Bit [2] - Control powerline wake-up message duration (see Table 10).
Bit [3] -Auto wake-up message (WUM): '0' disables transmission of WUM after wakeup from NSLEEP pin.
Bits [6:4] - '0'
Bit [7] - Enter Sleep mode reg. Instead of entering Sleep mode through the NSLEEP pin, the user can activate the Sleep mode selected in bits [1:0], by setting bit[7]. After entering Sleep mode, bit [7] is automatically cleared to '0'.

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

5.4 REG_59 – UUID[47:40] (Address 0x59)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[47:40]							

Bits [7:0] - UUID[47:40]

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

5.5 REG_5A – UUID[39:32] (Address 0x5A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[39:32]							

Bits [7:0] - UUID[39:32]

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

5.6 REG_5B – UUID[31:24] (Address 0x5B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[31:24]							

Bits [7:0] - UUID[31:24]

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

5.7 REG_5C – UUID[23:16] (Address 0x5C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[23:16]							

Bits [7:0] - UUID[23:16]

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

5.8 REG_5D – UUID[15:8] (Address 0x5D)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[15:8]							

Bits [7:0] - UUID[15:8]

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

5.9 REG_5E – UUID[7:0] (Address 0x5E)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[7:0]							

Bits [7:0] - UUID[7:0]

R - Readable bit, W - Writeable bit [x] - Value on power-up. '1' - bit is set; '0' - bit is cleared

5.10 DMX registers configuration (Command mode)

The Command mode allows the DMX-controller to access the DMX250 internal registers for write and read operations.

Enter the Command mode by lowering the HDC pin. When the HDC pin is high, the device is in Normal mode.

During Command mode, the DMX250 is in a *Soft-reset* state, TX-FIFO and RX-FIFO are reset and all data in the FIFOs is erased, and the device cannot send or receive a message to/from the powerline.

5.10.1 WRITE-REG command

Write register command consists of three bytes as described in Table 12.

Table 12 - WRITE-REG command structure

1st Byte	2nd Byte	3rd Byte
0xF5	**Control register address**	**Data to write**

1st byte is the write command byte.

2nd byte is the designated control register address to write to.

3rd byte is the data byte value to write.

For example, *writing 0x34 to REG_3 (address 0x03) preformed as follows:*

1. Lower the HDC pin (Enter Command mode).

2. Wait at least 100nsec

3. Transfer 3 bytes: [0xF5][0x03][0x34]

4. The value 0x34 is written to REG_3.

5. Wait for at least 100ns.

6. Raise the HDC pin (Exit Command mode to Normal mode).

5.10.2 READ-REG command

A READ-REG command consists of 2 bytes as described in Table 13.

Table 13 - READ-REG command structure

1st Byte	2nd Byte
0xFD	Control register address

1st byte is the Read command byte.

2nd byte is the designated register address to read from.

Following the second byte, the DMX250 outputs the register value to DMX-controller.

For example, *reading from REG_2 (address 0x02) is performed as follows:*

1. Lower the HDC pin (Enter Command mode).

2. Wait at least 100nsec

3. Transfer 2 bytes: [0xFD][0x02]

4. Wait for the DMX250 to output the value of REG_2.

5. Wait for at least 100ns.

6. Raise the HDC pin (Exit Command mode to Normal mode).

6. Specifications

Table 14 - Absolute maximal rating

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Input voltage, DC	V_{im}		-0.6	3.3	3.9	V
Output voltage, DC	V_{om}		-0.6	3.3	3.9	V
Ambient temperature	T_{am}		-40		125	°C
Storage temperature	T_{sm}		-55		150	°C

Table 15 - Recommended operation conditions

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DVCC} V_{AVCC}		3.0	3.3	3.6	V
Supply Voltage ripple	V_{CC_RIP} A_{VCC_RIP}	Max 2.5MHz, waveform type of triangular		50m		V-p-p
Ambient operating temperature range	T_A		-40		105	°C
Minimum high-level input voltage	V_{IH}		2			V
Maximum low-level input voltage	V_{IL}				0.8	V
Minimum high-level output voltage	V_{OH}		2.4			V
Maximum low-level output voltage	V_{OL}				0.4	V
Maximal output current	I_{out}	see Table 1				
Maximum input current	I_{IN}		-1		1	µA

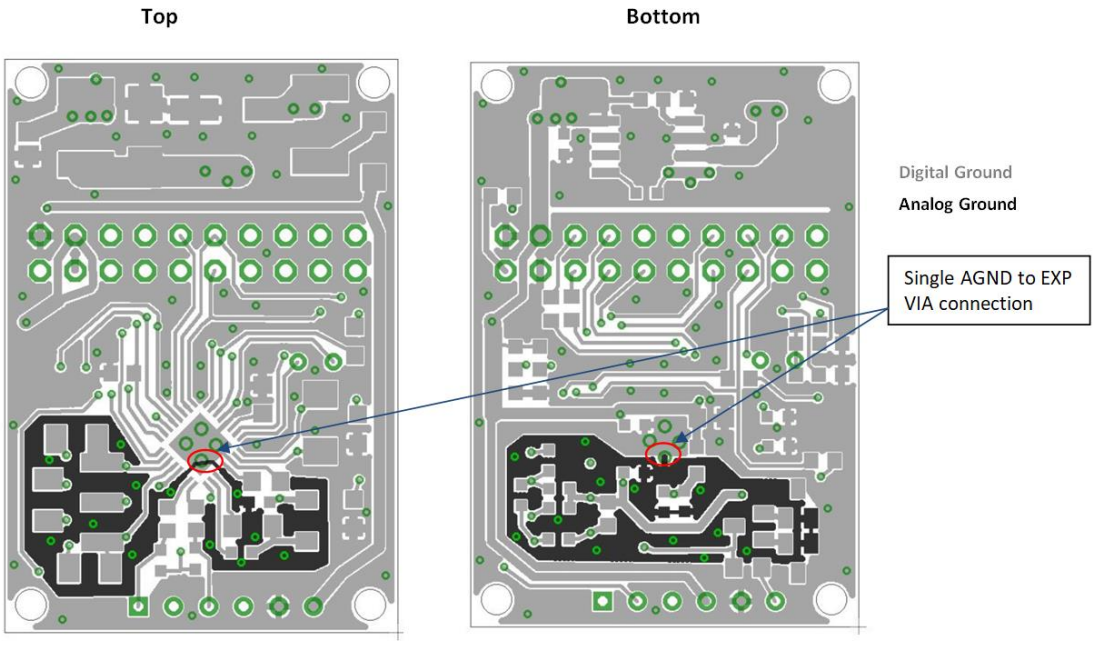
Table 16 - Device characteristics

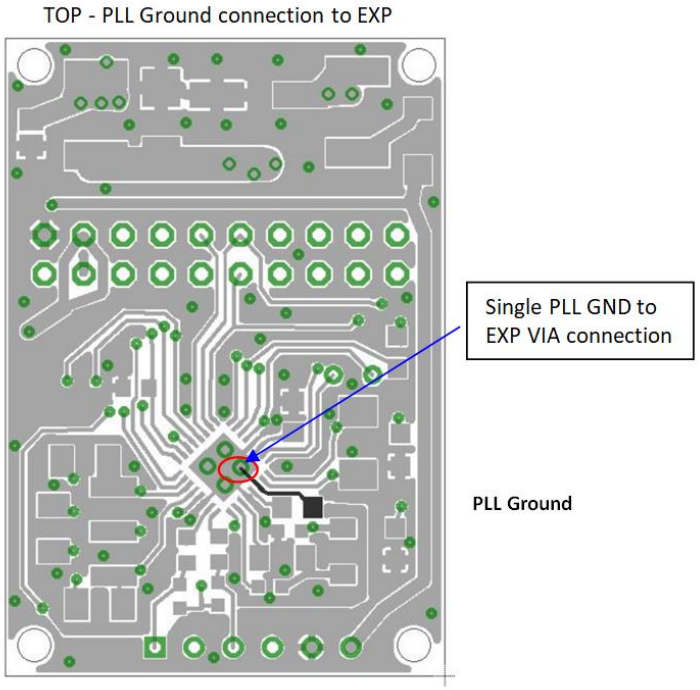
Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
External components requierments						
Powerline coupling capacitor	$C_{coupling}$	Capacitor rate should be selected with respect to powerline voltage		2.2		nF
Protection diodes capacitance	D_{protec}			10		pF
Capacitor at VCAP	V_{cap}		1	4.7		µF
Capacitor at PLLCAP	PLL_{cap}		1			µF
Capacitor at VREF	$VREF_{cap}$		1			µF
Inductor at L1	L1	see 2.5.4		3.3 / 18		µH
Inductor at L2	L2			15		µH
L1 pin input capacitance					1	pF
Crystal frequency	$Xtal_{\_freq}$	see2.5.3		16		MHz
Crystal frequency tolerance	$Xtal_{\_ppm}$				50	±ppm
AC signals characteristics						
Tx signal at TXO	TXO_{lev_1}	TXON high (transmission is active) see 2.5.6.		1		V-p-p
	TXO_{lev_2}			2		V-p-p
TXO input impedance	TXO_{In}	TXON low (transmission is not active)	5.3k			Ω
TXO output impedance	TXO_{out}	TXON high (transmission is active)		18		Ω
TXO driving strength	I_{TXO}	TXON high (transmission is active)	33		66	mA
Rx signal at RXI	RXI_{lev}		10m		3.3	V-p-p
RXI input impedance	RXI_{In}	An external 5.1kΩ series resistor to RXI pin must be installed.	5.1k			Ω
Carrier Frequency in-band	F_c	Selectionresolutionis	5		30	MHz

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
(channels selection)		100kHz, a total of 251 carrier frequencies, see 3.4				
Adjacent channels spacing	F_{adj}	The space between two adjacent channels operating over the same powerline.	1.5			MHz
Timing requierments of DMX/RDM prtocol interface						
DMX bitrate	T_{bit}	Output on HDO		4		µs
Break signal	T_{break}			200		µs
MAB	T_{mab}			20		µs
Stop bit length	T_{sb}			8		µs
Timing of device operation modes						
Power-cycle/ hard-reset	T_{init}	Initialization time after power-cycle or hard-reset event.		2		ms
Carrier frequency setting	T_{freq_cng}	Carreri frequnecy change process time		1		ms
Current Consumtption @ 3.3V						
Normal TX mode – low power	I_{Tx_lp}	TXON high (transmission is active)		77		mA
Normal TX mode – high power	I_{Tx_hp}			95		mA
Normal RX mode	I_{RX}	TXON low (transmission is not active)		46		mA
Enhanced sleep (SLP1)	I_{slp1}	see 4.3		120		µA
Fast wake-up (SLP2)	I_{slp2}	see 4.3		1000		µA
Low-power (SLP3)	I_{slp3}	see 4.3		85		µA
Deep Sleep (SLP4)	I_{slp4}	see 4.3		65		µA

7. DMX250 PCB layout recommendation

Note: Analog ground layer and GND PLL should be connected to the digital ground near the Exp pad.



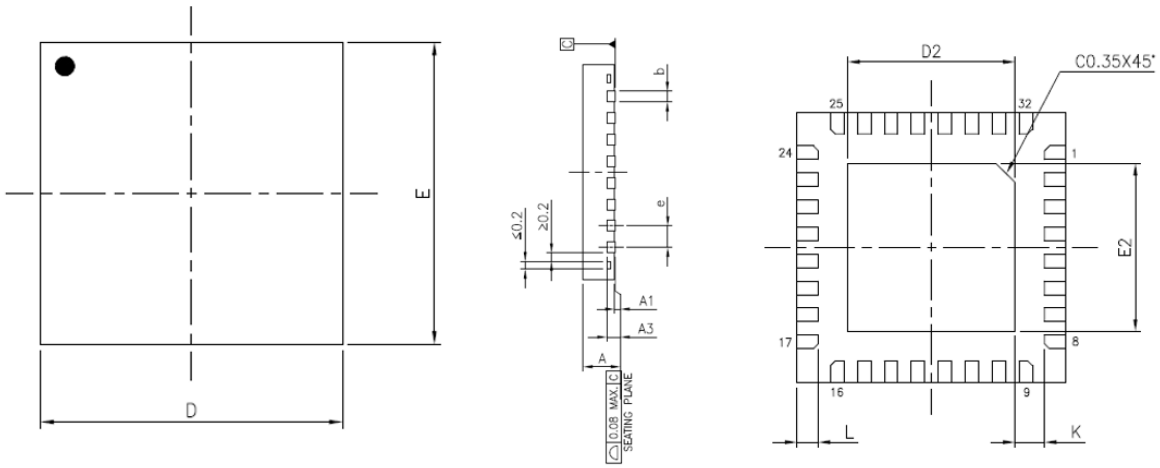


- ✓ VCC and DGND layout traces should be as wide as possible. Connect a 0.1uF capacitor between each VCC and DGND pins, as close as possible to the pins.
- ✓ It is recommended to keep the traces connecting the 3.3V power supply to VCC pins as short as possible with wide PCB traces.
- ✓ Connect AGND to EXP with a single short trace.
- ✓ Connect PLL_GND to EXP with a single short trace.
- ✓ Connect L1, L2, C13, C3, C5, C7, C8, C11, and C12 as close as possible to their pins.
- ✓ Connect R1 as close as possible to the RXI pin.
- ✓ Connect all filtering caps as close as possible to their pins.
- ✓ Connect crystal and its capacitors close to OSCI and OSCO pins. Keep DGND plan around them.

8. Package, Mechanical

The device package is QFN 32 5mm x 5mm.

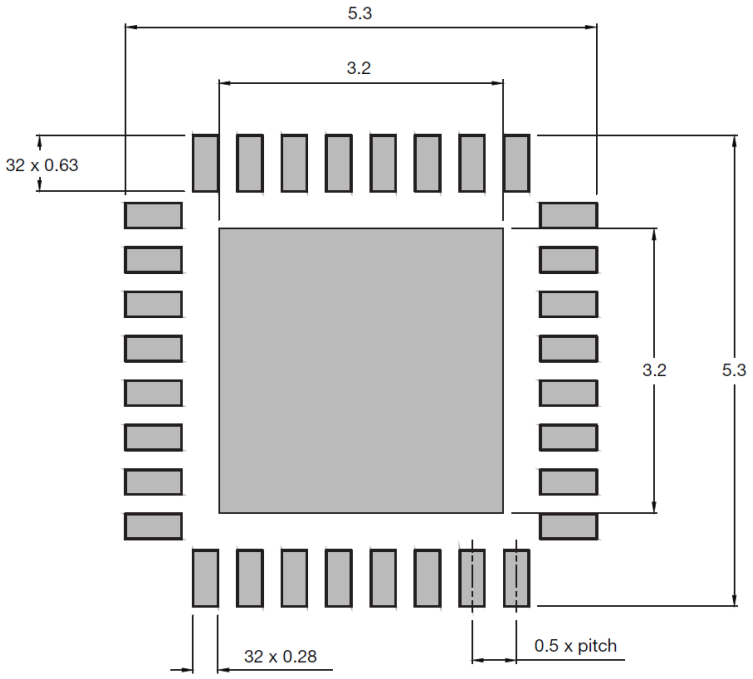
8.1 Mechanical Drawing



D2			E2		
MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
3.15	3.20	3.25	3.15	3.20	3.25

SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.18	0.25	0.30
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
K	0.20	—	—

8.2 PCB drawing



8.3 Soldering profile

Soldering reflow profile is according to IPC/JEDEC J-STD-020 (MSL3).

- The peak temperature (TP) is 260°C.
- Holding time is between 60 sec to 120 sec between TH min 150°C to TH max 200°C.
- Liquidus temperature (TL) is 217 °C. Liquidus time is between 60 sec to 150 sec.
- TL to TP max ramp-up is 3°C/sec.
- TP to TL max cooldown rate is 6°C/sec.
- Max time above 255°C (Tp) is 30 sec.

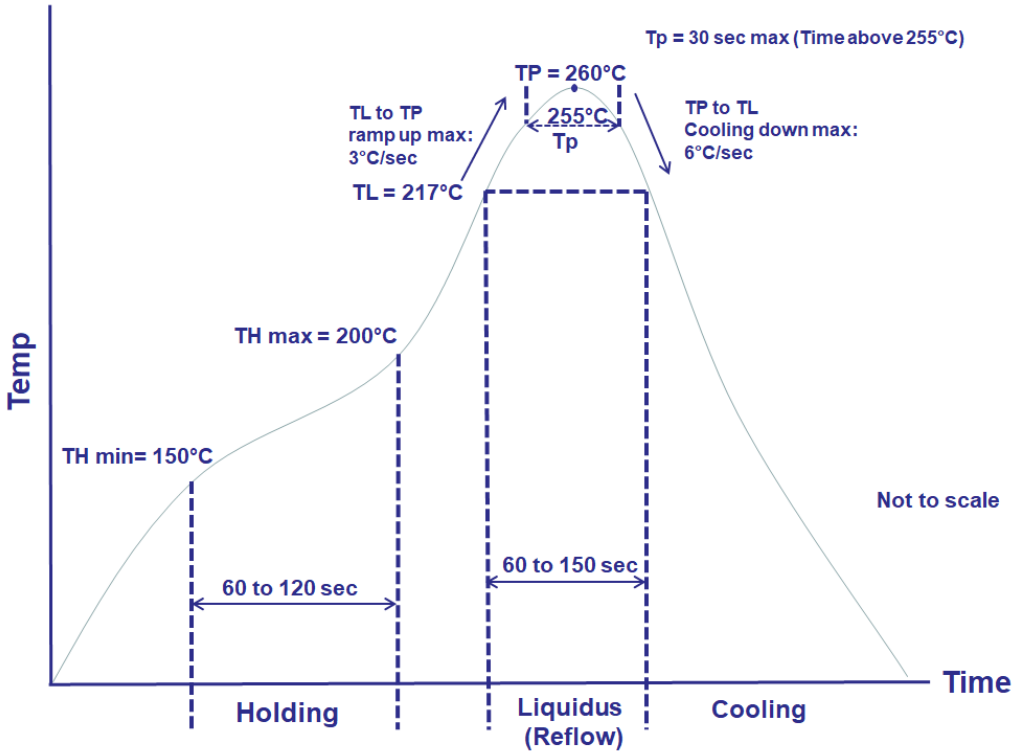


Figure 18 – Representation of IPC/JEDEC J-STD-020 (MSL3) profile

9. Test Environment

Figure 19 depicts a typical DC-BUS Test environment that allows testing the DMX250 devices in an emulated lab DC powerline environment.

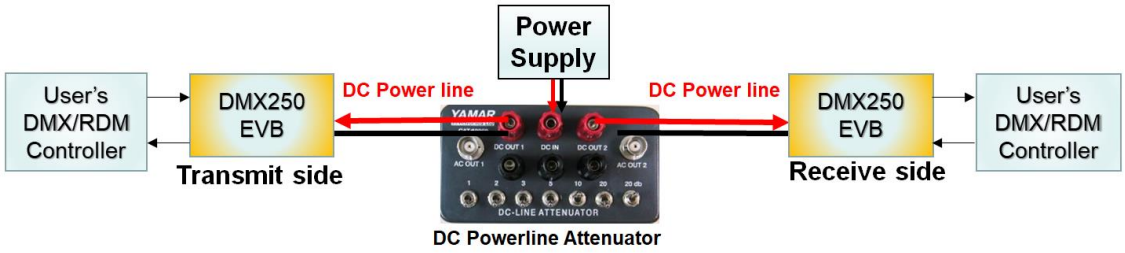


Figure 19 - DC-BUS Test environment

This test environment consists of two DMX250 evaluation boards (EVB), and two users' DMX-controllers. The DC-powerline attenuator is optional.

The DC-powerline attenuator is used to test the communication in variable attenuation levels (0-61dB), emulating a DC powerline environment. When connecting the EVB directly to a power supply, it is recommended to add in serial to the power supply an inductor (>22uH) to avoid strong attenuation due to the power supply input filtering capacitors.

Revision History

Rev.	Date	Description
0.73	11/09/2019	Initial preliminary revision.
0.74	02/10/2019	Update Table 2 and Figure 7.
0.75	14/11/2019	Update Figure 4 and NSLEEP pin description.
0.76	19/01/2020	Update Table 2.
0.77	18/02/2020	Update clause 2.5.3.1. Add UUID clause 3.5. Update clause 5 with UUID REGs. Add soldering profile description in section 8.3
0.78	01/08/2020	Update 2.5.3.1, 2.5.5, and Table 16.
0.79	12/01/2021	Editing.
0.80	16/01/2022	Update Table 2.