

Questa® Advanced Simulator

Questa's core simulation and debug engine

The Questa® Advanced Simulator combines high performance and capacity simulation with unified advanced debug and functional coverage capabilities for the most complete native support of Verilog, SystemVerilog, VHDL, SystemC, SVA, UPF and UVM.

The Questa Advanced Simulator is the core simulation and debug engine of the Questa Verification Solution; the comprehensive advanced verification platform capable of reducing the risk of validating complex FPGA and SoC designs.

Questa spans the levels of abstraction required for complex SoC and FPGA design and verification from TLM (Transaction Level Modeling) through RTL, gates, and transistors and has superior support of multiple verification methodologies including Assertion Based Verification (ABV), the Open Verification Methodology (OVM) and the Universal Verification Methodology (UVM) to increase testbench productivity, automation and reusability.

[Breaking the Speed Limits on SoC Verification with the Questa Flow](#)

[On-demand Web Seminar](#)

Learn best practice in verification flows in the industry today, and how to implement the optimal flow to speed your SoC design verification cycle.