Signetics

74LS197
Counter

Presettable 4-Bit Binary Ripple Counter
Product Specification

Logic Products

FEATURES

- **High speed 4-bit binary counting**
- **Asynchronous parallel load for presetting counter**
- **Overriding Master Reset**
- **Buffered Q_0 output drives $\overline{CP}_1$ input plus standard fan-out**

DESCRIPTION

The '197 is an asynchronously presettable binary ripple counter partitioned into divide-by-2 and divide-by-8 sections with each section having a separate Clock input. Stage changes are initiated in the counting modes by the HIGH-to-LOW transition of the Clock inputs, however, state changes of the Q outputs do not occur simultaneously because of the internal ripple delays. Designers should keep in mind when using external logic to decode the Q outputs, that the unequal delays can lead to decoding spikes, and thus a decoded signal should not be used as a strobe or clock. The Q_0 flip-flop is triggered by the $\overline{CP}_0$ input while the $\overline{CP}_1$ input triggers the divide-by-8 section.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74LS197	40MHz	16mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS197N
Plastic SO-14	N74LS197D

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

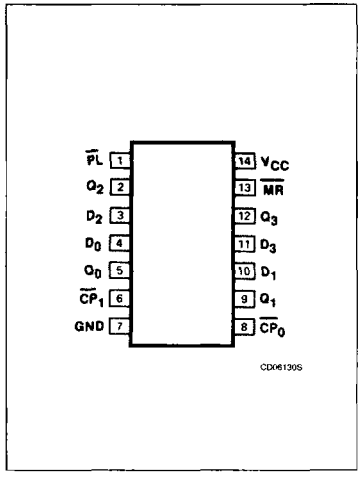
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
$\overline{CP}_0$	Clock input	6LSul
$\overline{CP}_1$	Clock input	3.5LSul
All	Other inputs	1LSul
$Q_0 - Q_3$	Outputs	10LSul

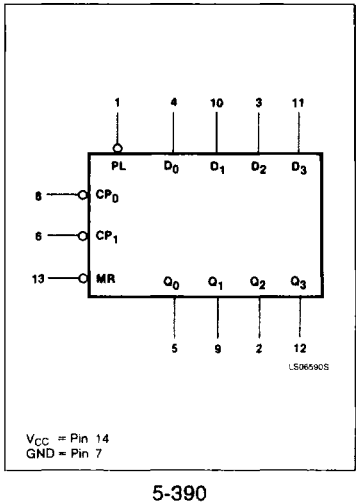
NOTE:
Where a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

The device has an asynchronous active-LOW Master Reset ($\overline{MR}$) input which overrides all other inputs and forces all outputs LOW. The counter is also asynchronously presettable. A LOW on the Parallel Load ($\overline{PL}$) input overrides the Clock inputs and loads the data from parallel Data ($D_0 - D_3$) inputs into the flip-flops. The counter acts as a transparent latch while the $\overline{PL}$ is LOW and any change in the D_n inputs will be reflected in the outputs.

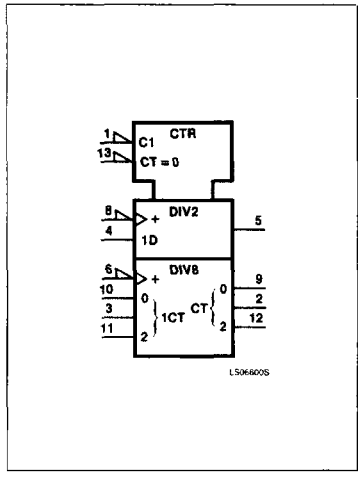
PIN CONFIGURATION



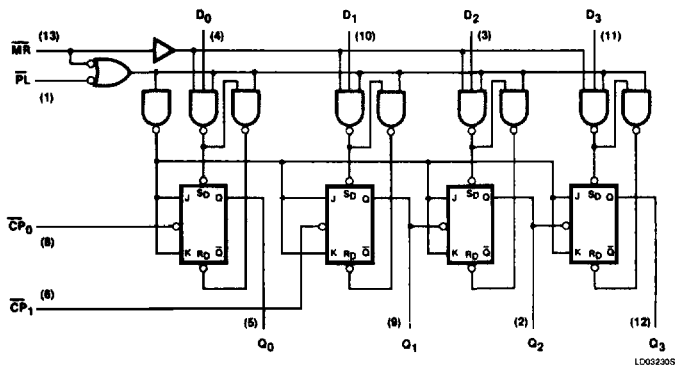
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



( ) = Pin numbers
V_{CC} = Pin 14
GND = Pin 7

COUNT SEQUENCE

COUNT	4-BIT BINARY[1]			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	L	L	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE:
1. Q_0 connected to input $\overline{CP}_1$; input applied to $\overline{CP}_0$.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUT
	$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	D_n	Q_n
Reset (clear)	L	X	X	X	L
Parallel load	H	L	X	L	L
	H	L	X	H	H
Count	H	H	↓	X	count

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↓ = HIGH-to-LOW clock transition

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−400	μA
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74LS197			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX		0.35	0.5	V
			I_{OL} = 4mA (74LS)		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V	$D_0 - D_3$, $\overline{PL}$			0.1	mA
			$\overline{MR}$, $\overline{CP}_0$, $\overline{CP}_1$			0.2	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V	$D_0 - D_3$, $\overline{PL}$			20	μA
			$\overline{MR}$, $\overline{CP}_0$, $\overline{CP}_1$			40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	$D_0 - D_3$, $\overline{PL}$			−0.4	mA
			$\overline{MR}$ input			−0.8	mA
			$\overline{CP}_0$ input			−2.4	mA
			$\overline{CP}_1$ input			−1.3	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			16	27	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

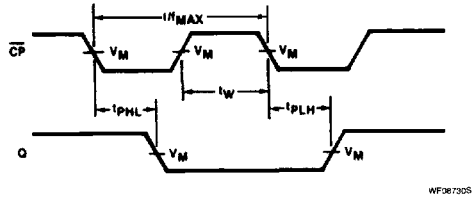
PARAMETER		TEST CONDITIONS		74LS		UNIT
				C_L = 15pF, R_L = 2kΩ		
				Min	Max	
f_{MAX}	Maximum count frequency	Waveform 1	$\overline{CP}_0$	30		MHz
			$\overline{CP}_1$	15		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ to Q_0	Waveform 1			15 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_1	Waveform 1			19 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_2	Waveform 1			51 63	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_3	Waveform 1			78 95	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2			27 44	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to output	Waveform 3			39 45	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 4			51	ns

NOTE:
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

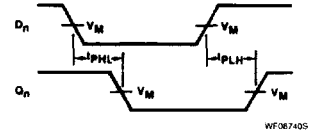
AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS		74LS Min	74LS Max	UNIT
t_W	Clock pulse width	Waveform 1	$\overline{CP}_0$	20		ns
			$\overline{CP}_1$	30		ns
t_W	$\overline{MR}$ pulse width	Waveform 4		15		ns
t_W	$\overline{PL}$ pulse width	Waveform 3		20		ns
$t_s(H)$	Set-up time HIGH data to $\overline{PL}$	Waveform 5		10		ns
$t_h(H)$	Hold time HIGH data to $\overline{PL}$	Waveform 5		20		ns
$t_s(L)$	Set-up time LOW data to $\overline{PL}$	Waveform 5		15		ns
$t_h(L)$	Hold time LOW data to $\overline{PL}$	Waveform 5		20		ns
t_{rec}	Recovery time $\overline{MR}$ to $\overline{CP}$	Waveform 4		30		ns
t_{rec}	Recovery time $\overline{PL}$ to $\overline{CP}$	Waveform 3		30		ns

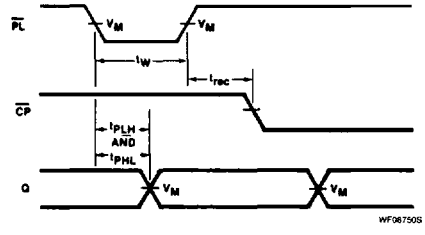
AC WAVEFORMS



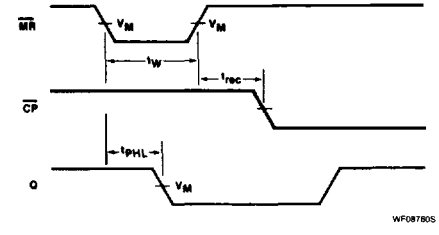
Waveform 1. Clock To Output Delays And Clock Pulse Width



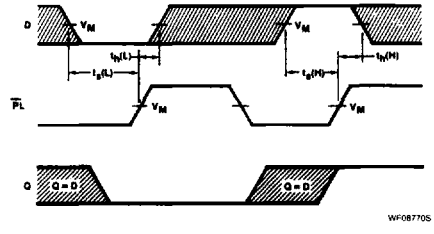
Waveform 2. Parallel Data To Output Delays



Waveform 3. Parallel Load Pulse Width, Parallel Load To Output Delay And Parallel Load To Clock Recovery Time



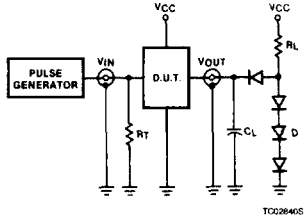
Waveform 4. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time

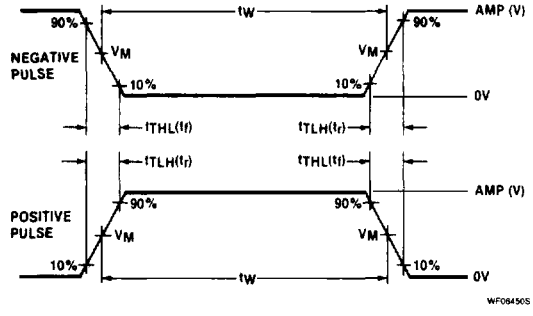


For all waveforms, $V_M = 1.5V$ for 74 and 74S; $V_M = 1.3V$ for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 5. Data Set-up And Hold Times

TEST CIRCUITS AND WAVEFORMS





V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns