LOW VOLTAGE VIDEO AMPLIFIER WITH LPF

■FEATURES

- ●Operating Voltage 2.8 to 5.5V
- ●6th Order LPF -33dB at 19MHz
- ●6dB Amp. , 75Ω Driver
- ●Power Save Circuit
- ●Bipolar Technology
- ●Package Outline SOT-23-6-1,DFN6-G1 (ESON6-G1)

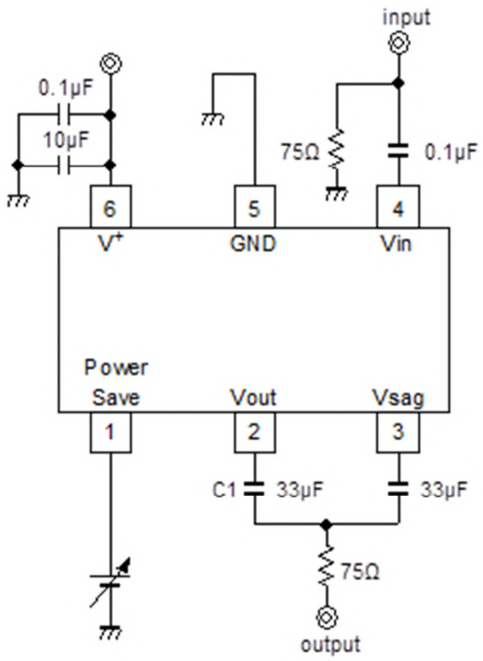
■GENERAL DESCRIPTION

The NJM2561 is a Low Voltage Video Amplifier contained LPF circuit. Internal 75Ω driver is easy to connect TV monitor directly. The NJM2561 features low power and small package, and is suitable for low power design on downsizing of Car camera and CCTV.

■APPLICATION

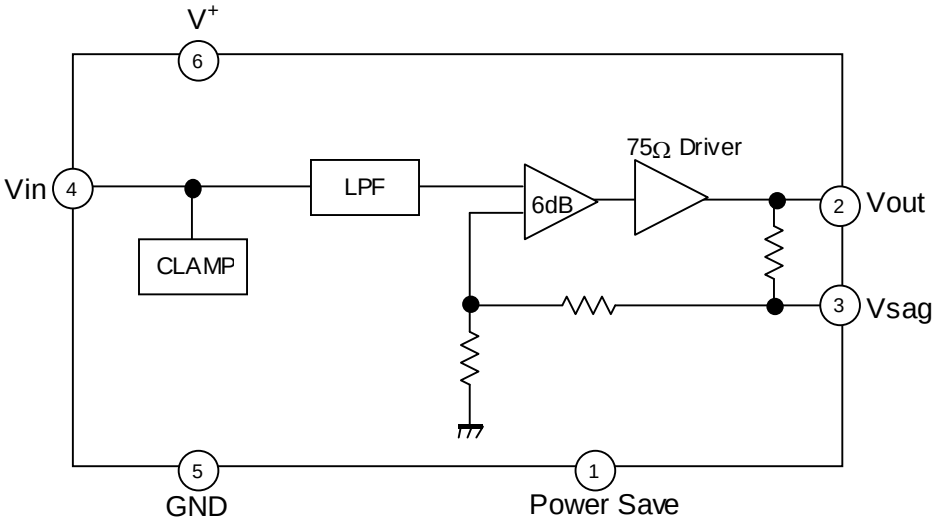
- ●Car Camera
- ●Car Navigation
- ●CCTV

■APPLICATION CIRCUIT



■EQUIVALENT CIRCUIT・BLOCK DIAGRAM

(Pin Number: SOT-23-6-1)



■**Voltage Gain Valuation**

Voltage Gain	Part No.
6.0dB	NJM2561B
12.4dB	NJM2562
16.5dB	NJM2563
9.0dB	NJM2571A

■**Supply Voltage Valuation**

Supply Voltage	Part No.
2.6 to 5.5V	NJM2561A

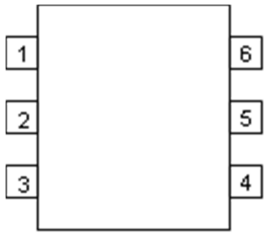
■**Output DC - coupling Valuation**

Supply Voltage	Part No.
2.8 to 5.5V	NJM2561B
2.8 to 5.5V	NJM2561F1A (Screening product)
4.5 to 5.5V	NJM41031

■**Operating Temperature Range Valuation**

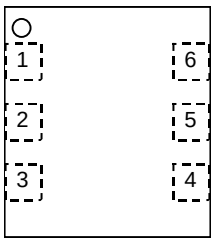
Operating Temperature Range	Part No.
-40 to 105°C	NJM2561F1-T

■**PIN CONFIGURATION (SOT-23-6-1)**



PIN NO.	SYMBOL	DESCRIPTION
1	Power Save	Power Save Terminal
2	Vout	Video Signal Output Terminal
3	Vsag	SAG correction Terminal
4	Vin	Video Signal Input Terminal
5	GND	GND Terminal
6	V+	Power Supply Terminal

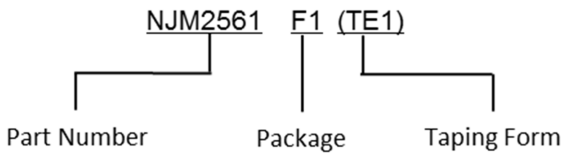
■**PIN CONFIGURATION (DFN6-G1 Top view)**



PIN NO.	SYMBOL	DESCRIPTION
1	Vsag	SAG correction Terminal
2	GND	GND Terminal
3	Power save	Power Save Terminal
4	V+	Power Supply Terminal
5	Vout	Video Signal Output Terminal
6	Vin	Video Signal Input Terminal

■**MARK INFORMATION**

●SOT-23-6-1



●DFN6-G1

■ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ(pcs)
NJM2561F1	SOT-23-6-1	YES	YES	Sn-2Bi	A4	15.0	3,000
NJM2561KG1	DFN6-G1	YES	YES	Sn-2Bi	2561	3.5	3,000

■ABSOLUTE MAXIMUM RATINGS

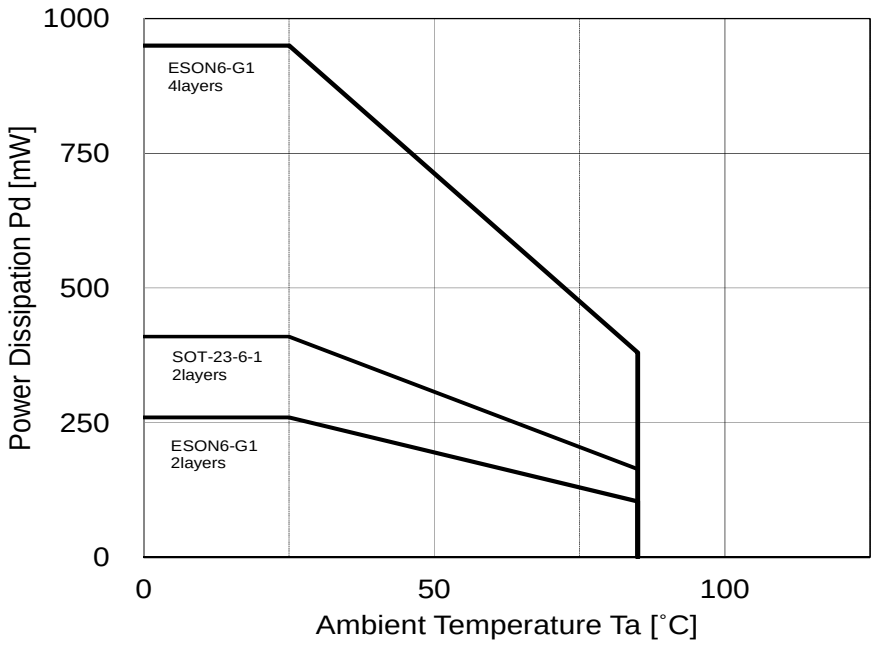
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V+	7.0	V
Power Dissipation (Ta=25°C)(4)	P_D	SOT-23-6-1: 410 (1) DFN6-G1: 260(2) DFN6-G1: 950(3)	mW
Operating Temperature Range	T_{opr}	-40 to 85	°C
Storage Temperature Range	T_{stg}	-40 to 125	°C

(1) At on a board of EIA/JEDEC specification. (114.3 x 76.2 x 1.6mm 2 layers, FR-4)
(2) At on a board of EIA/JEDEC specification. (101.5 x 114.5 x 1.6mm 2 layers, FR-4)
(3) At on a board of EIA/JEDEC specification. (101.5 x 114.5 x 1.6mm 4 layers, FR-4)

■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V+	2.8 to 5.5	V

■POWER DISSIPATION vs. AMBIENT TEMPERATURE



■**ELECTRICAL CHARACTERISTICS** (V^+=3.0V,R_L=150Ω,Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	No Signal	-	8.0	12.0	mA
Operating Current at Power Save	Isave	No Signal, Power Save Mode	-	30	50	μA
Maximum Output Voltage Swing	Vom	f=100kHz,THD=1%	2.2	2.5	-	Vp-p
Voltage Gain	Gv	Vin=100kHz, 1.0Vp-p, Input Sine Signal	6.1	6.5	6.9	dB
Low Pass Filter Characteristic	Gfy4.5M	Vin=4.5MHz/100kHz, 1.0Vpp	-0.6	-0.1	0.4	dB
	Gfy19M	Vin=19MHz/100kHz, 1.0Vpp	-	-33	-23	
Differential Gain	DG	Vin=1.0Vp-p, 10step Video Signal	-	0.5	-	%
Differential Phase	DP	Vin=1.0Vp-p, 10step Video Signal	-	0.5	-	deg
S/N Ratio	SNv	Vin=1.0Vp-p, R_L=75Ω 100% White Video Signal, 100KHz to 6MHz	-	+60	-	dB
2nd. Distortion	Hv	Vin=1.0Vp-p, 3.58MHz, Sine Signal, R_L=75Ω	-	-50	-	dB
SW Change Voltage High Level	VthPH	Active	1.8	-	V^+	V
SW Change Voltage Low Level	VthPL	Non-active	0	-	0.3	

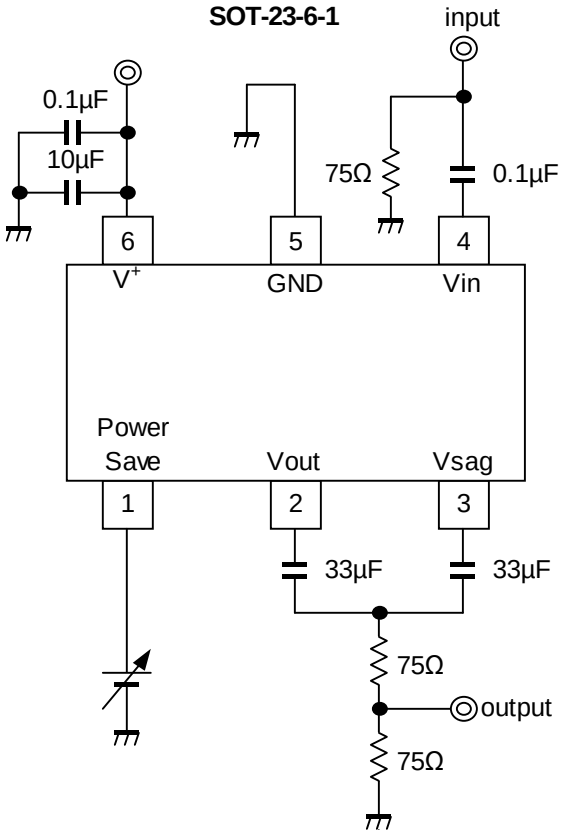
Note: NJM2561F1A is tested to guarantee enough output dynamic range on V^+=3.3V, 1.5Vp-p input signal for DC-coupling(output capacitor less) video application.

■**CONTROL TERMINAL**

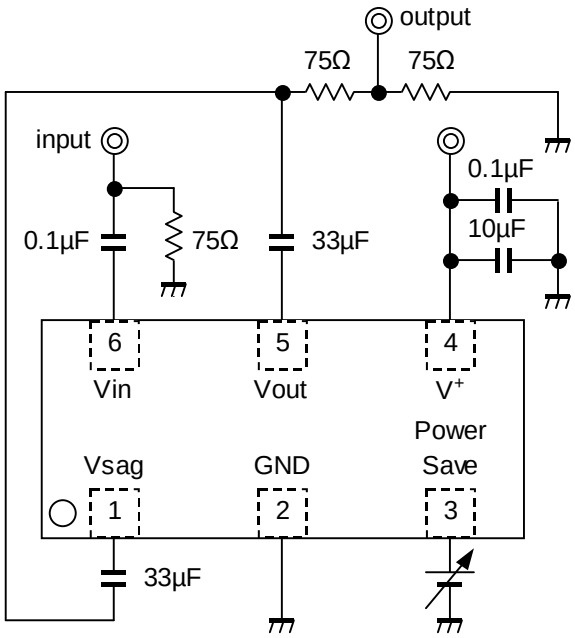
PARAMETER	STATUS	NOTE
Power Save	H	Power Save: OFF (Active)
	L	Power Save: ON (Mute)
	OPEN	Power Save: ON (Mute)

■TEST CIRCUIT

SOT-23-6-1

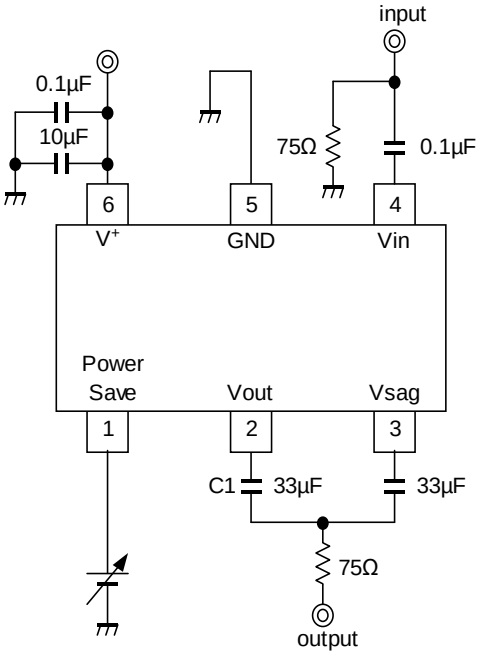


DFN6-G1 (Top View)

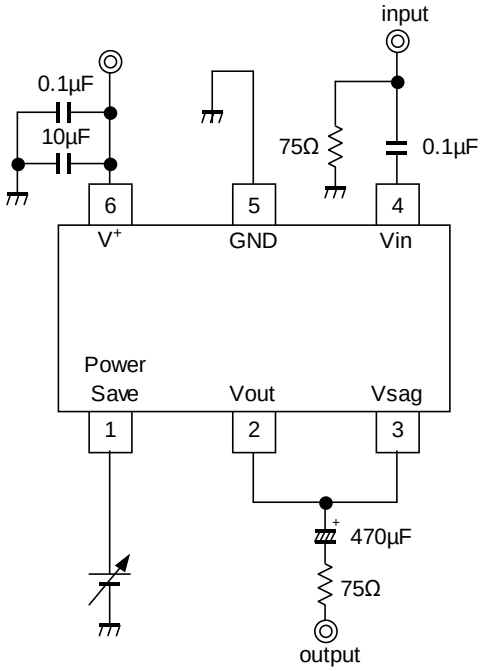


■**APPLICATION CIRCUIT 1**(SOT-23-6-1)

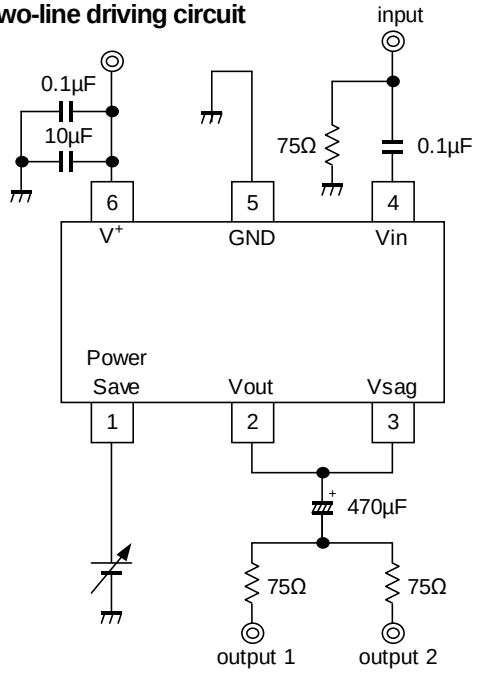
(1) Standard circuit



(2) SAG correction unused circuit



(3) Two-line driving circuit



(1) Standard circuit

This circuit is for a portable equipment of small mounting space.The SAG correction reduces output coupling capacitor values. However, this circuit may cause to SAG deterioration, and lose synchronization by luminance fluctuation. Adjust the C1 value, checking the waveform containing a lot of low frequency components like a bounce waveform (Worst condition waveform of SAG). Change the capacitor of C1 into a large value to improve SAG.

(2) SAG correction unused circuit

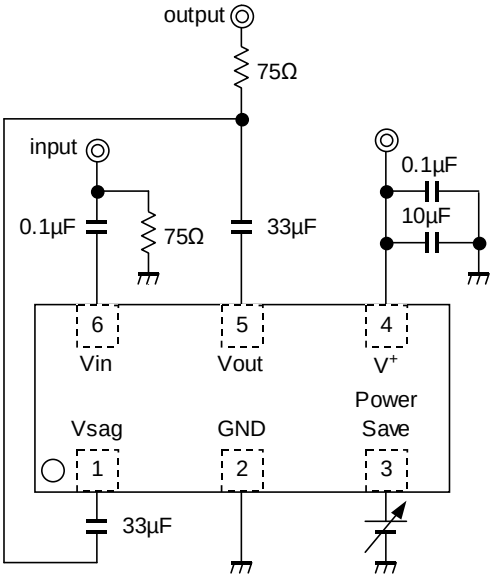
We recommend this circuit when there is no space limitation. Connect the coupling capacitor after connecting the Vout pin and Vsag pin. The recommended value is 470µF or more.

(3) Two-line driving circuit

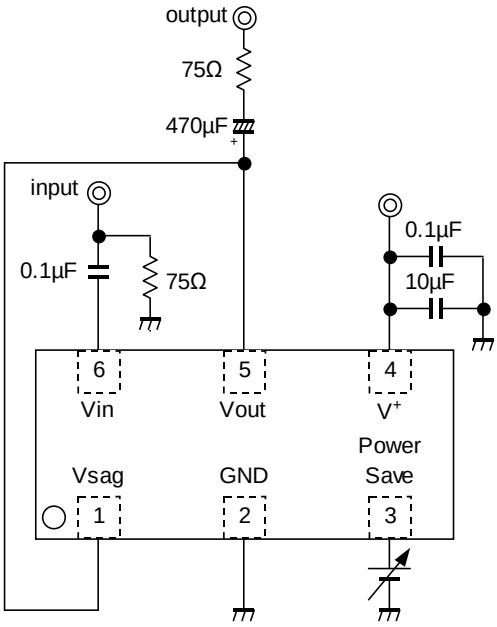
This circuit drives two-line of 150Ω. However, it may cause to lose synchronization by an input signal of large APL change (100% white signals more than 1Vp-p). Confirm the large APL change waveform (100% white signals more than 1Vp-p) and evaluate sufficiently.

■APPLICATION CIRCUIT (DFN6-G1)

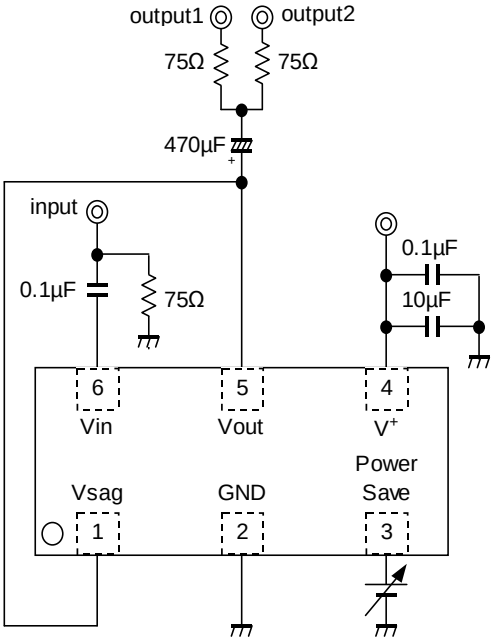
(1) Standard circuit



(2) SAG correction unused circuit



(3) Two-line driving circuit



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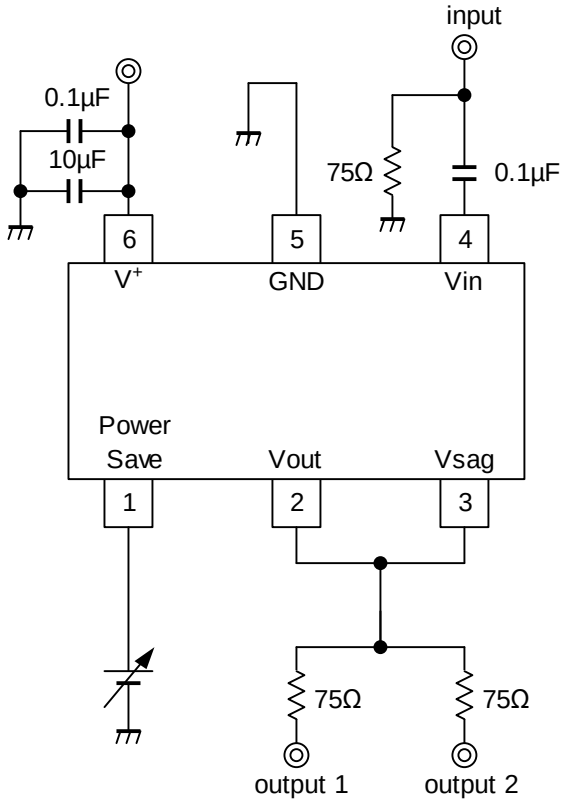
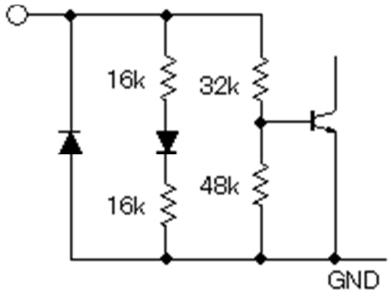
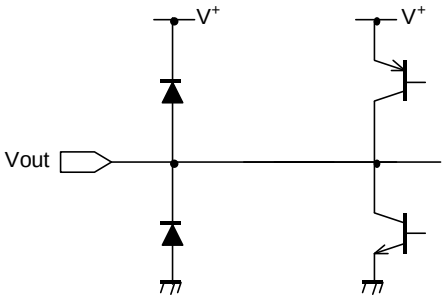
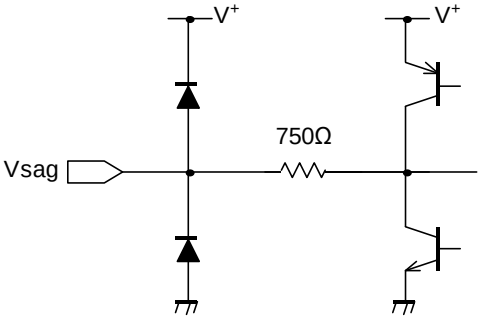
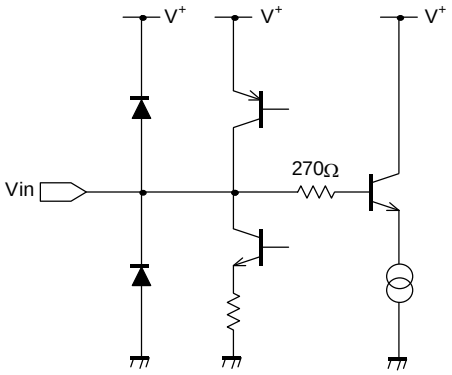
This circuit drives two-line of 150Ω. However, it may cause to lose synchronization by an input signal of large APL change (100% white signals more than 1Vp-p). Confirm the large APL change waveform (100% white signals more than 1Vp-p) and evaluate sufficiently.

■**NJM2561F1A (DC-coupling Screening product) APPLICATION CIRCUIT** (SOT-23-6-1 only)



■TERMINAL DESCRIPTION

PIN.No.		SYMBOL	EQUIVALENT CIRCUIT	DC VOLTAGE
SOT-23-6-1	DFN6-G1			
1	3	Power Save		-
2	5	Vout		0.33V
3	1	Vsag		-
4	6.	Vin		1.1V
5	2	GND	-	-
6	4	V+	-	-

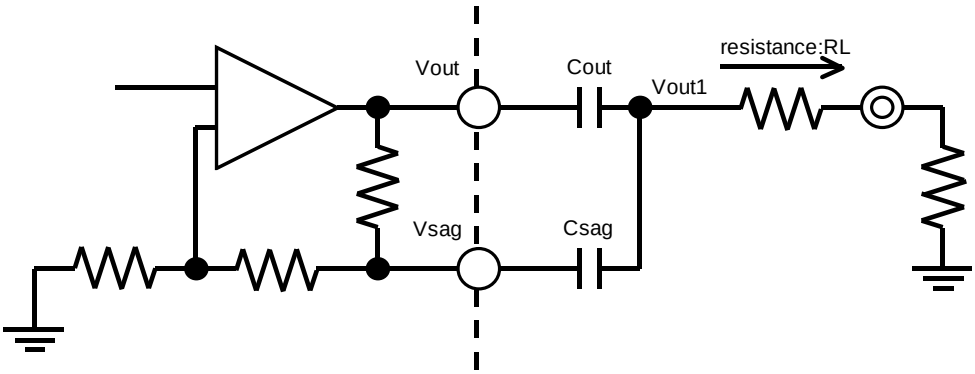
■APPLICATION

●SAG correction circuit

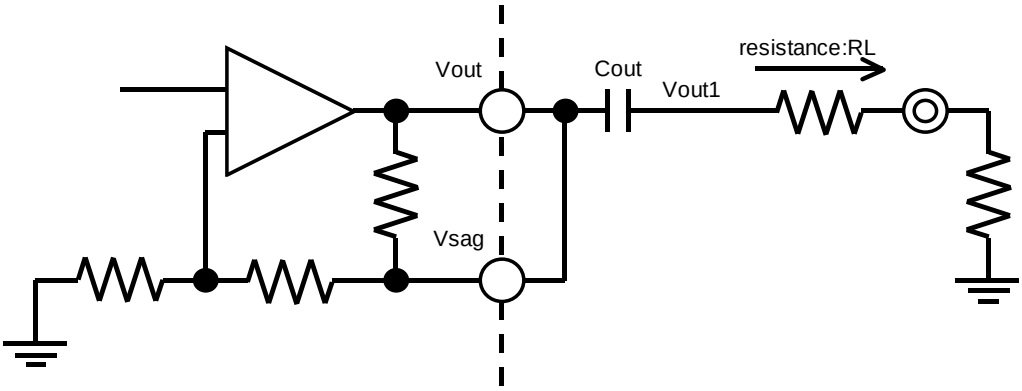
SAG correction circuit is a circuit to correct for low-frequency attenuation by high-pass filter consisting of the output coupling capacitance and load resistance. Low-frequency attenuation raises the sag in the vertical period of the video signal.

Capacitor for Vsag (Csag) is connected to the negative feedback of the amplifier. This Csag increase the low frequency gain to correct for the attenuation of low frequency gain.

Example SAG collection circuit

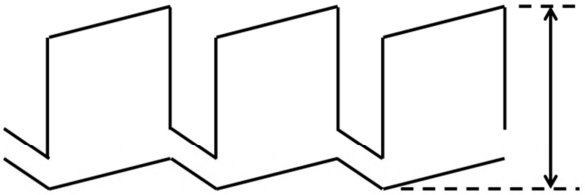


Example of not using sag compensation circuit

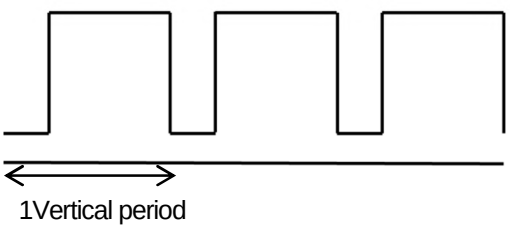


Waveform of Vout terminal and Vout1 terminal

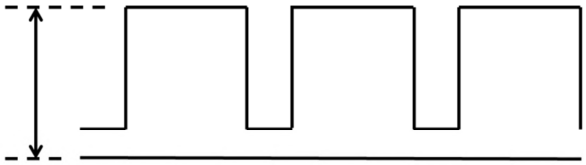
using SAG correction circuit
Waveform of Vout



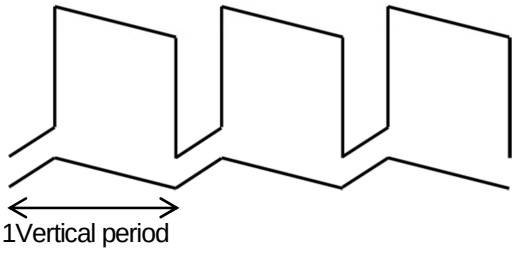
Waveform of Vout1



not using SAG correction circuit
Waveform of Vout



Waveform of Vout1



SAG correction circuit generates a low frequency component signal amplified to Vout terminal.
Changes of the luminance signal will be low-frequency components, if you want to output a large signal luminance changes. Therefore, generate correction signal of change of a luminance signal to Vout pin.
At this time, signal is over the dynamic range of Vout pin. This may cause a lack of sync signal, and waveform distortion.

Please see diagram below (green waveform), if you want to output large changes of a signal luminance, such as 100% white video signal and black signal. Thus, output signal exceed dynamic range of Vout pin and may be the signal lack.

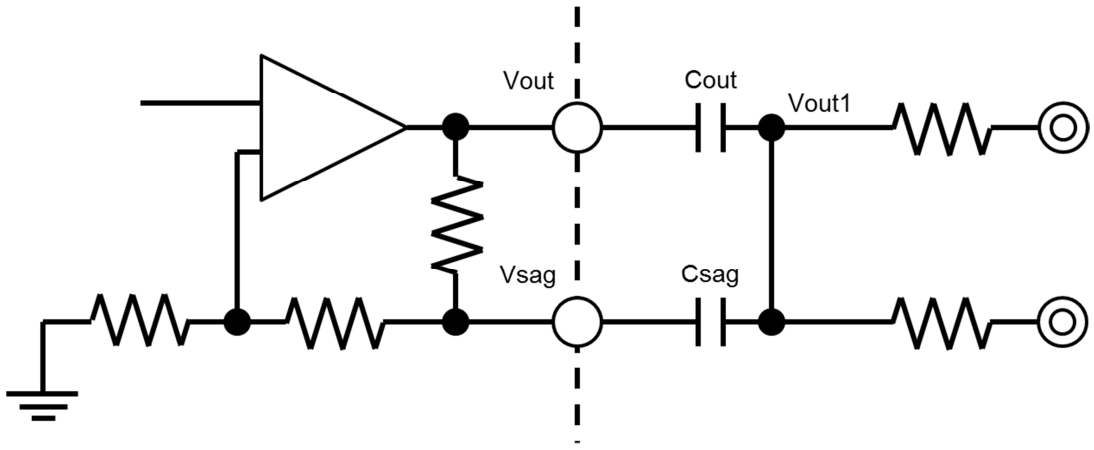
< Countermeasure for waveform distortion >

1. Please using small value the Sag compensation capacitor (VSAG).
It can ensure the dynamic range by using small value the capacitor (VSAG). It because of low-frequency variation of Vout pin is smaller. However, the output (VOUT) must be use large capacitor for this reason sag characteristics become exacerbated.

2. Please do not use the sag correction circuit.
Signal can output within dynamic range for reason it does not change the DC level of the output terminal.
However, the output (VOUT) must be use large capacitor for this reason sag characteristics become exacerbated.

< Dual drive at using SAG correction circuit >

Using sag correction circuit at dual drive circuit is below. Dual drives are less load resistance. Thus, the cut-off frequency of HPF that is composed of the output capacitor and load resistance will be small. Therefore, the sag characteristics deteriorate. Please size up to the output capacitor (Vout) for not to deteriorate the sag characteristics.

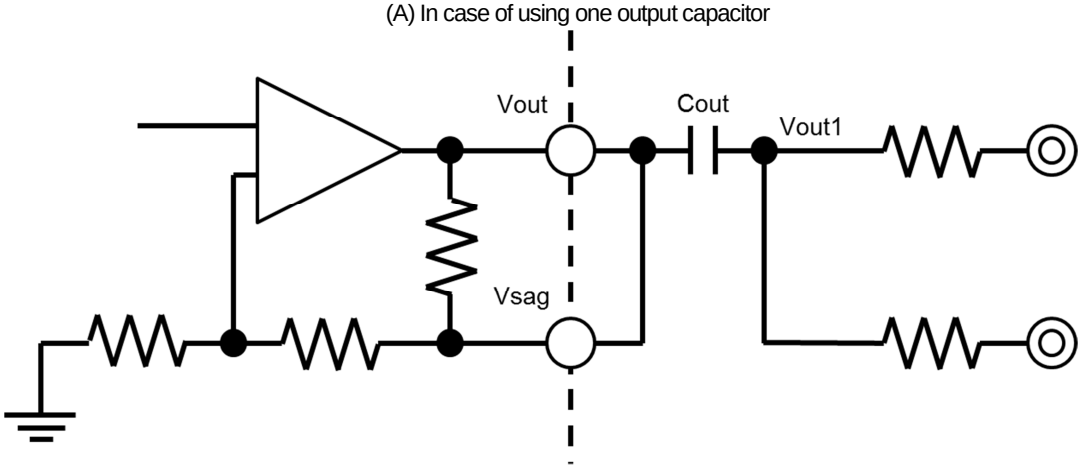


< Dual drive at not using SAG correction circuit >

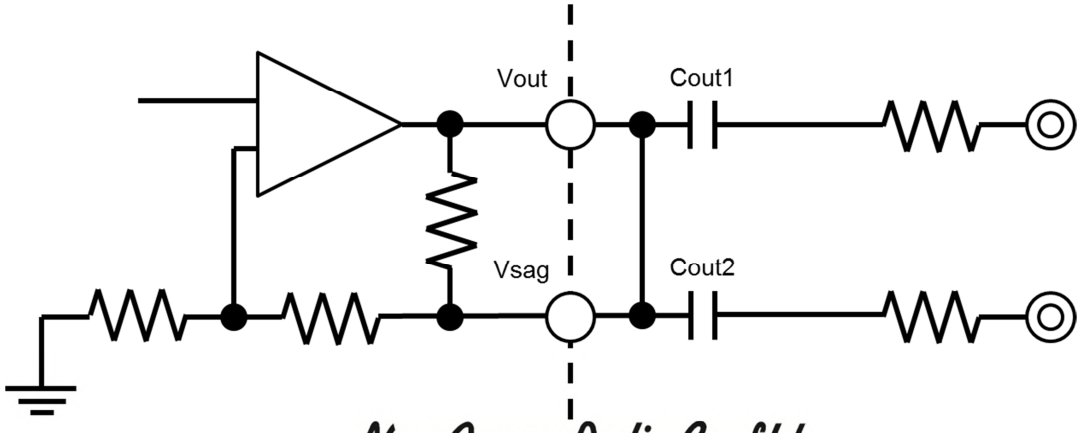
We recommended two-example dual drive circuit with not use sag correction circuit. Please change the configuration to be used according to the situation. Please configure to meet the following conditions. Then you can adjust the characteristics of each configuration.

$$Cout = Cout1 + Cout2$$
$$Cout1 = Cout2$$

(A) In case of using one output capacitor

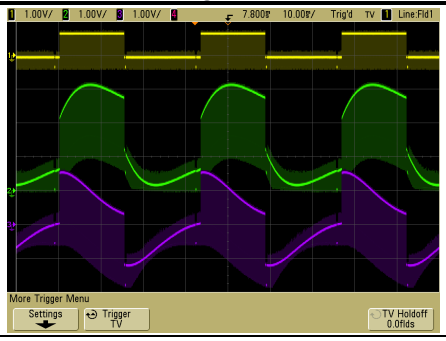
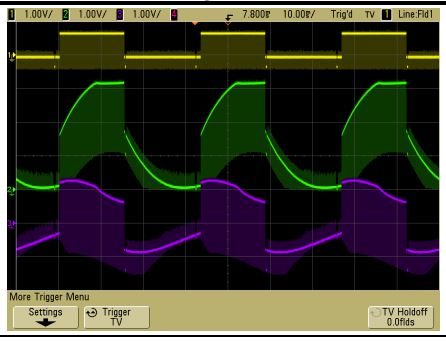
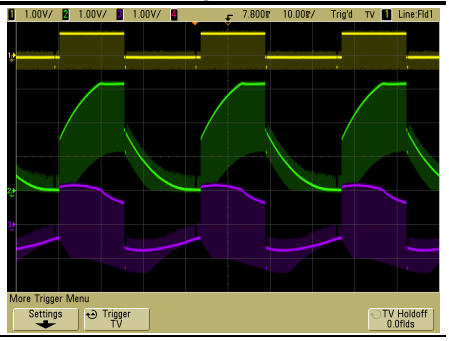
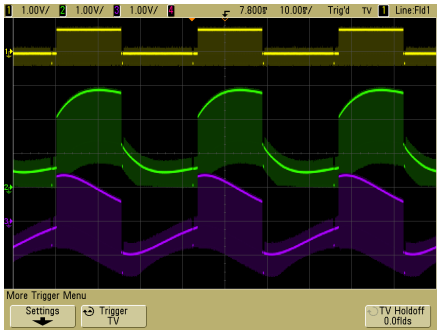
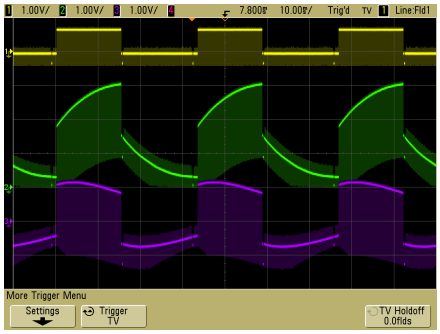
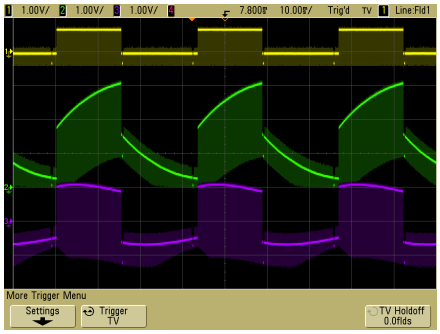
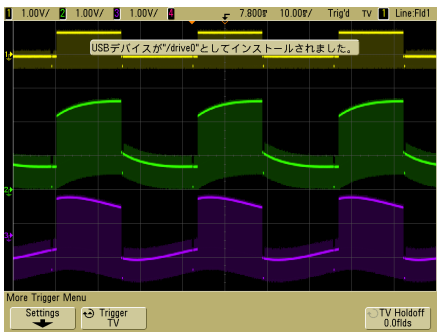
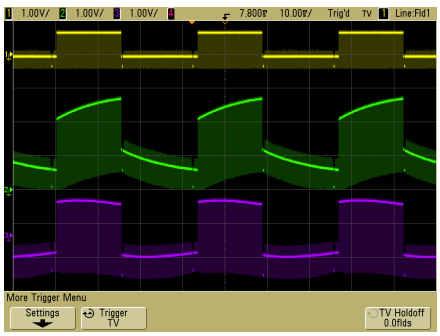
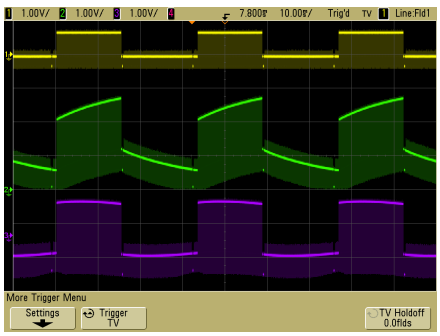
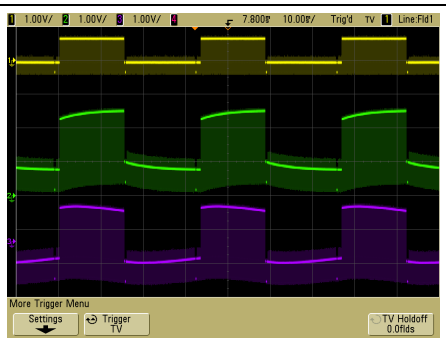
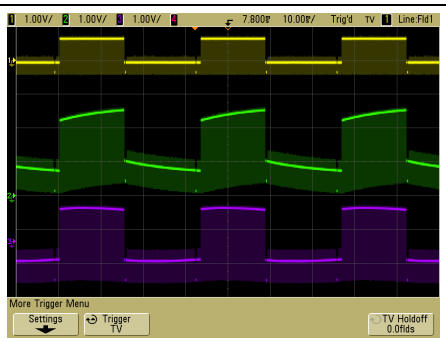
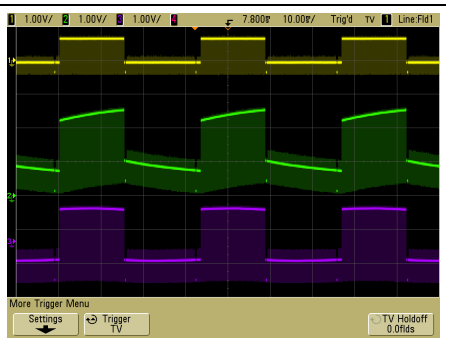
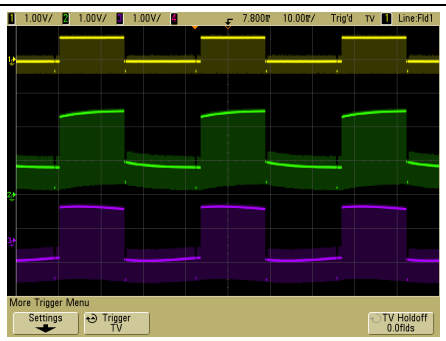
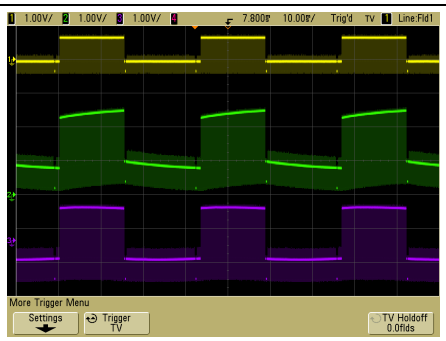
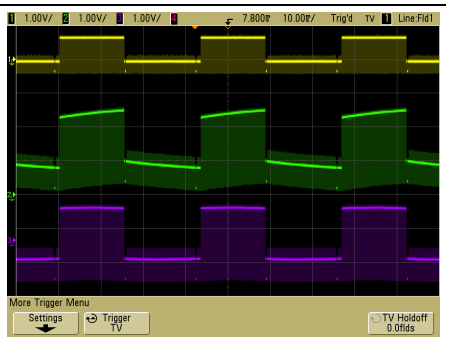


(B) In case of using two output capacitors

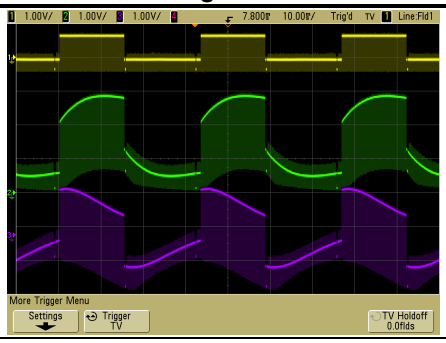
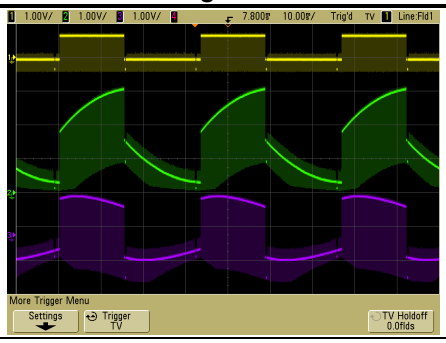
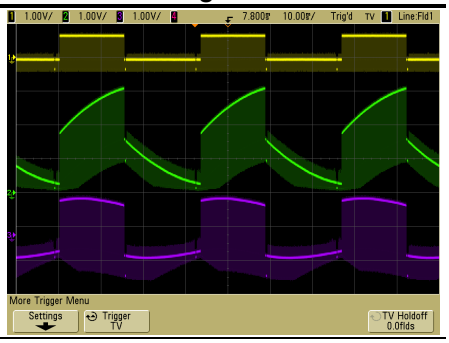
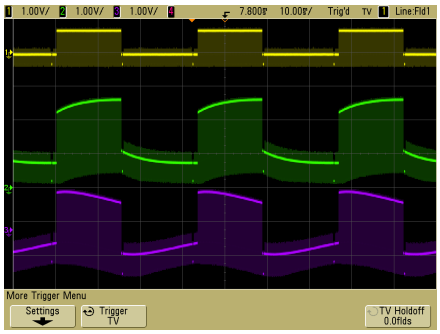
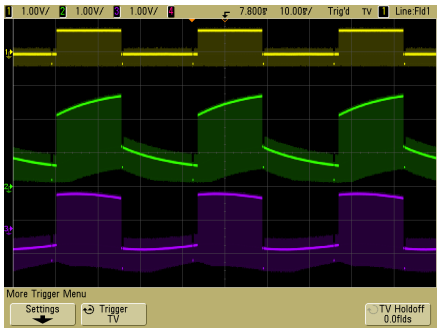
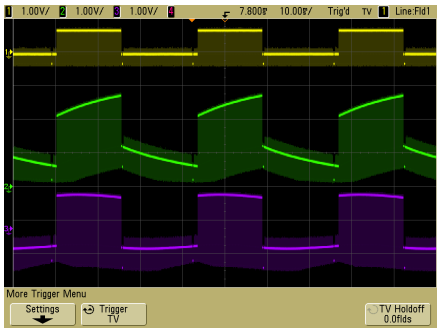
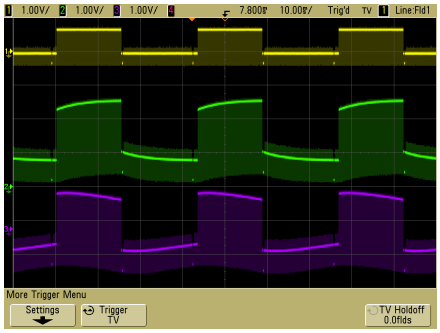
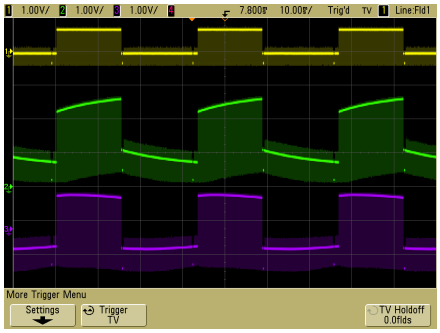
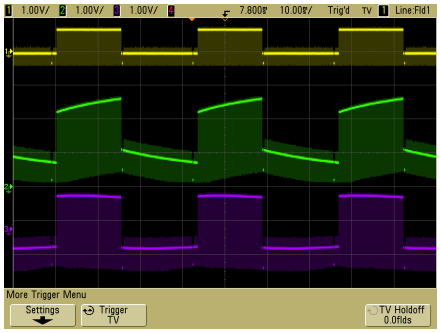
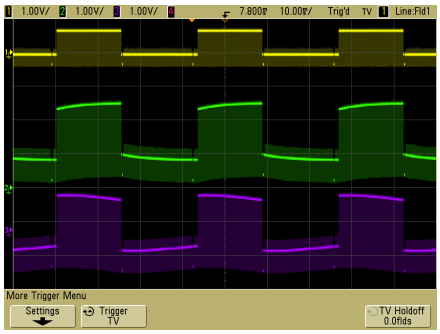
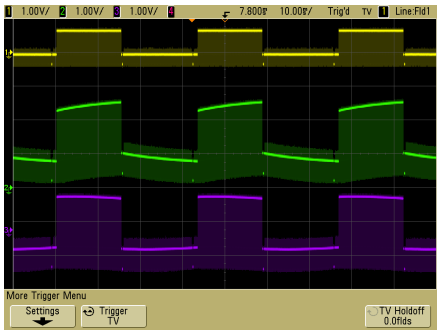
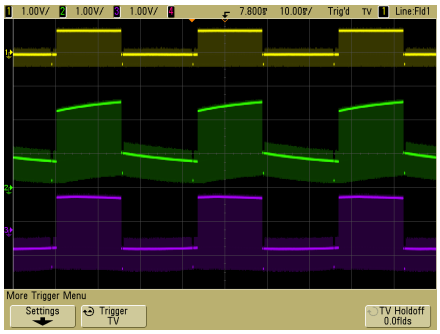
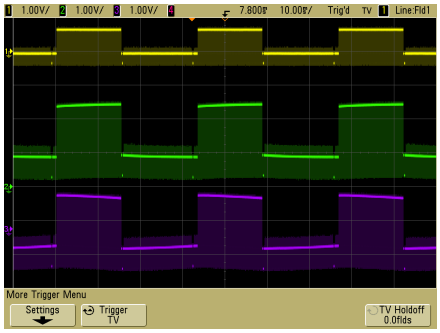
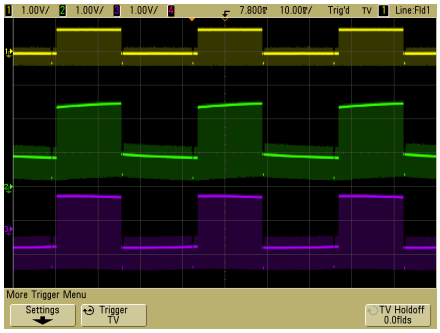
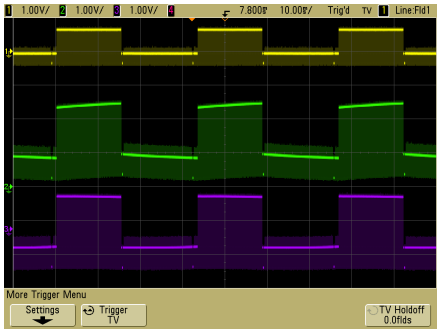


< Using SAG correction circuit >

Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω, Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

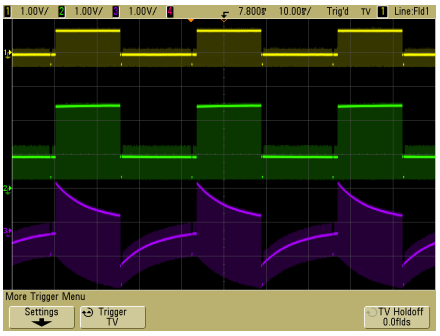
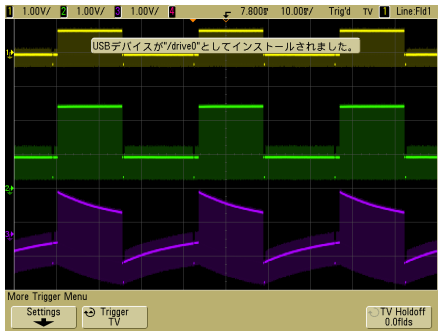
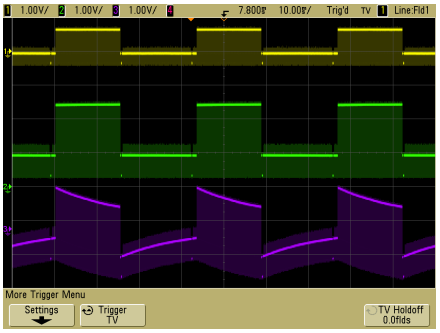
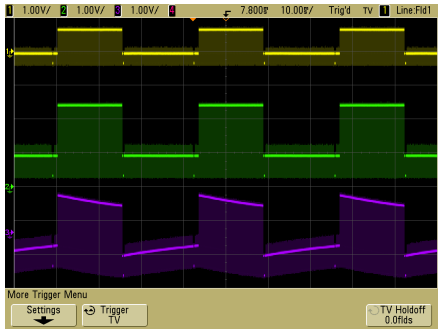
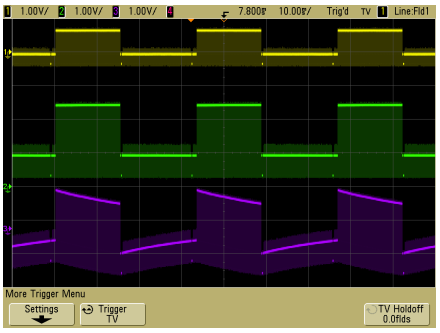
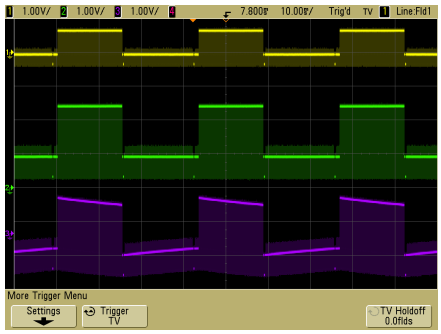
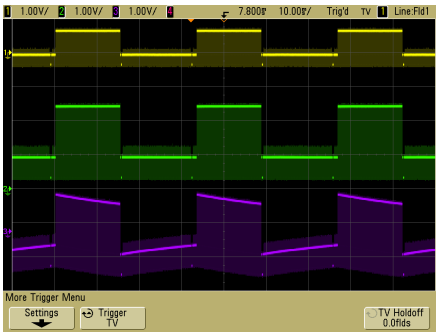
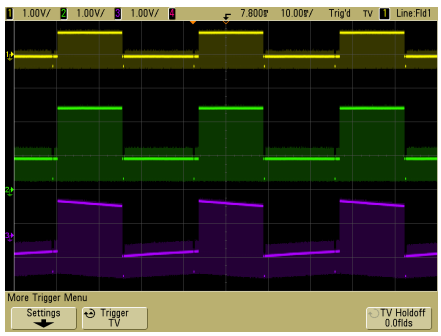
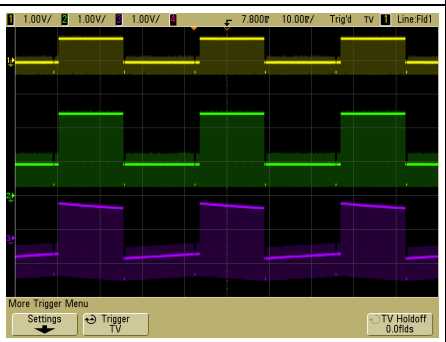
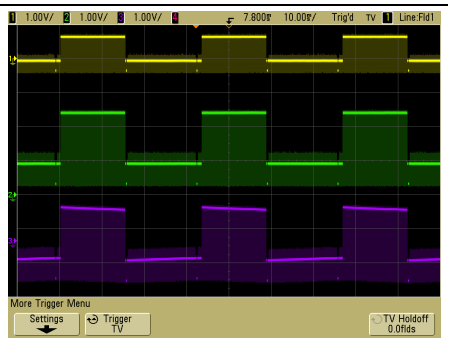
	Csag=10uF	Csag=22uF	Csag=33uF
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=75Ω, Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

	Csag=10uF	Csag=22uF	Csag=33uF
Cout=100uF			
Cout=220uF			
Cout=330uF			
Cout=470uF			
Cout=1000uF			

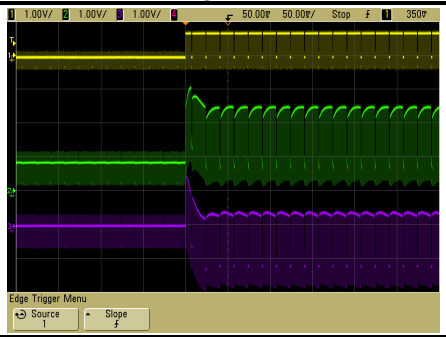
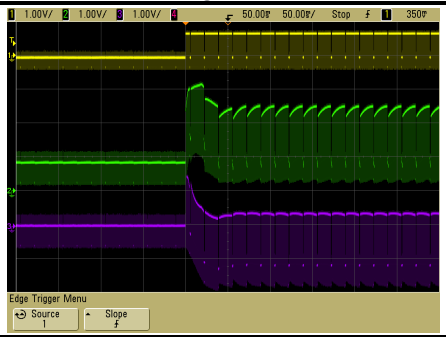
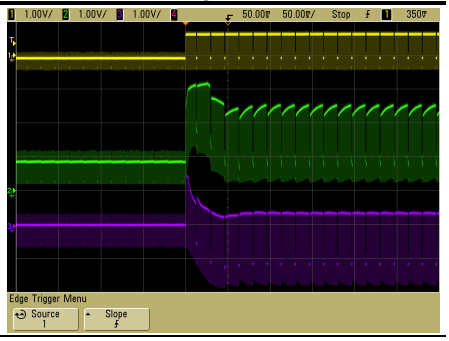
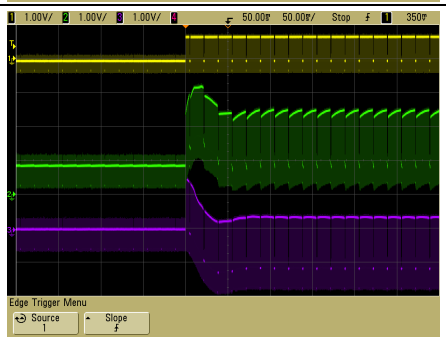
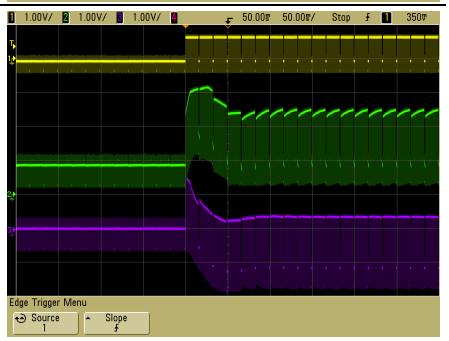
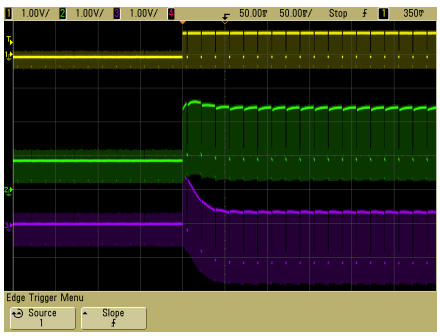
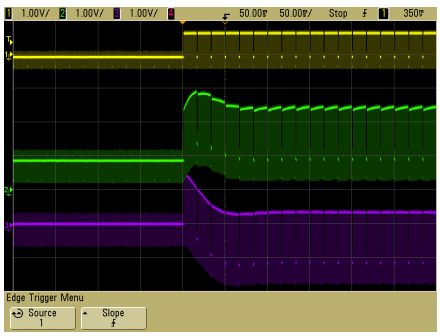
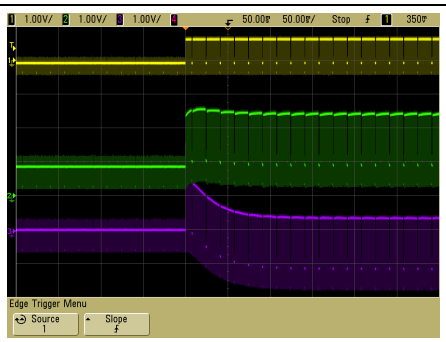
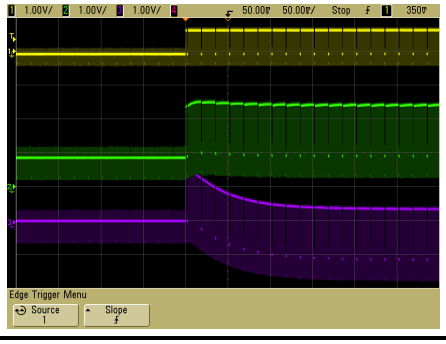
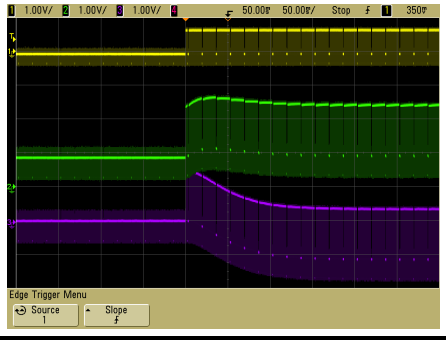
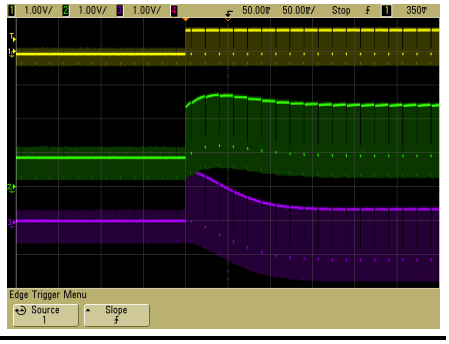
< Not using SAG correction circuit >

Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω, Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

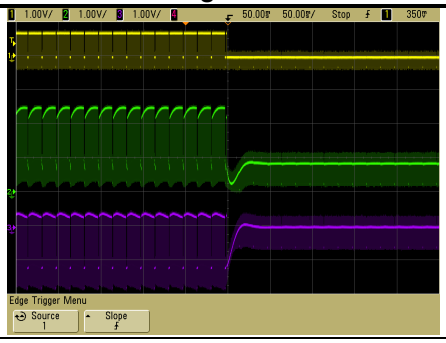
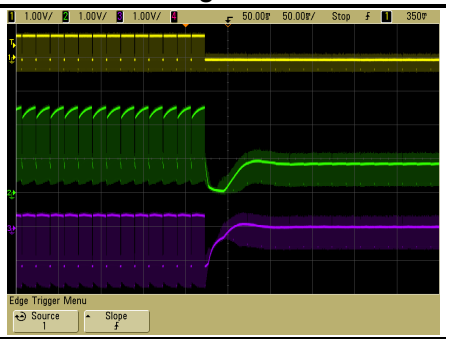
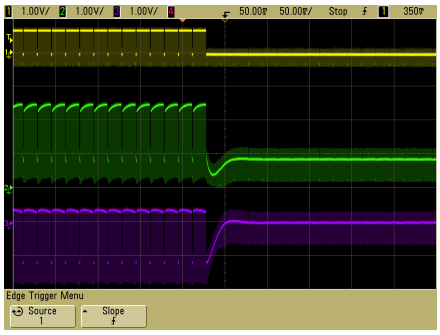
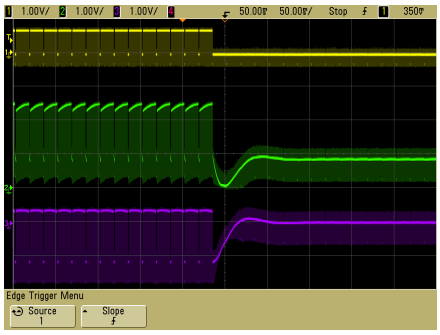
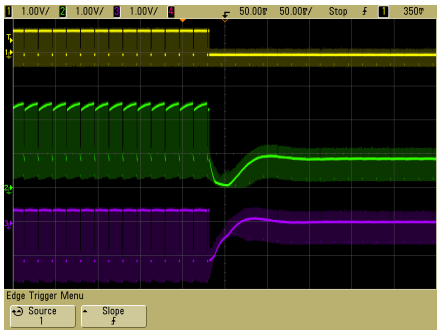
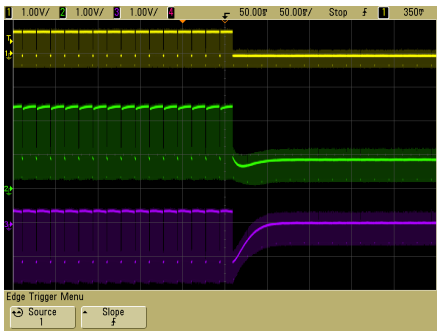
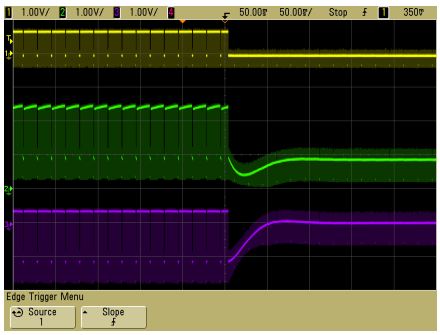
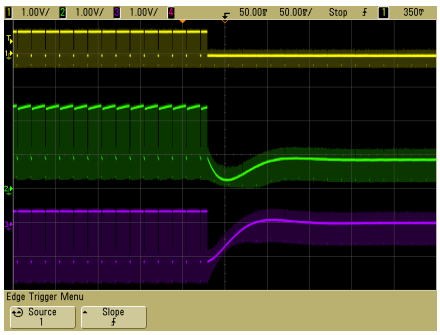
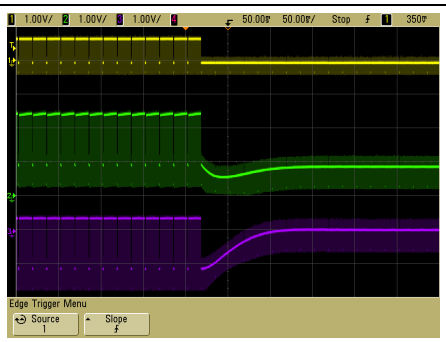
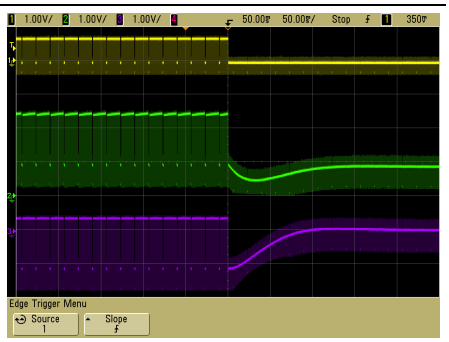
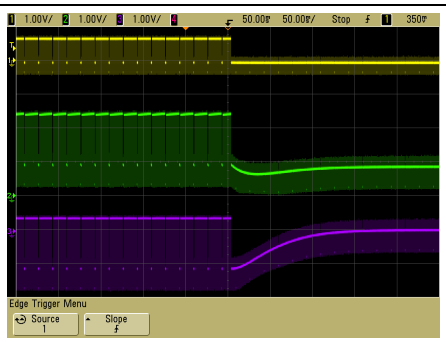
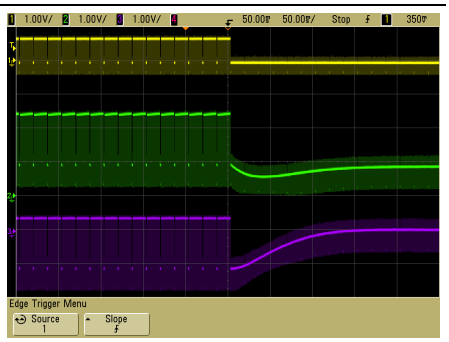
	RL=75Ω	RL=150Ω
Cout=100uF		
Cout=220uF		
Cout=330uF		
Cout=470uF		
Cout=1000uF		

< Using SAG correction circuit >

Input signal: Black to White100%, resistance150Ω, Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

	Csag=10uF	Csag=22uF	Csag=33uF
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

Input signal: White100% to Black, resistance150Ω, Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

	Csag=10uF	Csag=22uF	Csag=33uF
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

< Using SAG correction circuit >

Input signal: Black to White100%, resistance=75Ω, Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

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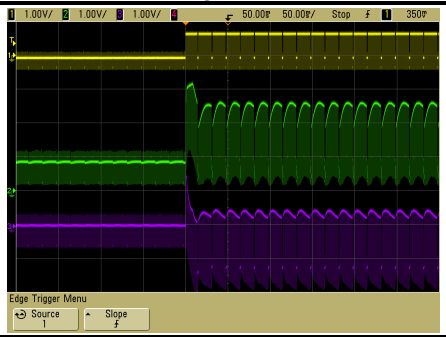
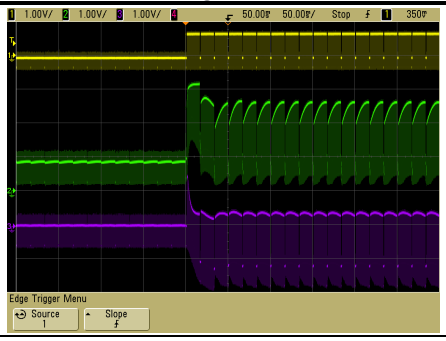
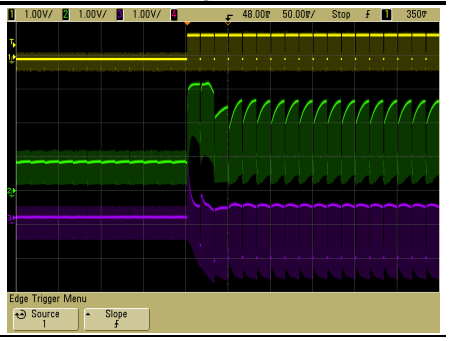
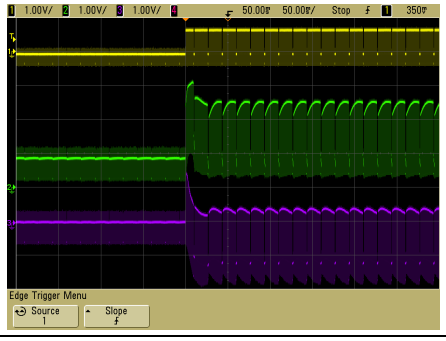
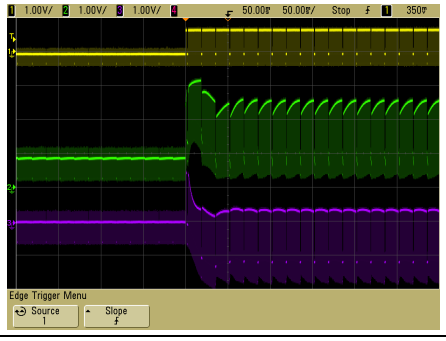
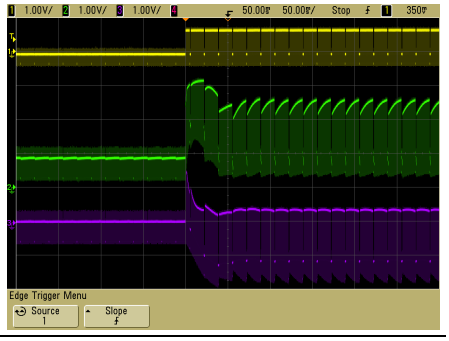
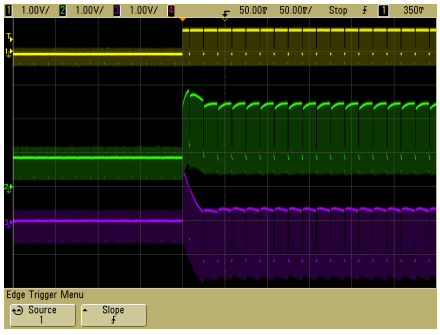
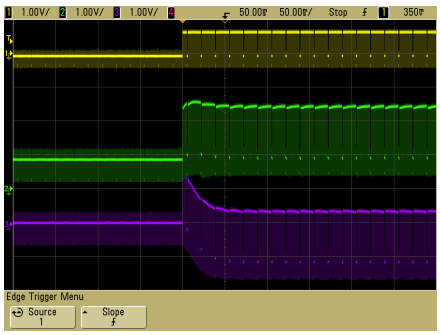
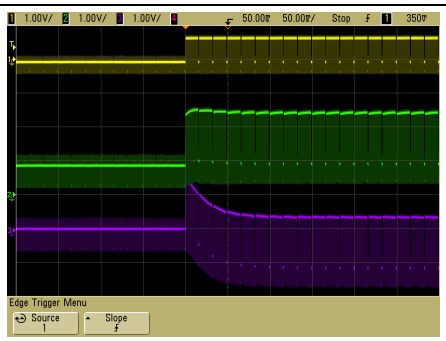
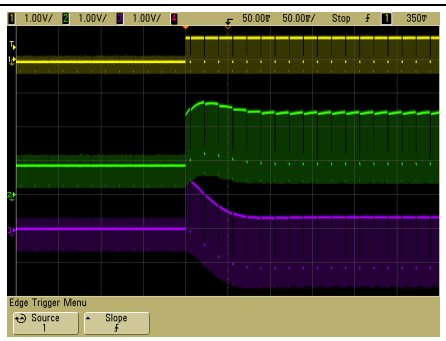
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

Input signal: White100% to Black, resistance=75Ω, Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

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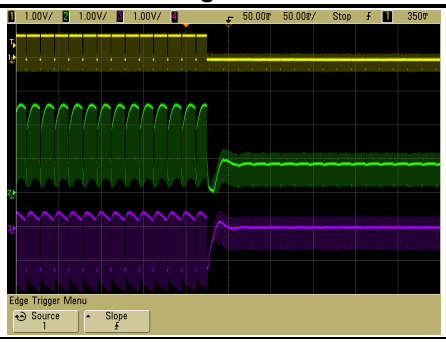
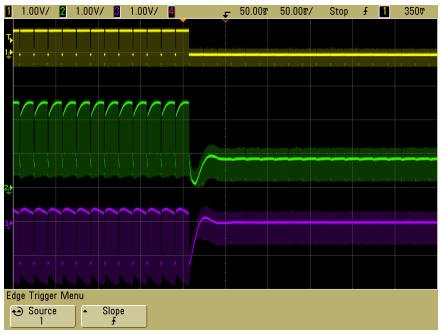
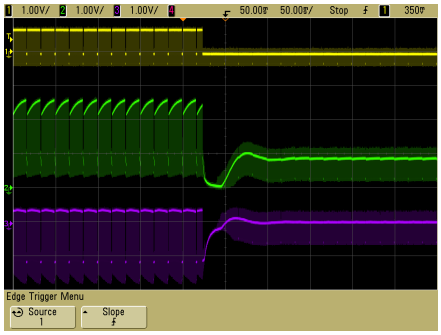
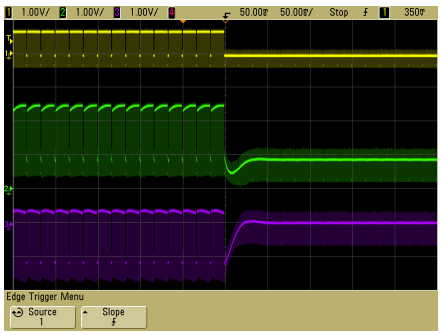
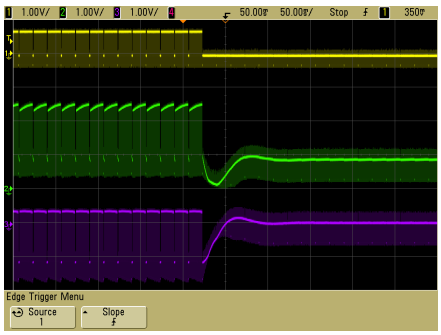
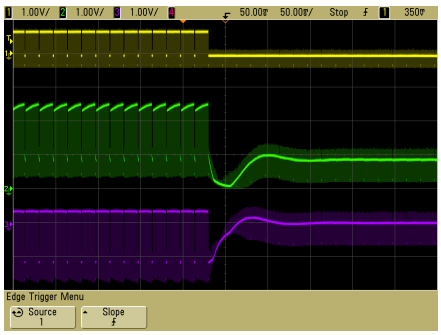
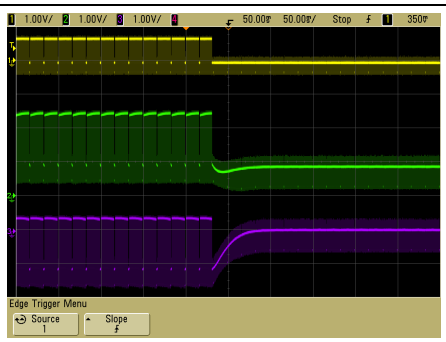
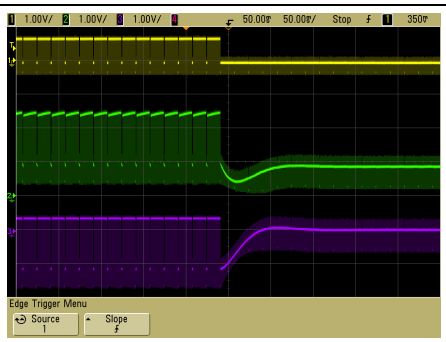
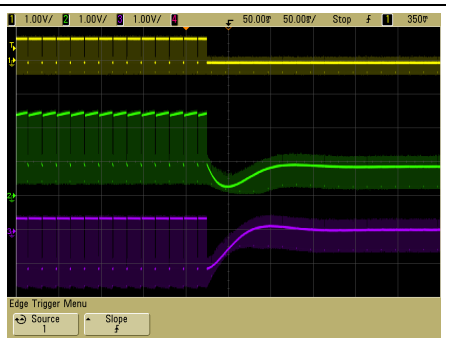
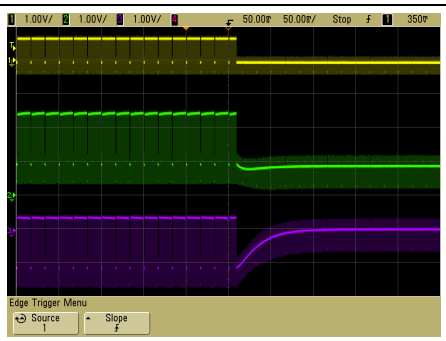
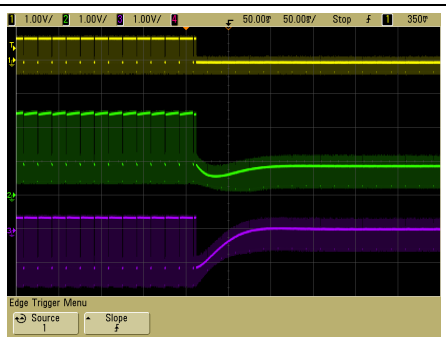
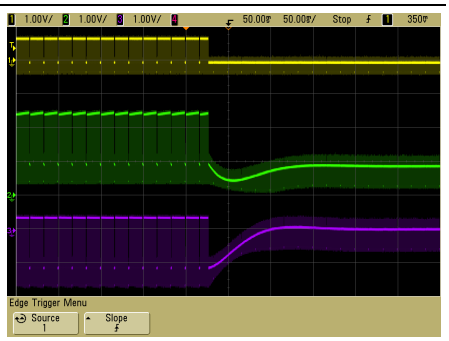
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

♦**Clamp circuit**

1. Operation of Sync-tip-clamp

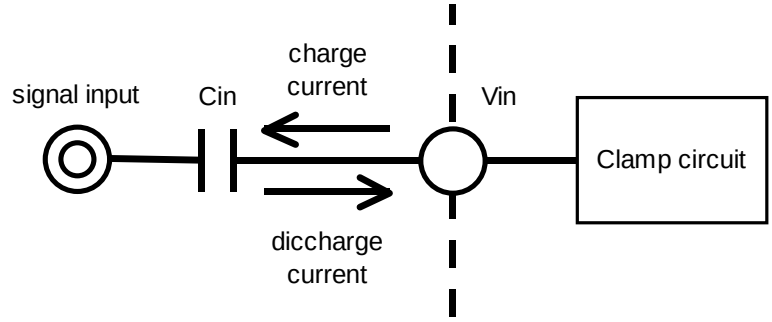
Input circuit will be explained. Sync-tip clamp circuit (below the clamp circuit) operates to keep a sync tip of the minimum potential of the video signal. Clamp circuit is a circuit of the capacitor charging and discharging of the external input Cin. It is charged to the capacitor to the external input Cin at sync tip of the video signal. Therefore, the potential of the sync tip is fixed.

And it is discharged charge by capacitor Cin at period other than the video signal sync tip. This is due to a small discharge current to the IC.

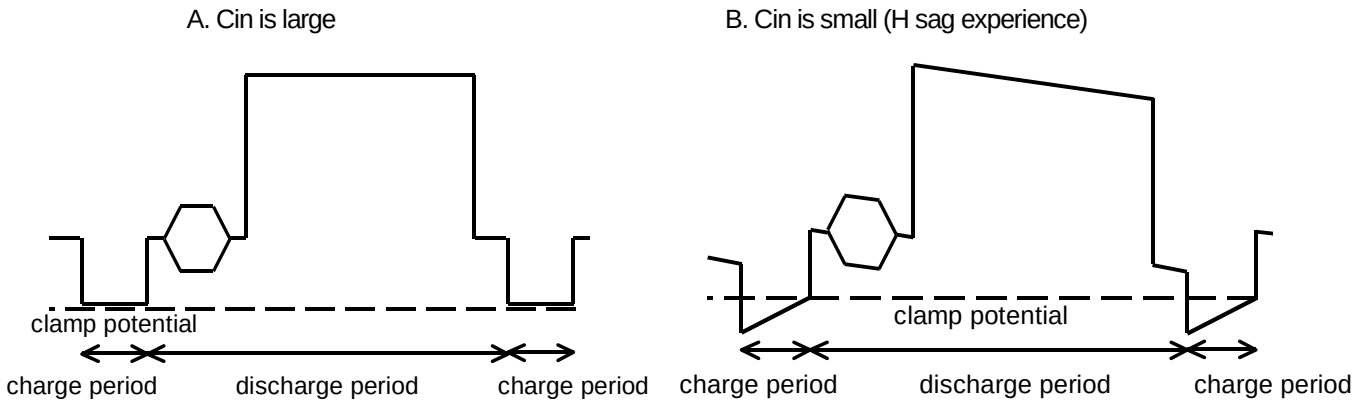
In this way, this clamp circuit is fixed sync tip of video signal to a constant potential from charging of Cin and discharging of Cin at every one horizontal period of the video signal.

The minute current be discharged an electrical charge from the input capacitor at the period other than the sync tip of video signals. Decrease of voltage on discharge is dependent on the size of the input capacitor Cin.

If you decrease the value of the input capacitor, will cause distortion, called the H sag. Therefore, the input capacitor recommend on more than 0.1uF.



< Clamp circuit >



< Waveform of input terminal >

2. Input impedance

The input impedance of the clamp circuit is different at the capacitor discharge period and the charge period.

The input impedance of the charging period is a few kΩ. On the other hand, the input impedance of the discharge period is several MΩ. Because is a small discharge-current through to the IC.

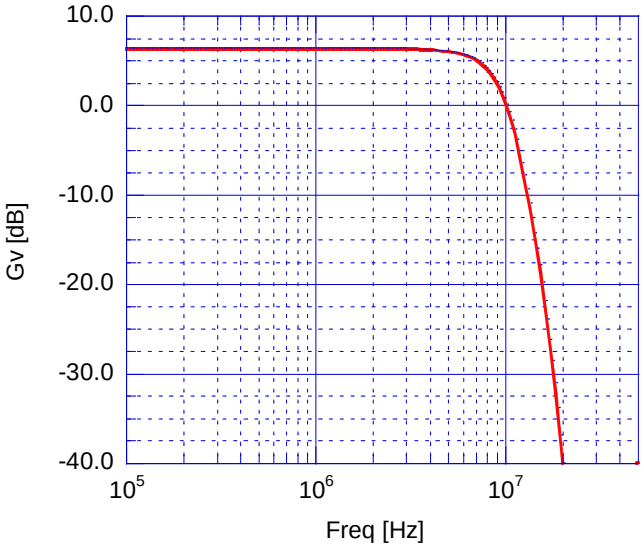
Thus the input impedance will vary depending on the operating state of the clamp circuit.

3. Impedance of signal source

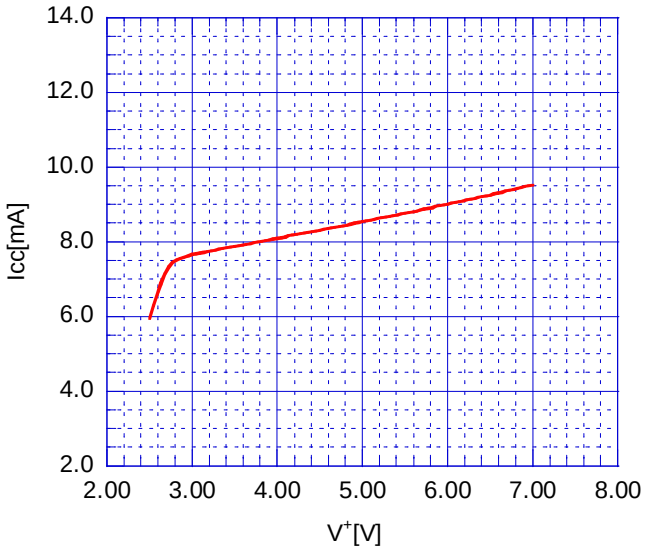
Source impedance to the input terminal, please lower than 200Ω. A high source impedance, the signal may be distorted. If so, please to connect a buffer for impedance conversion.

■TYPICAL CHARACTERISTICS

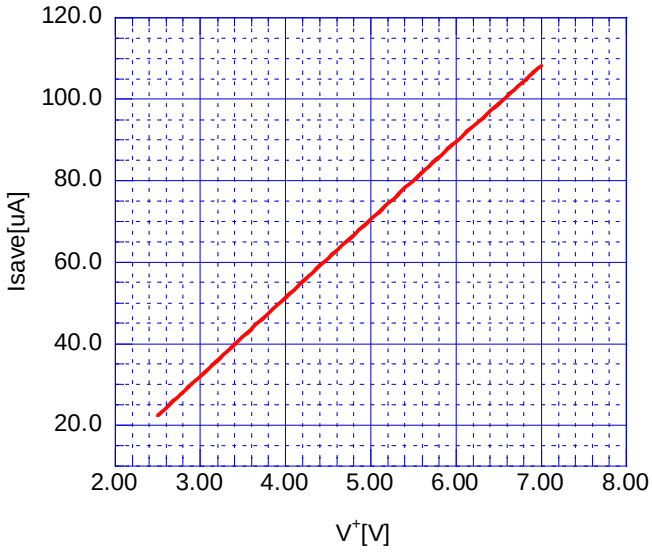
Voltage Gain vs Frequency



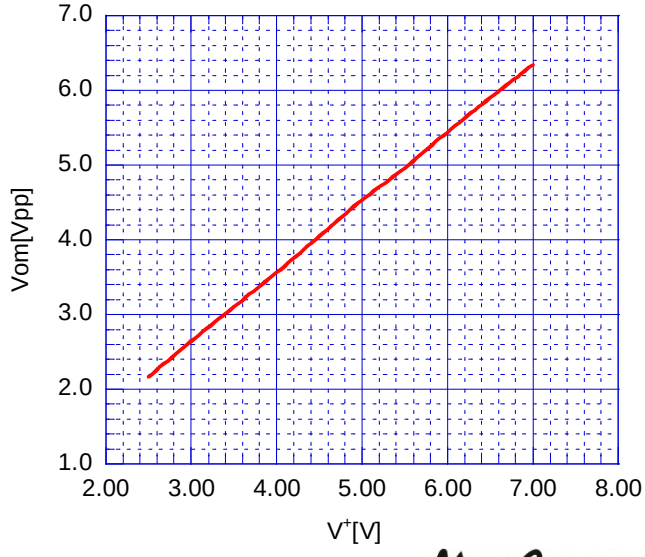
Icc vs V^+



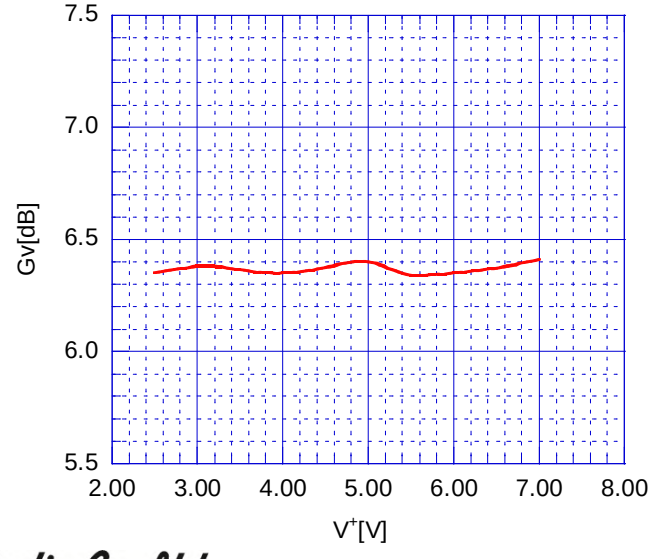
Isave vs V^+



Vom vs V^+

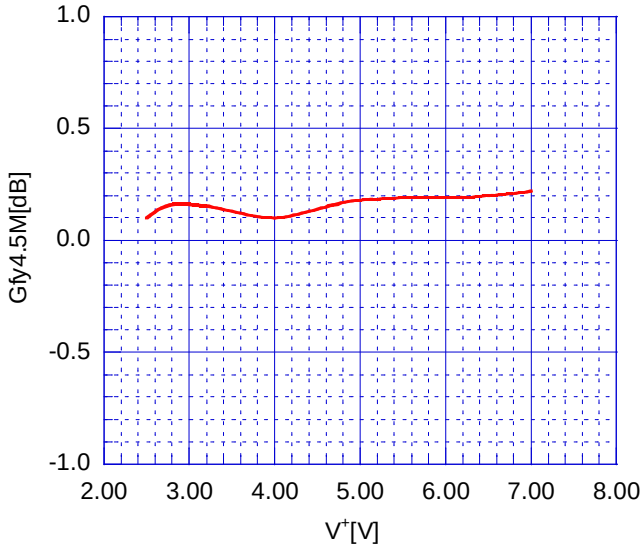


Gv vs V^+

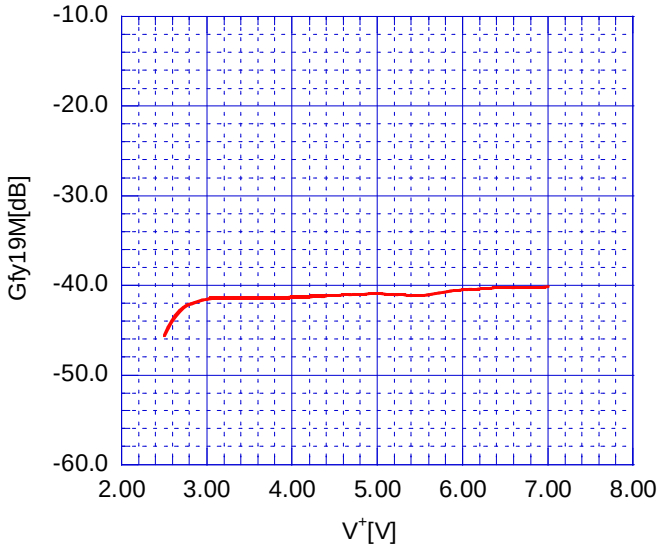


■TYPICAL CHARACTERISTICS

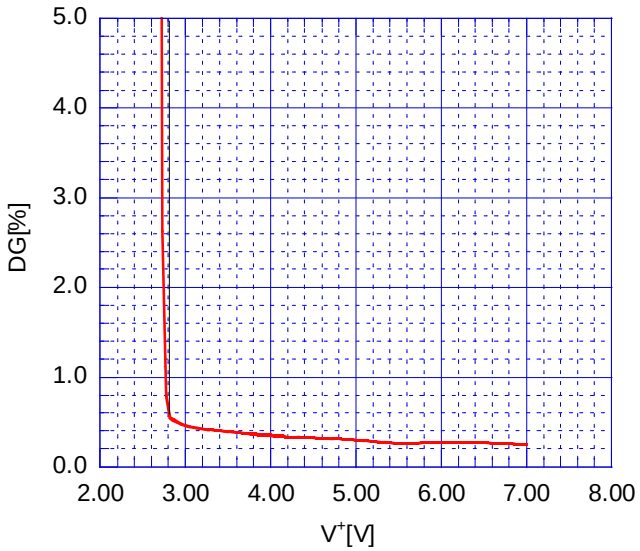
Gfy4.5M vs V^+



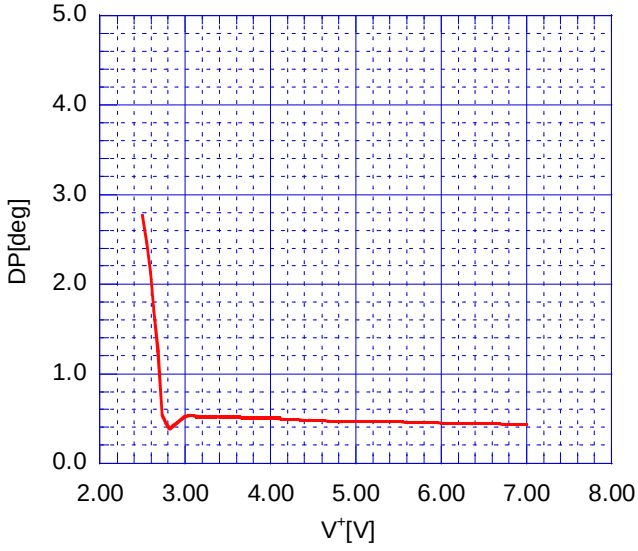
Gfy19M vs V^+



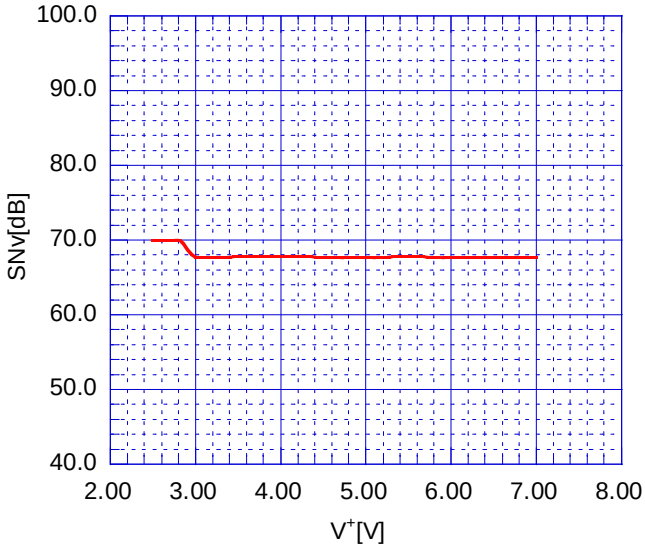
DG vs V^+



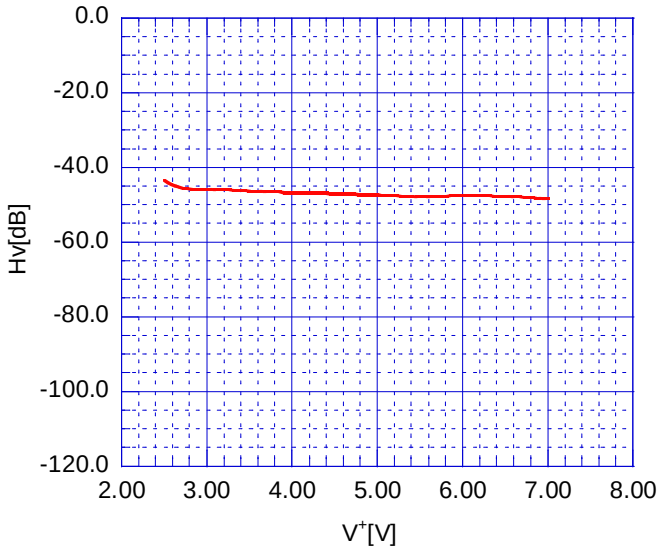
DP vs V^+



SNv vs V^+

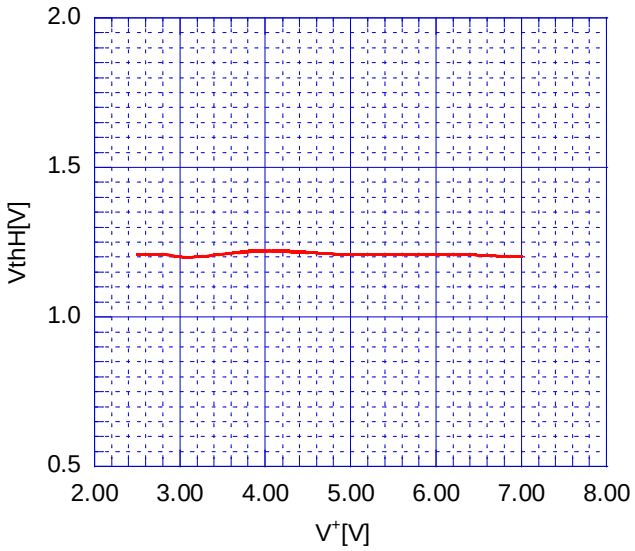


Hv vs V^+

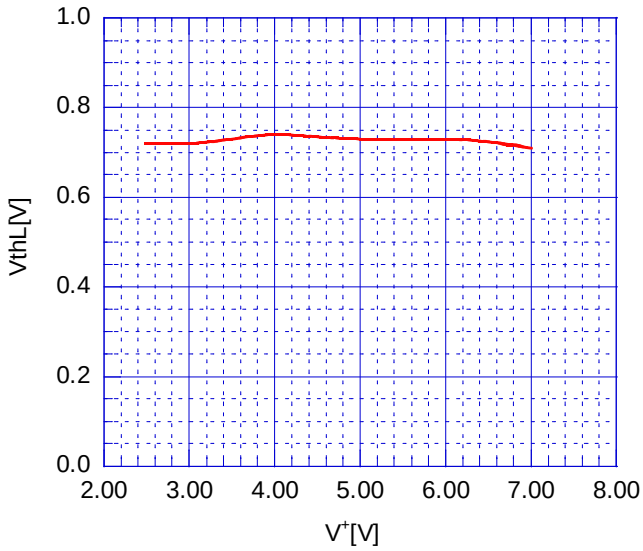


■TYPICAL CHARACTERISTICS

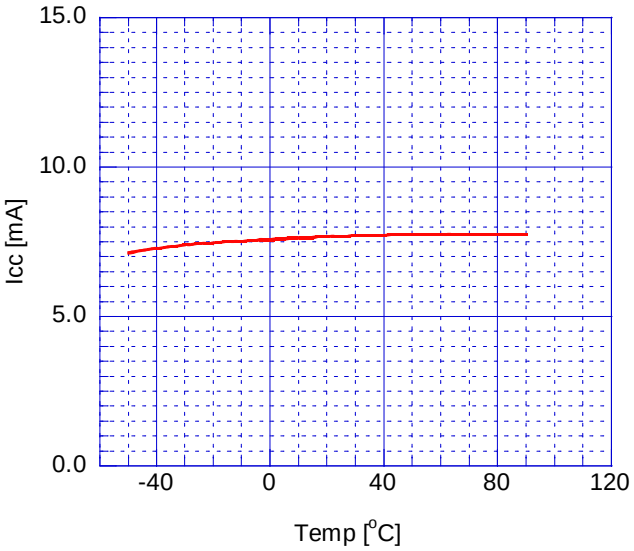
VthH vs V^+



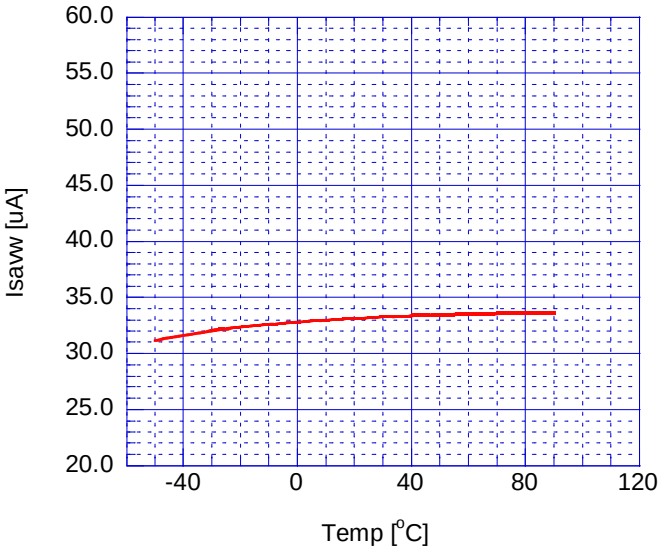
VthL vs V^+



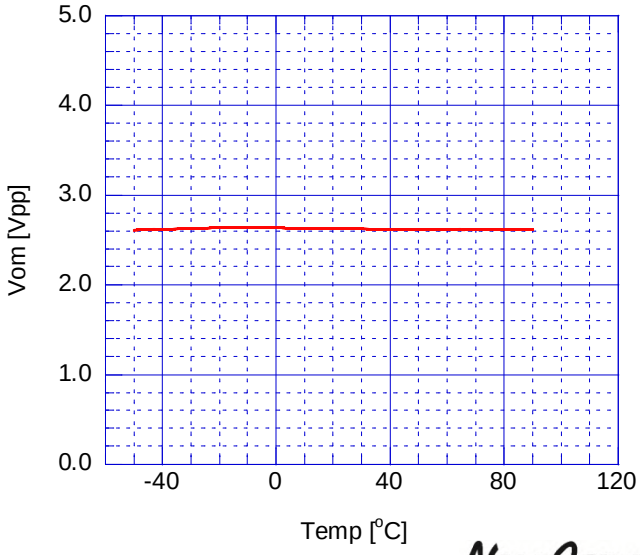
Icc vs Temp.



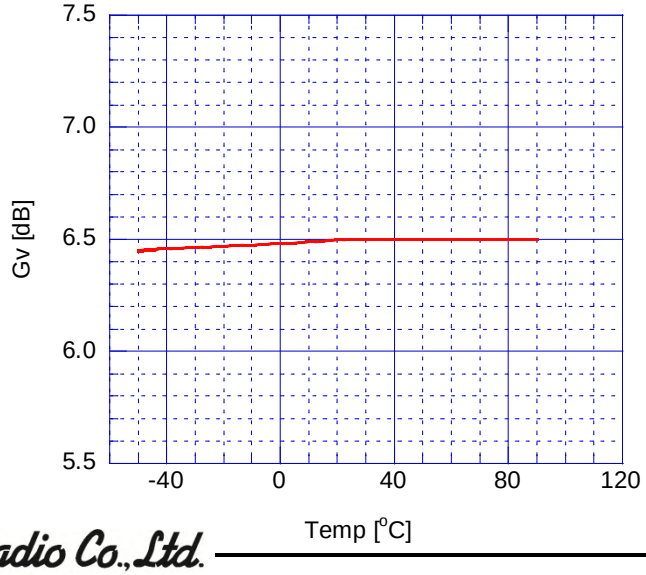
Isave vs Temp.



Vom vs Temp.

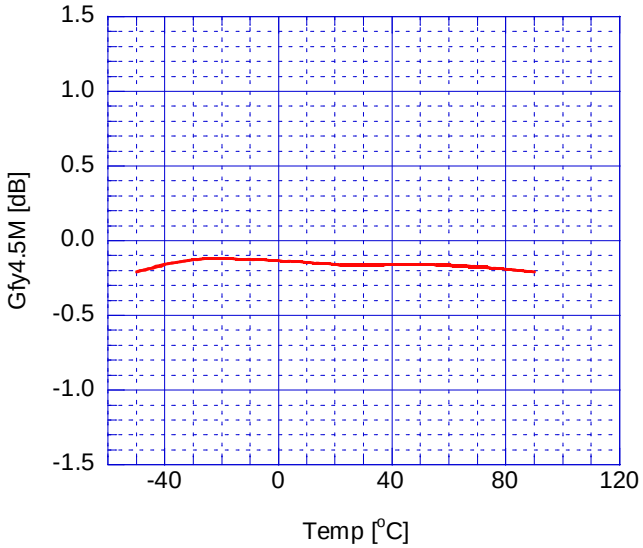


Gv vs Temp.

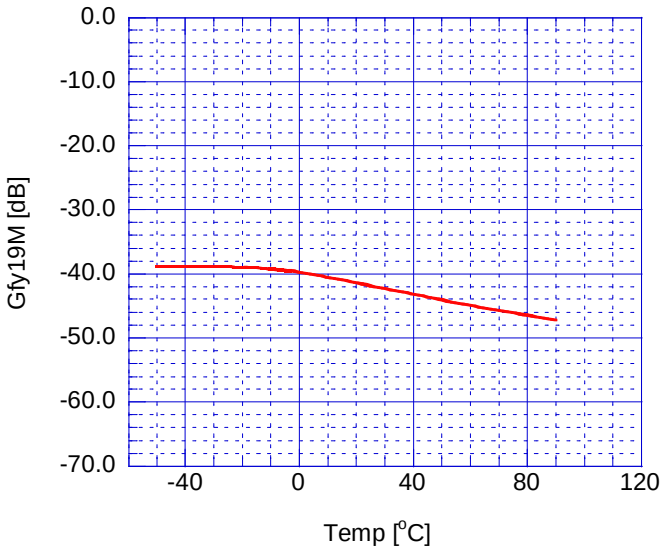


■TYPICAL CHARACTERISTICS

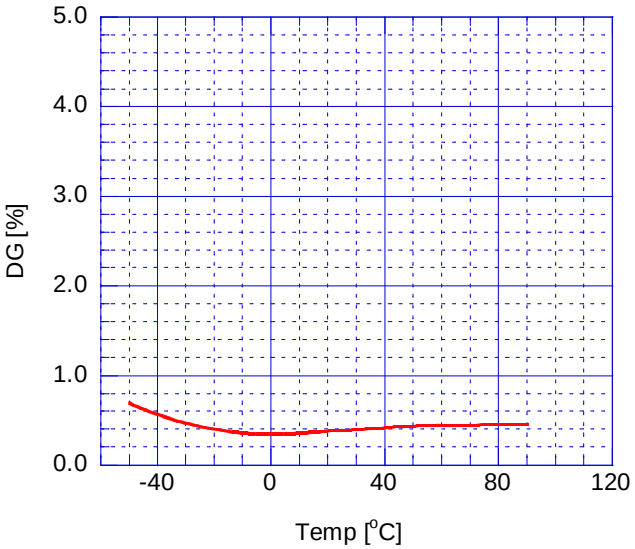
LPF4.5M vs Temp.



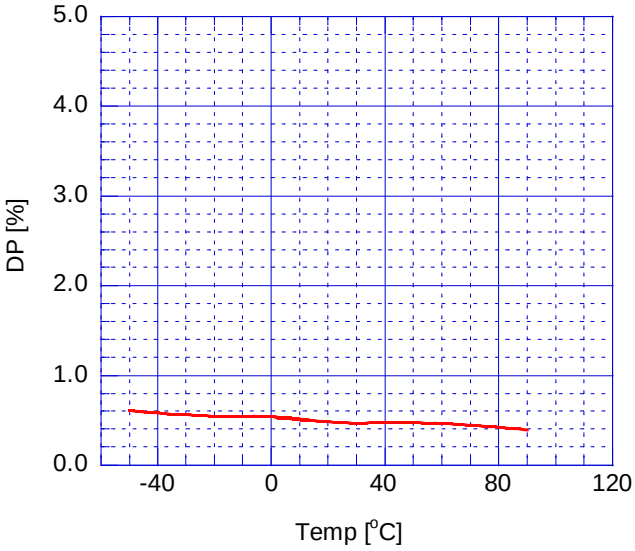
LPF19M vs Temp.



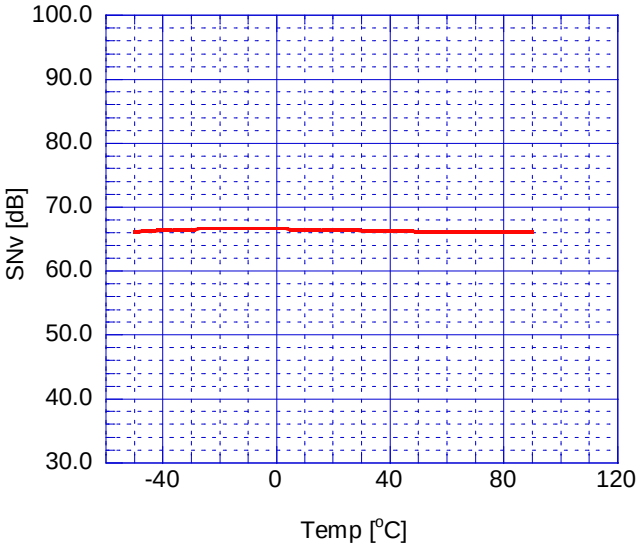
DG vs Temp.



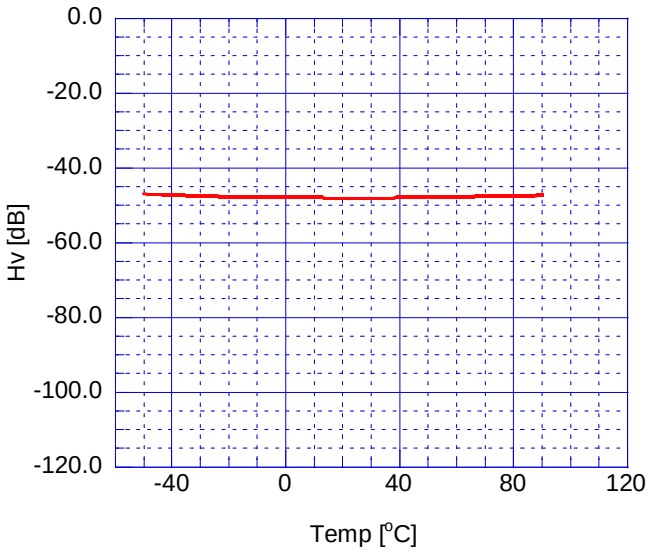
DP vs Temp.



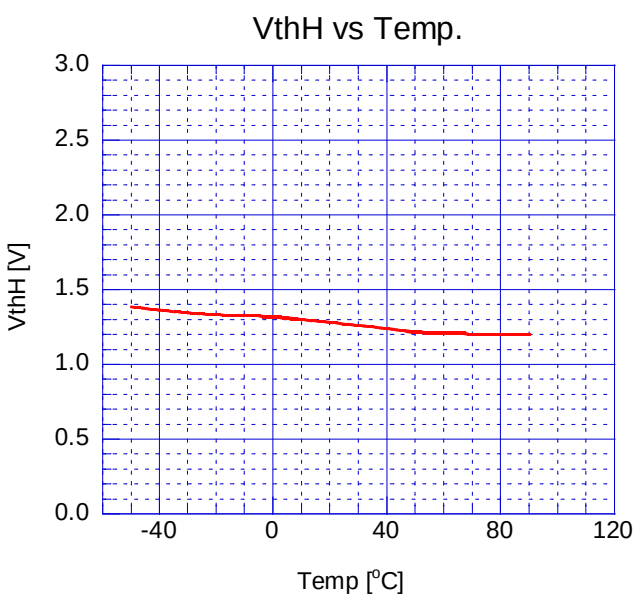
SNv vs Temp.

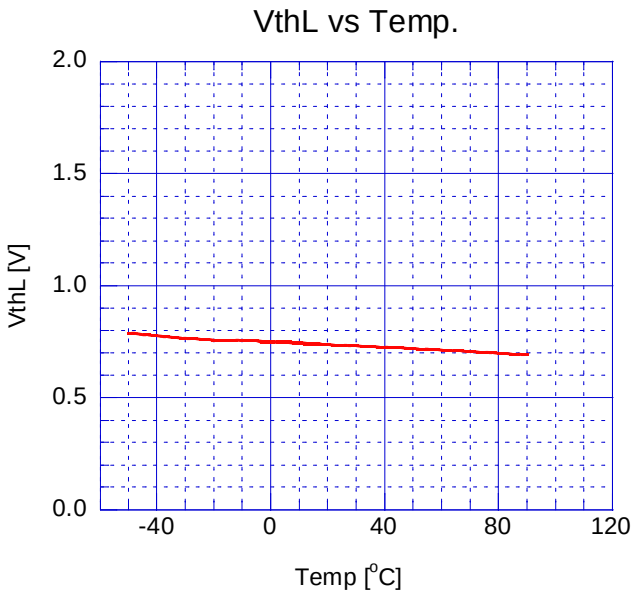


Hv vs Temp.



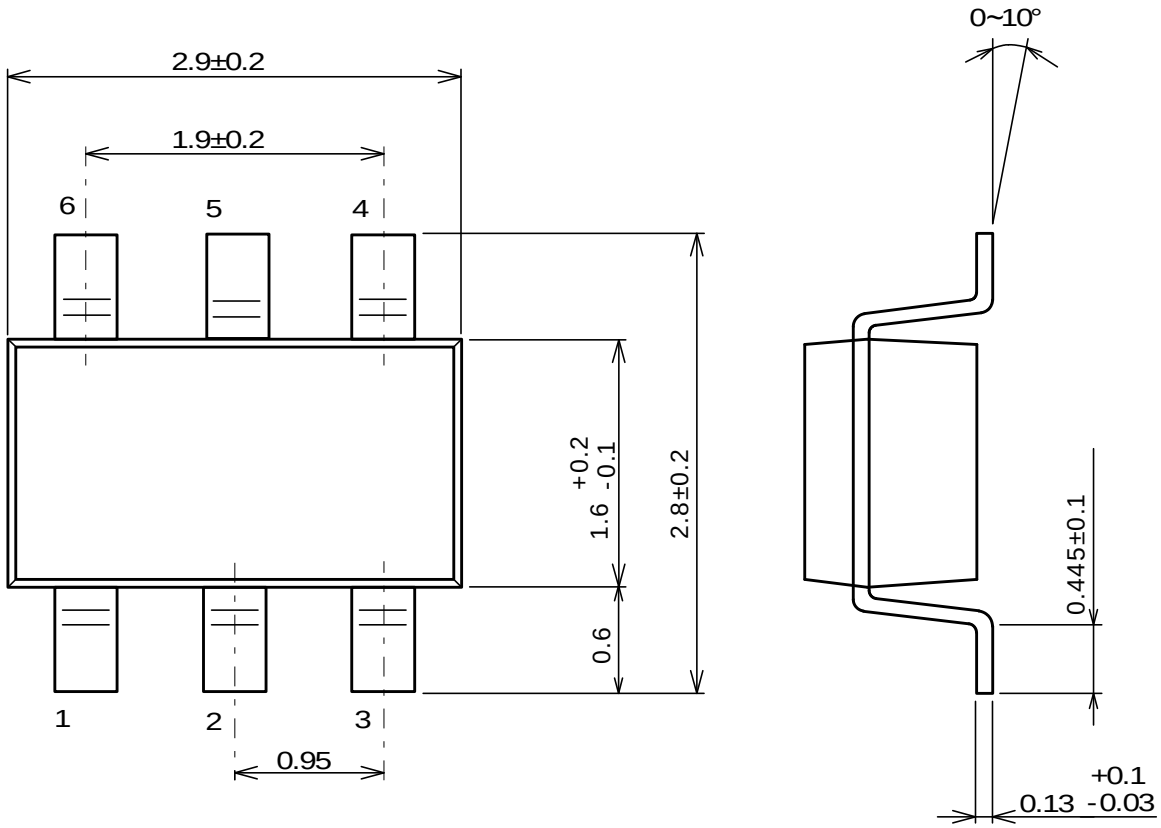
■TYPICAL CHARACTERISTICS

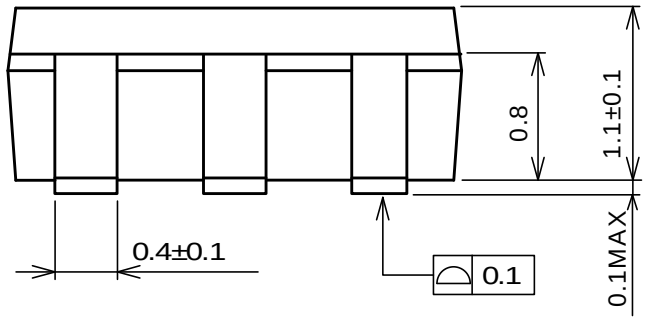




■PACKAGE OUTLINE

SOT-23-6-1(MTP6-1)

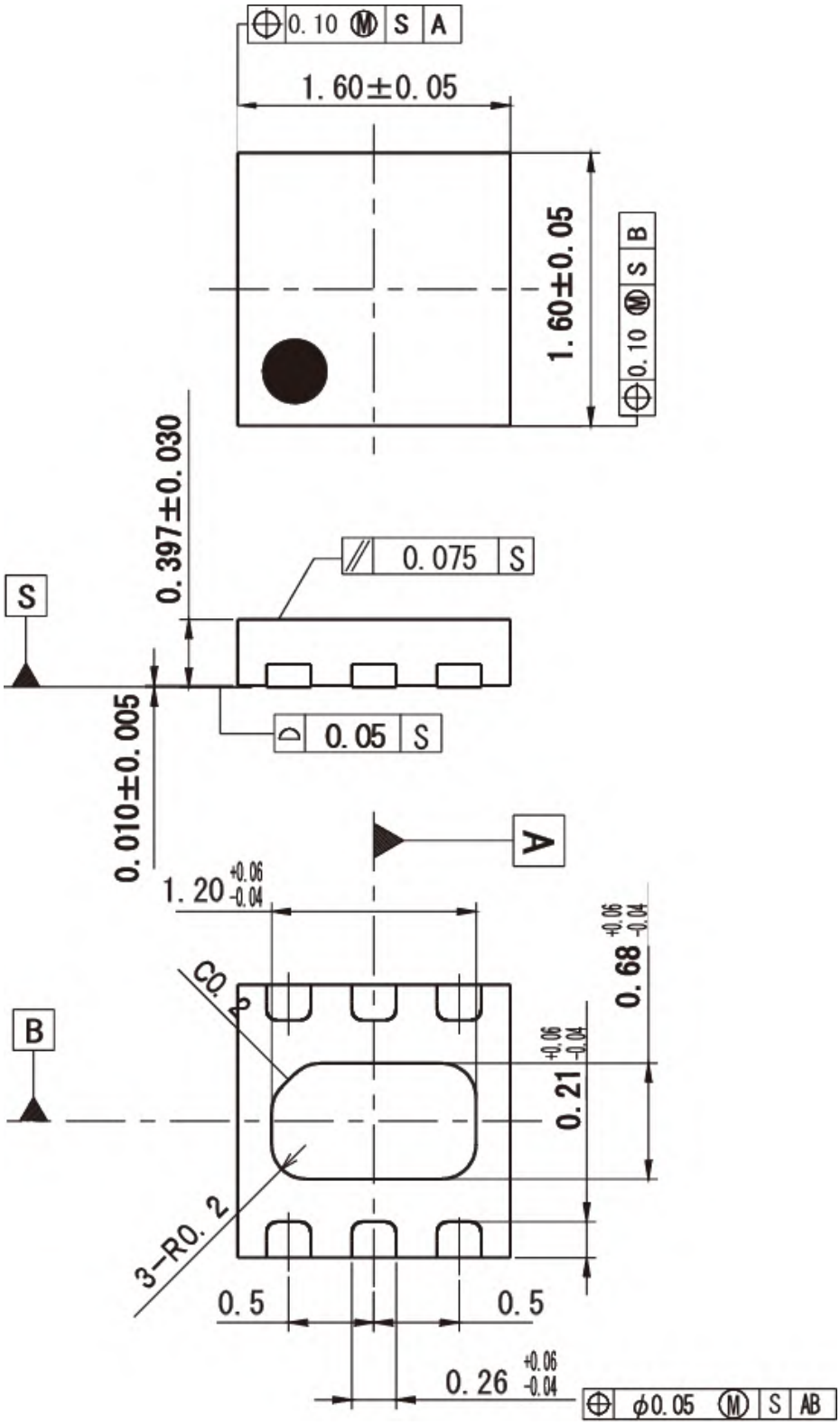




UNIT : mm

■PACKAGE OUTLINE

DFN6-G1 (ESON6-G1)

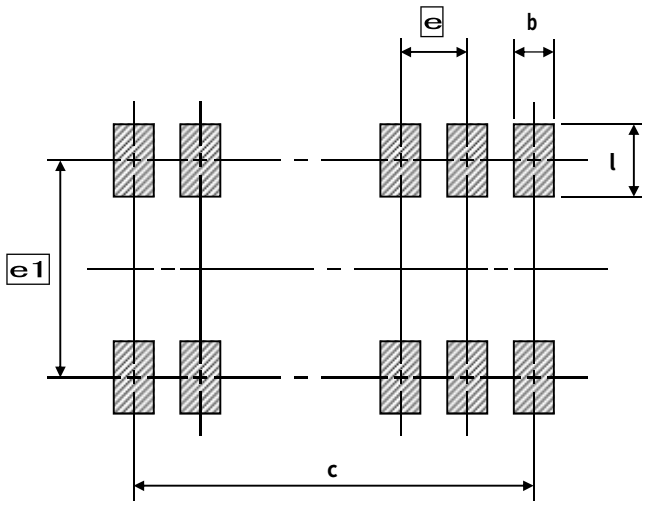


UNIT : mm

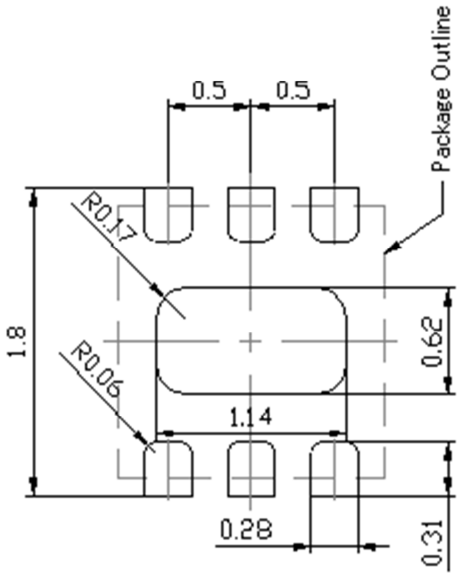
■SOLDER FOOT PRINT

PKG	b	l	c	e1	e
SOT-23-6-1	0.70	1.00	1.90	2.40	0.95

UNIT : mm



DFN6-G1



UNIT : mm

Note : These solder foot print dimensions are just examples.
When designing PCB, please estimate the pattern carefully.

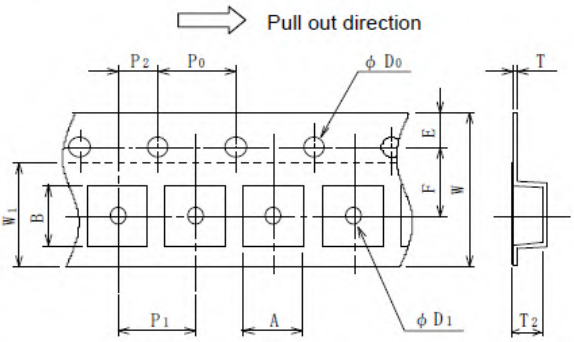
■PACKING SPECIFICATION (SOT-23-6-1)

General Description

NJRC delivers ICs in 4 methods, plastic tube container, two kinds of Taping, tray and vinyl bag packing. Except adhesive tape treated anti electrostatic and contain carbon are using as the ESD (Electrostatic Discharge Damage) protection.

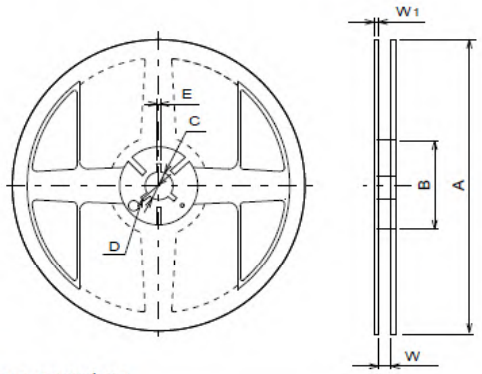
SOT-23(MTP) Emboss Taping (TE1)

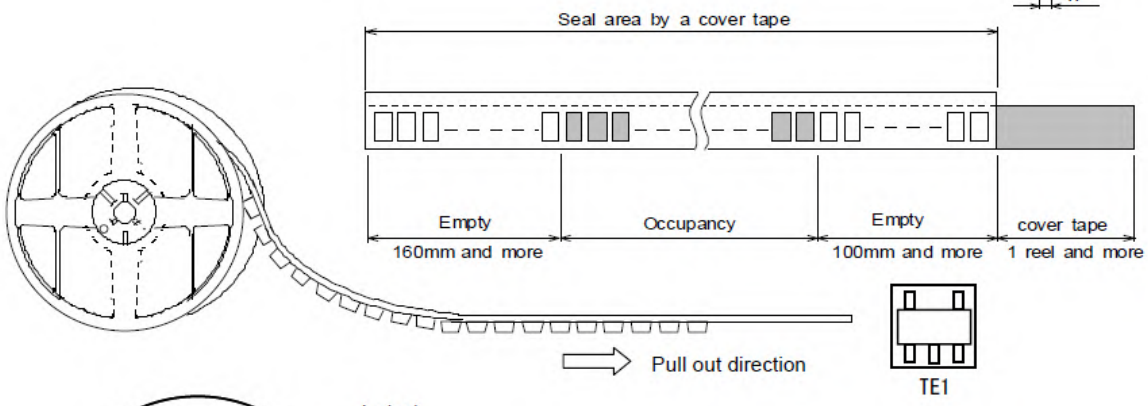
Symbol	SOT-23-6-1	Remark
A	3.3±0.1	Bottom size
B	3.2±0.1	Bottom size
D_0	1.55	
D_1	1.05	
E	1.75±0.1	
F	3.5±0.05	
P_0	4.0±0.1	
P_1	4.0±0.1	
P_2	2.0±0.05	
T	0.25±0.05	
T_2	1.57	
W	8.0±0.3	
W_1	5.5	Thickness 0.1MAX

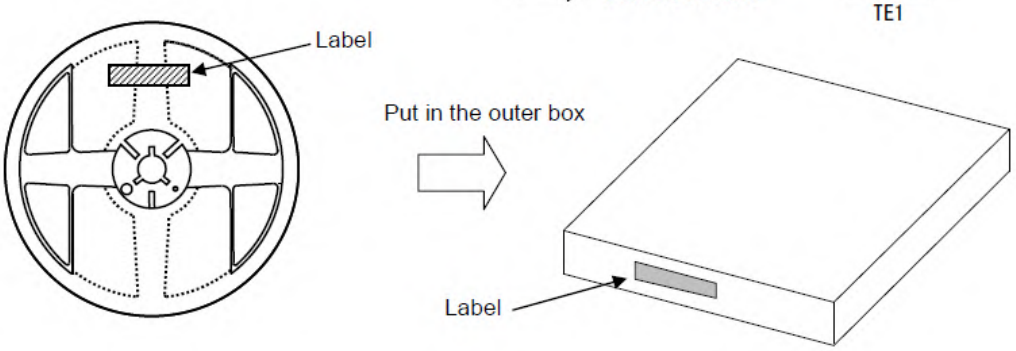


Symbol	SOT-23-6-1
A	Ø180±1
B	Ø 60±1
C	Ø 13±0.2
D	Ø 21±0.8
E	2±0.5
W	9±0.5
W_1	1.2±0.2
Contents	3,000pcs

Unit : mm







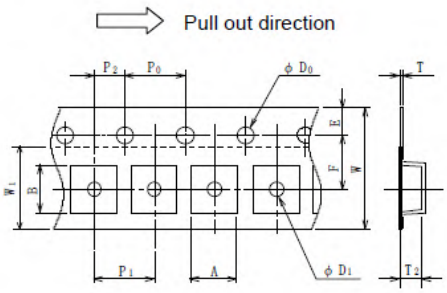
■PACKING SPECIFICATION (DFN6-G1)

General Description

NJRC delivers ICs in 4 methods, plastic tube container, two kinds of Taping, tray and vinyl bag packing. Except adhesive tape treated anti electrostatic and contain carbon are using as the ESD (Electrostatic Discharge Damage) protection.

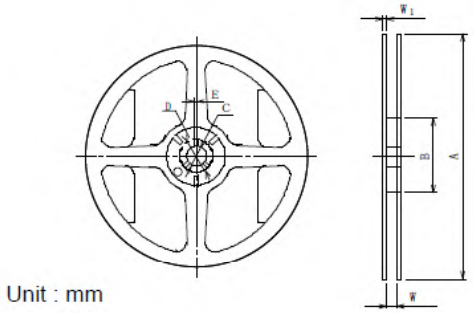
DFN(ESON) Emboss Taping (TE3)

Symbol	DFN6-G1 (ESON6-G1)	Remark
A	1.85±0.05	Bottom size
B	1.85±0.05	Bottom size
D_0	1.5+0.1/-0	
D1	0.5 ±0.1	
E	1.75±0.1	
F	3.50±0.05	
P_0	4.0 ±0.1	
P_1	4.0 ±0.1	
P_2	2.00±0.05	
T	0.25±0.05	
T_2	0.75	
W	8.0 ±0.2	
W_1	5.5	Thickness 0.1MAX

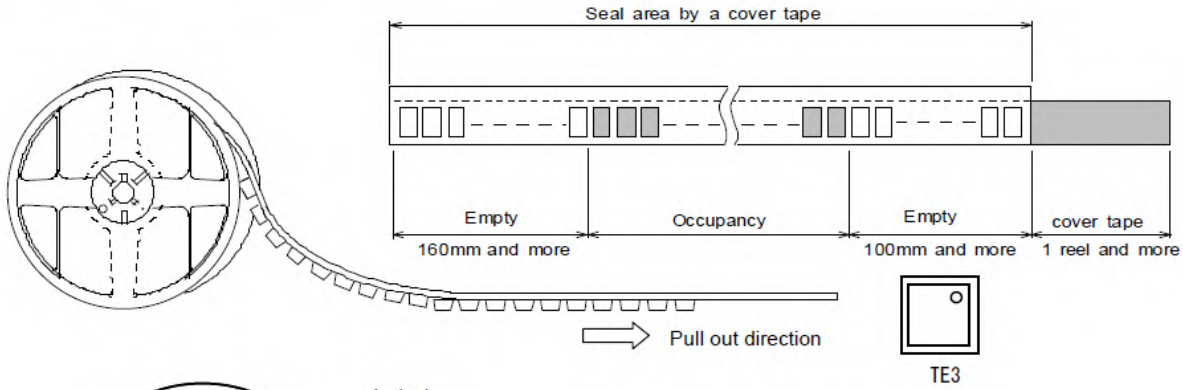


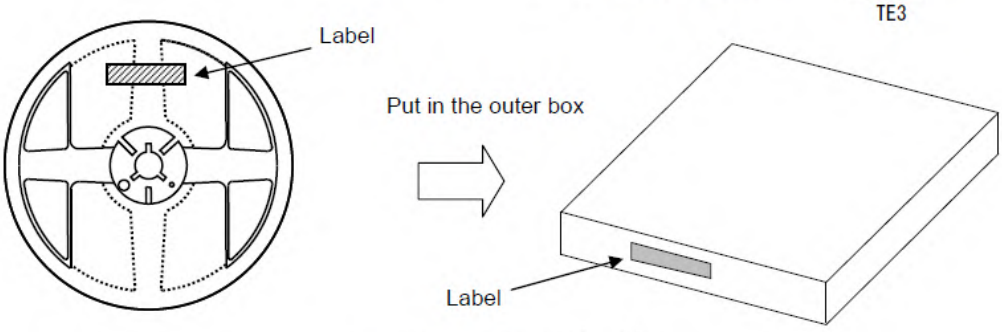
Unit : mm

Symbol	DFN6-G1 (ESON6-G1)
A	φ180 +0/-1.5
B	φ 60 +1/-0
C	φ13.0±0.2
D	φ21.0±0.8
E	2.0±0.5
W	9.0 +0.3/-0
W_1	1.2
Contents	3,000pcs



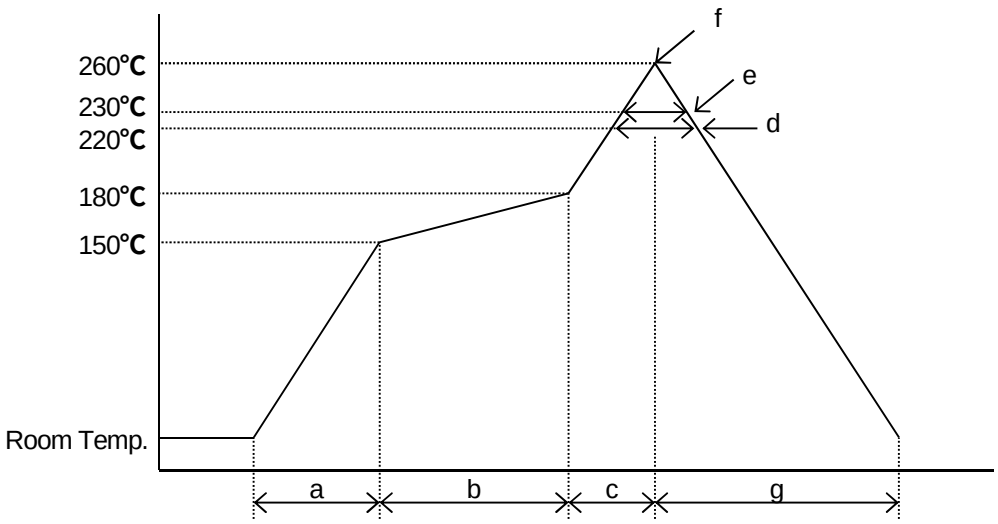
Unit : mm





■RECOMMENDED MOUNTING METHOD

∗Recommended reflow soldering procedure



a：Temperature ramping rate	: 1 to 4℃/s
b：Pre-heating temperature	: 150 to 180℃
time	: 60 to 120s
c：Temperature ramp rate	: 1 to 4℃/s
d：220℃ or higher time	: Shorter than 60s
e：230℃ or higher time	: Shorter than 40s
f：Peak temperature	: Lower than 260℃
g：Temperature ramping rate	: 1 to 6℃/s

The temperature indicates at the surface of mold package.

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