Signetics

SCB68459
Disk Phase Locked Loop (DPLL)

Preliminary Specification

Microprocessor Products

2

DESCRIPTION

The SCB68459 Disk Phase Locked Loop (DPLL) is a bipolar device that complements the SCN68454 Intelligent Multiple Disk Controller (IMDC). Together, with an external voltage controlled oscillator (VCO), the DPLL and IMDC provide all the functions required to control up to four disks with SA800, ST500, or SA1000 type interfaces.

The DPLL uses an external VCO for the variable clock rate which tracks the read data from the disk unit. This VCO can be any device that can interface to the DPLL. The IMDC can control up to four disks; if these are all the same, only one DPLL is needed. If different disk types are driven by the same IMDC, then a DPLL is required for each disk drive type.

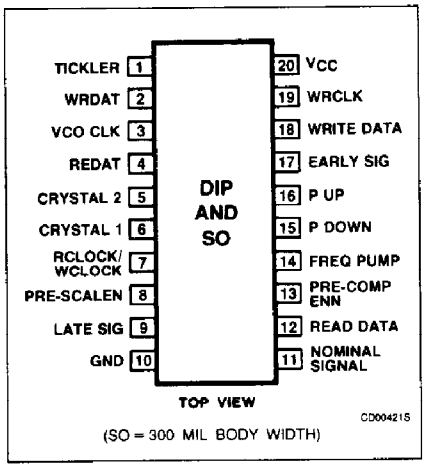
The SCB68459 DPLL operates by producing an oscillator frequency to match the frequency of an input signal. In this locked condition, any slight change in the input frequency (called jitter) will appear as a change in phase between the input frequency and the VCO frequency. This phase shift then acts as an error signal to change the frequency of the local DPLL VCO to match the input frequency.

The SCB68459 is constructed using Signetics extended performance logic (EPL) bipolar technology.

FEATURES

- **Supports composite data rate of 100KHz to 10MHz**
- **On chip multiplexer for read and write clock**
- **Supports MFM and FM data formats**
- **Generates synchronous clock for read data**
- **Built in pre-compensation circuit**
- **Phase detector and frequency detection for improved operation**
- **External loop gain control**
- **Minimal amount of external components required for operation**
- **Single +5 volt power supply**
- **Crystal controlled write clock**

PIN CONFIGURATION



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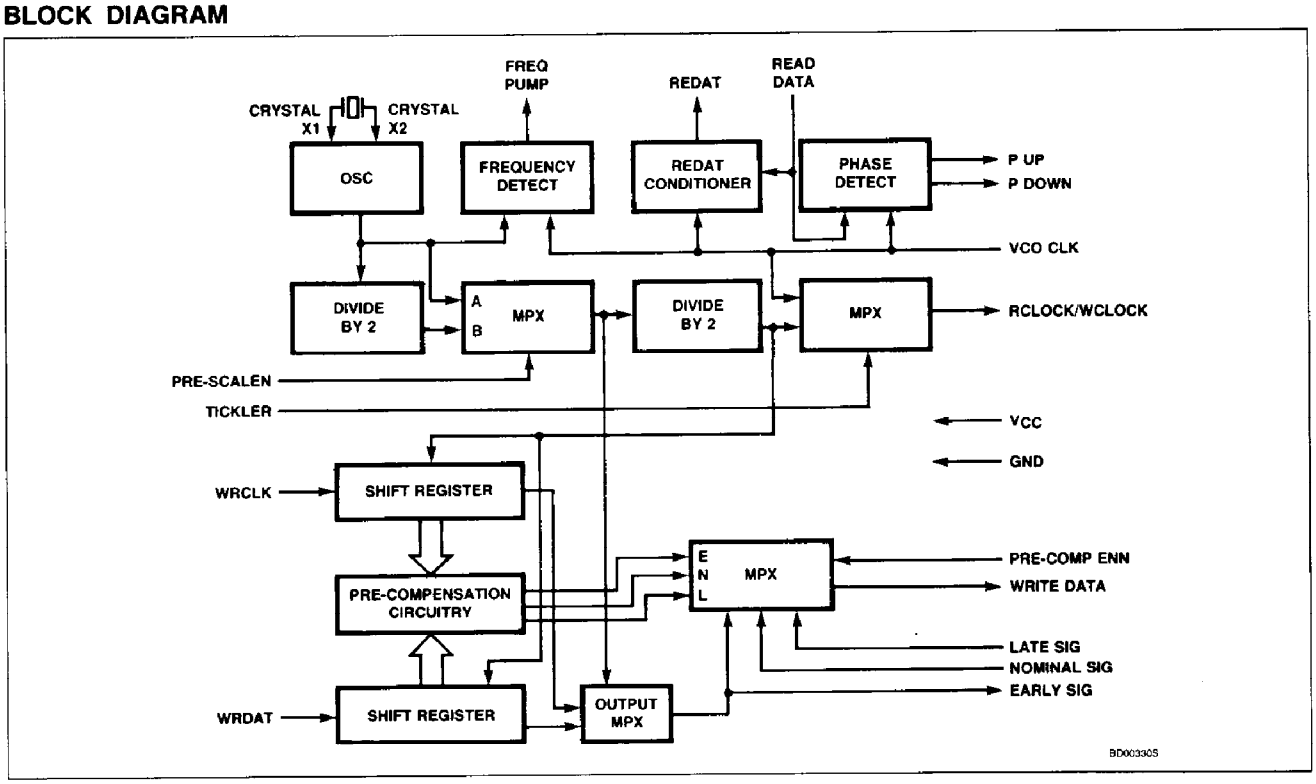
ORDERING CODE

PACKAGES	V_{CC} = 5V ± 5%, T_A = 0 to 70°C
Ceramic DIP	SCB68459CAI20
Plastic DIP	SCB68459CAN20
Small Outline	SCB68459CAD20

BLOCK DIAGRAM



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PIN DESCRIPTION

The pin description table describes the function of each of the pins of the DPLL. Signal names ending in "N" are active low. All other signals are active high.

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
WRDAT	2	I	**Write Data Pattern:** Active high. WRDAT is a non-return to zero (NRZ) input which contains the data information; i.e., it is the polarity of the WRITE DATA to be output in the second half of the bit cell time.
WRCLK	19	I	**Write Clock Pattern:** Active high. WRCLCK is an NRZ input which contains the clock information; i.e., it is the polarity of the WRITE DATA to be output during the first half of the bit cell time.
PRE-SCALEN	8	I	**Pre-Scale:** Active low. When PRE-SCALEN is low, the crystal frequency is divided by 4 (the normal divide by two plus an additional divide by 2) before being used as WRCLOCK. When PRE-SCALEN is high, the crystal frequency is not pre-scaled. Typically used to encode/decode both FM and MFM with the same crystal frequency.
TICKLER	1	I	**Tickler:** Active high. TICKLER controls the operation of the RCLOCK/WCLOCK output signal. If TICKLER is high, internal logic routes the crystal controlled clock to the output. If TICKLER is low, the PLL synchronized to the incoming READ DATA will generate RCLOCK. This clock is then routed to the output signal RCLOCK/WCLOCK.
RCLOCK/ WCLOCK	7	O	**Read Clock/Write Clock:** RCLOCK is the output when the TICKLER signal is low. As an output, it is the clock phase locked onto the incoming READ DATA signal. RCLOCK is twice the data frequency. WCLOCK is the output of the crystal oscillator, divided internally by 2, and will output continuously while the DPLL is enabled and the TICKLER signal is high. WCLOCK defines the bit cell frequency.
PRE-COMP ENN	13	I	**Pre-Compensation Enable:** Active low. When PRE-COMP ENN is high, no write compensation is applied to the outgoing data. When it is low, the data stream is write pre-compensated.
FREQ PUMP	14	O	**Frequency Pump Error Signal:** Current output which is summed through a resistor along with P UP and P DOWN. The three outputs are then used to charge or discharge a capacitor which generates an error voltage for the VCO.
P DOWN	15	O	**Pump Down Error Signal:** Current output which is summed through a resistor along with FREQ PUMP and P UP. The three outputs are then used to charge or discharge a capacitor which generates an error voltage for the VCO.
P UP	16	O	**Pump Up Error Signal:** Current output which is summed through a resistor along with FREQ PUMP and P DOWN. The three outputs are then used to charge or discharge a capacitor which generates an error voltage for the VCO.
VCO CLK	3	I	**Variable Clock:** Generated by an external VCO.
CRYSTAL X1	6	I	**Crystal 1:** Input connection provided to attach a crystal for the internal oscillator. The crystal frequency is defined to be twice the data bit rate.
CRYSTAL X2	5	I	**Crystal 2:** Input connection provided to attach a crystal for the internal oscillator. The crystal frequency is defined to be twice the data bit rate.
EARLY SIG	17	O	**Early Data Signal:** Active high. Used as the input to a user supplied delay line or delay circuit. The delays are determined by the requirements of the particular disk unit to which the DPLL is attached. If pre-compensation delays are enabled by the signal PRE-COMP ENN, this signal together with NOMINAL SIG and LATE SIG are used to generate the WRITE DATA signal.
NOMINAL SIG	11	I	**Nominal Data Signal:** Active high. This input is used by the DPLL together with the EARLY SIG output and the LATE SIG to generate the write pre-compensation delays. The user should insert a delay line between the EARLY SIG output and the NOM SIG input and between the output of the first delay line and the LATE SIG input (these delays being the delay between an early and nominal signal or a nominal and late signal, respectively). The values of these depend on the disk drive to be used. If pre-compensation is not enabled, NOMINAL SIG is used to generate the WRITE DATA signal. In systems where pre-compensation is never used, the EARLY SIG output should be connected to the NOMINAL SIG input.
LATE SIG	9	I	**Late Signal:** Active high. This input is used by the DPLL together with the NOMINAL SIG to generate the write pre-compensation delays. The user should insert a delay line between the NOM SIG input and the LATE SIG input. The value depends on the disk drive to be used.
READ DATA	12	I	**Read Data:** Active high. This is the composite clock and data read from the disk unit. It is used as the incoming signal for the phase lock loop.
WRITE DATA	18	O	**Write Data:** Active high. This is the output signal, write pre-compensated if so enabled, formed from the WRDAT and WRCLK inputs.
REDAT	4	O	**Composite Read Data:** Active High. REDAT is the output signal which reflects the READ DATA input signal but synchronized to the RCLOCK generated by the internal PLL. The REDAT signal will be asserted for one period of the RCLOCK signal following the assertion of READ DATA.
V_{CC}	20	I	**+5V ±5% power input.**
GND	10	I	**Signal and power ground input.**

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DPLL FUNCTIONS

Read/Write Clock

The DPLL provides a read/write clock for the IMDC. This clock is either derived from a crystal or from a PLL locking onto the combined data and clock stream from the disk.

Generation of the Output Data

The DPLL inputs two pieces of information, the NRZ data and clock information bits in parallel, from the IMDC. It combines them into the same cell by issuing the clock during the first half of the first half of the bit cell time, and the data information during the first half of the second half of the bit cell time. This information then becomes the WRITE DATA signal which goes to the disk drive.

Pre-Compensation

In addition, the DPLL provides facilities for pre-compensating the data during the writing of the data to disk. The write pre-compensating algorithm is built into the chip. Note that this feature can be disabled where necessary.

The logic in the DPLL does the pre-compensation algorithm in a slightly different manner than with a ROM lookup table. If the different data and clock patterns which require compensation are drawn out, only two patterns are found. The two patterns are a series of ones followed by a zero, or a series of zeros followed by a one. By using a shift register and simple logic, the signals necessary for gating early, late, and nominal can be determined (the last being the absence of the previous two). This is the method which is implemented in the DPLL.

PLL Function

With a phase locked loop (PLL) circuit in the read chain, the data can be recovered more accurately. The PLL provides a clock signal which is derived from the read data stream and tracks it through a reasonable variation. The clock signal is used by the decoding hardware to sample the read data stream.

Delay Lines

The delay lines referred to in this document can be purchased as a single unit or constructed with logic and passive components. The delay line, typically, has a single input with several outputs. The outputs reflect the input but delayed by some period of time. A delay line for an eight inch MFM floppy disk drive, for example, would have each output delayed 175nsec from the other. The first output is delayed 175nsec from the input and the second output is delayed 175nsec from the first output. The delay time actually used in each application would be the function of the disk drive and specified by the manufacturer.

OPERATION

The PLL in the DPLL is intended to be used with an external VCO. As shown in figure 1, the DPLL interfaces between the IMDC and the disk unit. The only other attachments are the resistors and capacitor for the external VCO. These values should be chosen for the operating characteristic required by the system. For IBM System 34 interfaces, the decode of side zero, track zero, would be used for the PRE-SCALEN input. This input would then automatically divide the crystal controlled clock output for RCLOCK/WCLOCK. The crystal used with the DPLL should be twice the data rate for the interfaced disk unit.

DESIGN NOTE

Refer to figure 1 (R1 > R2 > R3). The recommended values are:

R1 = 100K ohms
R2 = 10K ohms
R3 = 1K ohms

R1 X C1 = 5 X period
R2 X C1 = 50 X period
R3 X C1 = 500 X period

Clock Considerations

The on-chip oscillator can be controlled by either one of the following methods:

1. Crystal – if precise timing is required.
2. External drive – If application requires that the DPLL be driven from a system clock.

Crystal Timing

When a crystal is used, the on-chip oscillator operates at the resonant frequency (f_0) of the crystal. The series-resonant quartz crystal connects to the DPLL via pins 6 (CRYSTAL X1) and 5 (CRYSTAL X2). The lead lengths of the crystal should be approximately equal, and as short as possible. Also, the timing circuits should not be in close proximity to external sources of noise. The crystal should be hermetically sealed (HC type can) and have the following electrical characteristics:

Type – Fundamental mode, series resonant
Impedance at fundamental – 35ohms maximum
Impedance at harmonics and spurs – 50ohms minimum

The resonant frequency (f_0) of the crystal is related to the desired cycle time (T) by the equation: $f_0 = 2/T$, thus for a cycle time of 200 nanoseconds, f_0 = 10MHz. The DPLL will operate at crystal controlled frequencies from 4MHz to 20MHz.

Using an External Clock

The DPLL can be synchronized with an external clock by simply connecting the appropriate drive circuits to the CRYSTAL X1 and CRYSTAL X2 inputs (see figure 2.)

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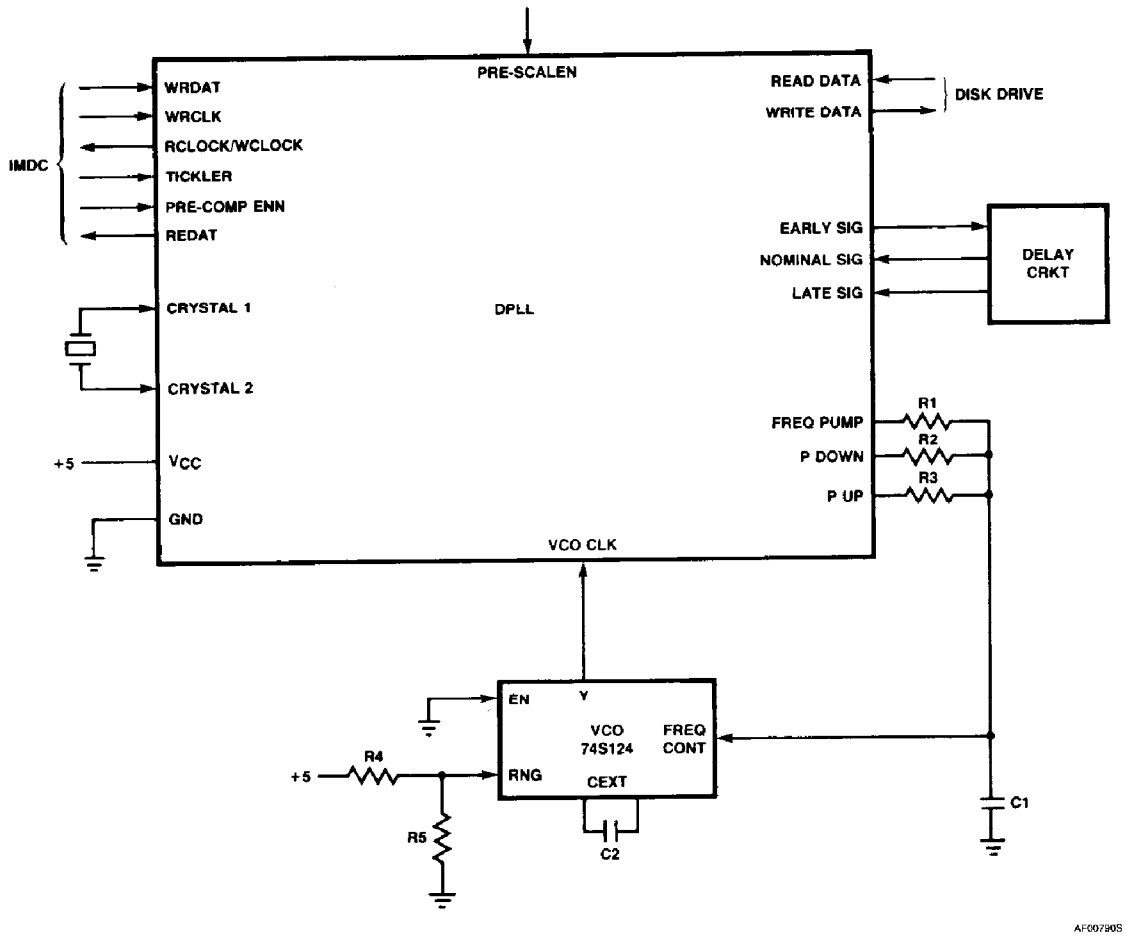

Figure 1. Typical Application

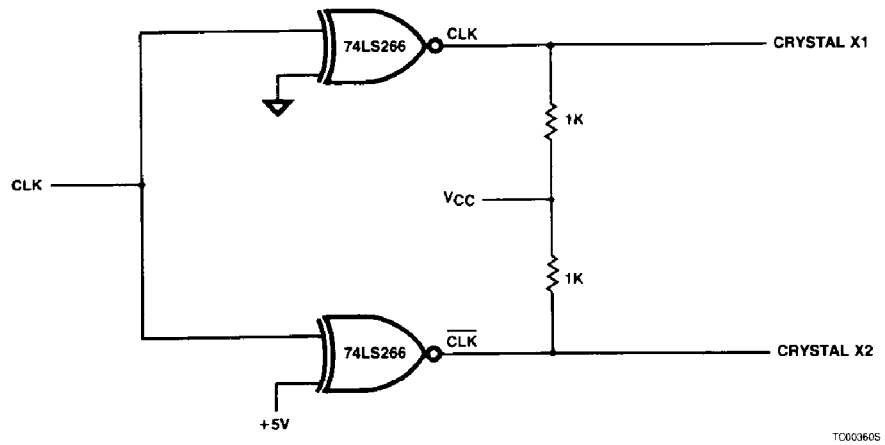

Figure 2. Recommended Clock Circuitry

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Supply voltage	−0.5 to +7.0	V
Input voltage	−0.5 to +5.5	V
Operating temperature range[2]	0 to +70	°C
Storage temperature	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±5%, T_A = 0°C to +70°C [3,4,7]

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Max	UNIT
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.0		V
V_{OL}	Output low voltage	I_{OUT} = 5.3mA		0.4	V
V_{OH}	Output high voltage	I_{OUT} = −400μA	2.4		V
	All outputs except open collector[5]				
I_{IL}	Input low current	V_{IN} = 0.4V		−400	μA
I_{IH}	Input high current	V_{IN} = 2.4V		20	μA
I_{OC}	Open collector off state current[5]	V_{OUT} = 2.4V		20	μA
I_{SC}	Output short circuit current[6]	V_{CC} = max	−40	−100	mA
I_{CC}	V_{CC} supply current	V_{CC} = max		130	mA

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or at any other conditions other than those indicated in the Electrical Characteristics section of this data sheet is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. Parameters are valid over specified temperature range.
4. All voltage measurements are referenced to ground . For testing, all signals swing between 0.4V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
5. P DOWN is an open collector output.
6. No more than one output should be connected to ground at one time.
7. Capacitive test load is 100pF for all pins.

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AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $+70°C$[3, 4] (see figures 3 – 10)

NO.	FIGURE	CHARACTERISTIC	TENTATIVE LIMITS		UNITS
			Min	Max	
1	3	CLK low pulse width	25		ns
2	3	CLK high pulse width	25		ns
3	3	CLK period	50		ns
4	4	READ DATA low to RCLOCK/WCLOCK high		5	ns
5	4	RCLOCK/WCLOCK low to REDAT high		10	ns
6	4	READ DATA high pulse width	10		ns
7	4	READ DATA high to RCLOCK/WCLOCK low	20		ns
8	5	CRYSTAL X1 low to RCLOCK/WCLOCK low		65	ns
9	5	CRYSTAL X1 low to RCLOCK/WCLOCK high		65	ns
10	5	VCO CLK low to RCLOCK/WCLOCK high		30	ns
11	5	VCO CLK high to RCLOCK/WCLOCK low		30	ns
12	6	VCO CLK high to P DOWN low		20	ns
13	6	VCO CLK low to P DOWN three-state		20	ns
14	7	VCO CLK low to P UP three-state		20	ns
15	7	READ DATA high to P UP high		20	ns
16	8	VCO CLK high to FREQ PUMP high		40	ns
17	8	VCO CLK high to FREQ PUMP three-state		40	ns
18	8	CRYSTAL X1 high to FREQ PUMP low		40	ns
19	8	CRYSTAL X1 high to FREQ PUMP three-state		40	ns
20	9	WRCLK high to RCLOCK/WCLOCK low	20		ns
21	9	RCLOCK/WCLOCK low to WRCLK low	20		ns
22	9	WRDAT high to RCLOCK/WCLOCK low	20		ns
23	9	RCLOCK/WCLOCK low to WRDAT low	20		ns
24	9	EARLY SIG high pulse width	20	40	ns
25	9, 10	NOMINAL SIG high to WRITE DATA high		20	ns
26	9	CRYSTAL X1 high to EARLY SIG high		40	ns
27	10	EARLY SIG high to NOMINAL SIG high		30	ns
28	10	EARLY SIG high to LATE SIG high		60	ns
29	10	EARLY SIG high to WRITE DATA high		20	ns
30	10	LATE SIG high to WRITE DATA high		20	ns

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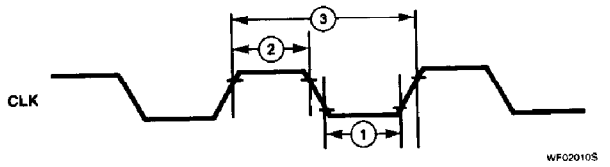

Figure 3. CLK Timing

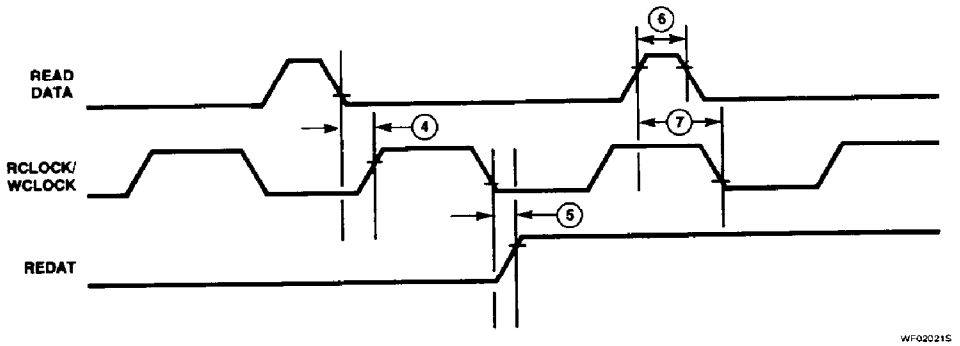

Figure 4. READ DATA/REDAT Timing

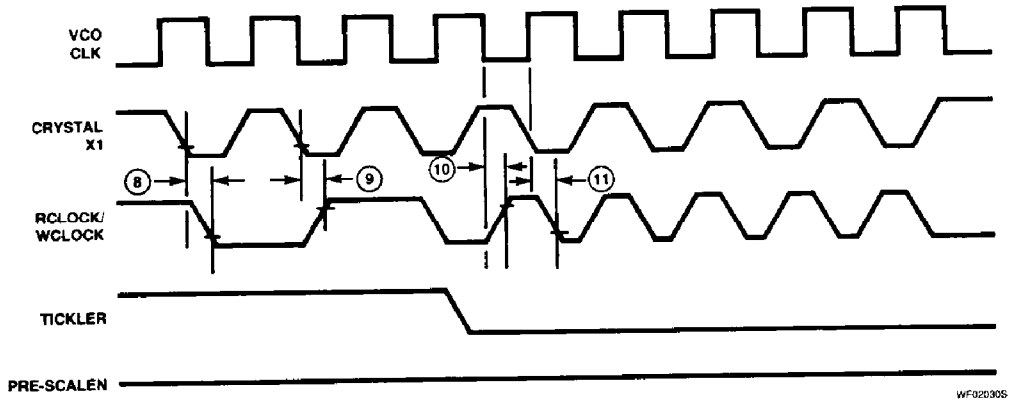

Figure 5. RCLOCK/WCLOCK Timing

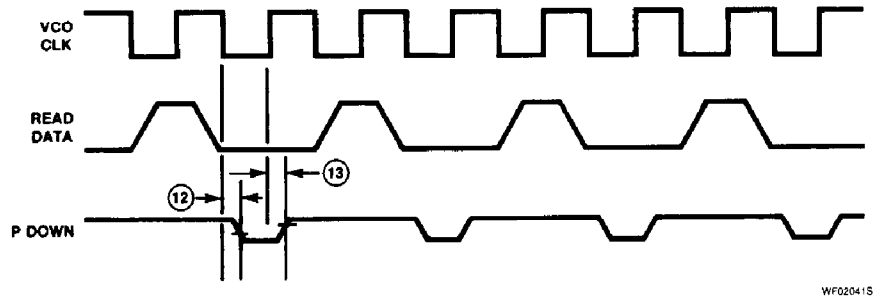

Figure 6. PUMP DOWN Timing

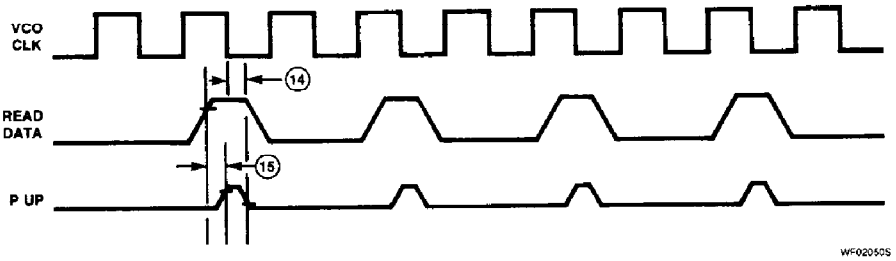

Figure 7. PUMP UP Timing

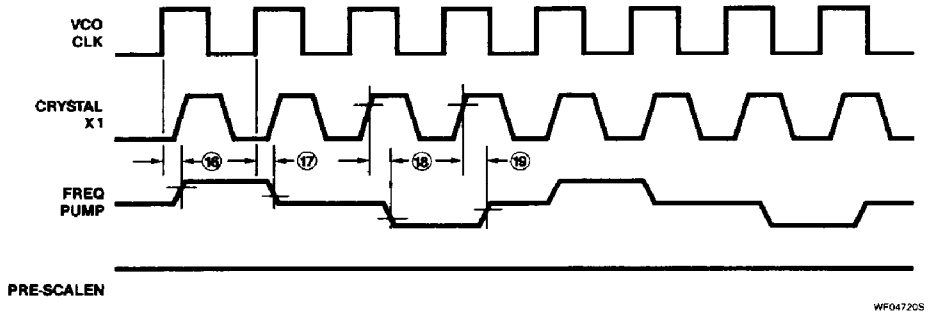

Figure 8. FREQ Pump Timing

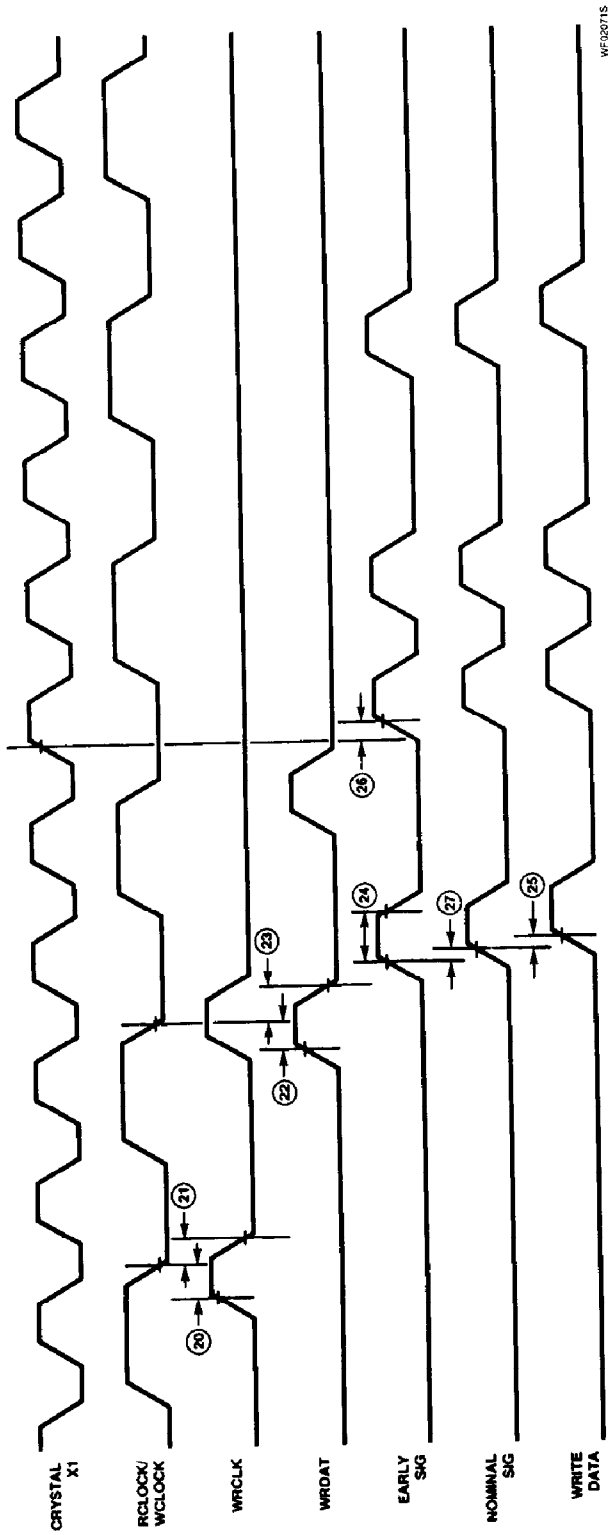

Figure 9. WRITE DATA With PRE-COMP ENN Inactive

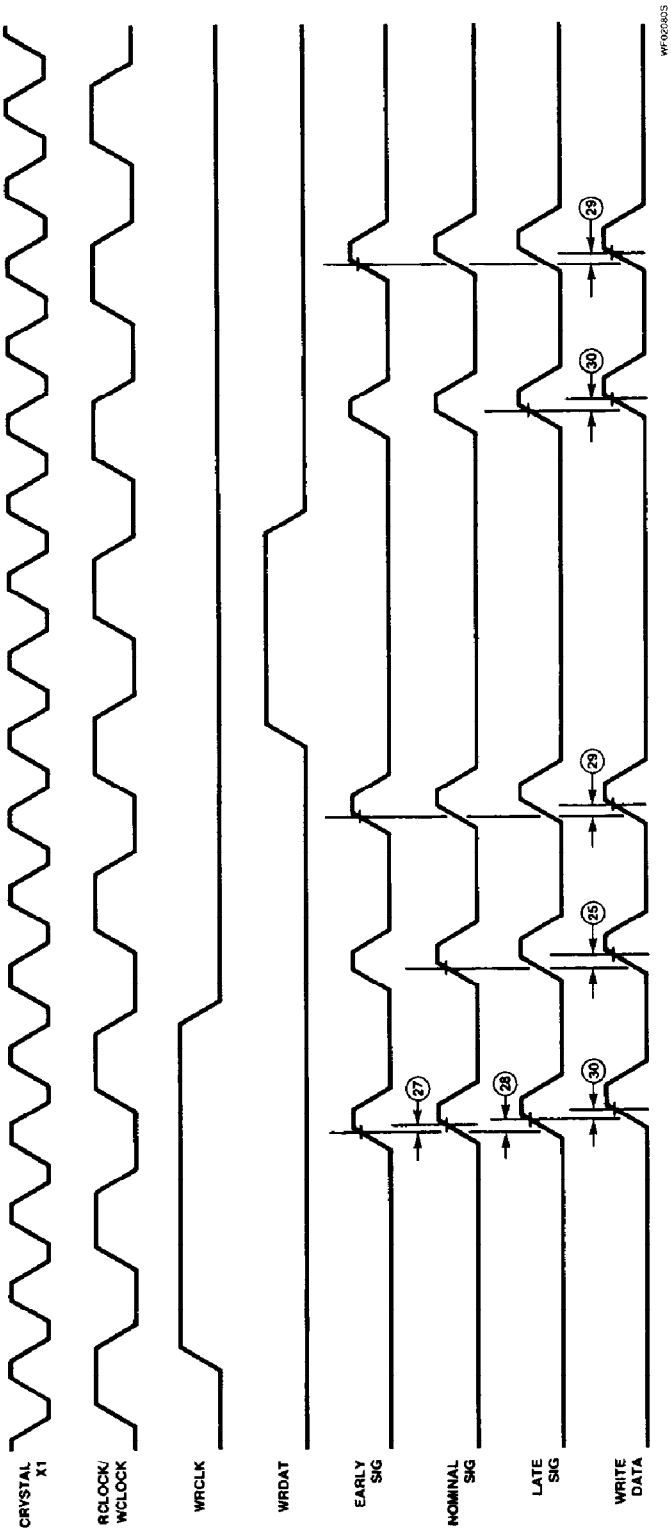

Figure 10. WRITE DATA With PRE-COMP ENN Active