# CA3039

OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

December 2000

## Diode Array

### Features

- **Six Matched Diodes on a Common Substrate**
- **Excellent Reverse Recovery Time . . . . . 1ns (Typ)**
- **$V_F$ Match . . . . . 5mV (Max)**
- **Low Capacitance . . . . . $C_D$ = 0.65pF (Typ) at $V_R$ = -2V**

### Applications

- **Ultra-Fast Low Capacitance Matched Diodes for Applications in Communications and Switching Systems**
- **Balanced Modulators or Demodulators**
- **Ring Modulators**
- **High Speed Diode Gates**
- **Analog Switches**

### Description

The CA3039 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

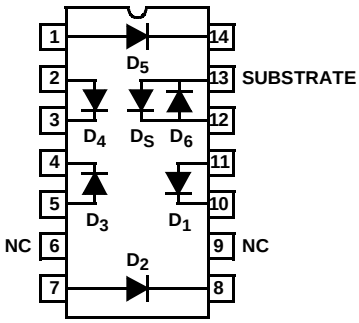
For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

### Part Number Information

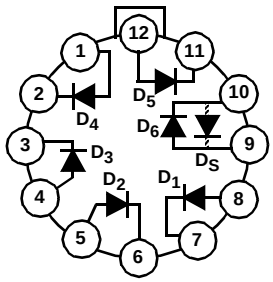
| PART NUMBER | TEMP. RANGE ($^oC$) | PACKAGE | PKG. NO. |
|---|---|---|---|
| CA3039 | -55 to 125 | 12 Pin Metal Can | T12.B |
| CA3039M | -55 to 125 | 14 Ld SOIC | M14.15 |
| CA3039M96 | -55 to 125 | 14 Ld SOIC Tape and Reel | M14.15 |

### Pinouts

**CA3039**
**(SOIC)**
TOP VIEW




**CA3039**
**(METAL CAN)**
TOP VIEW






File Number **343.4**

## Absolute Maximum Ratings

Inverse Voltage (PIV) for: $D_1$ - $D_5$ . . . . . 5V
$D_6$ . . . . . 0.5V
Diode-to-Substrate Voltage ($V_{DI}$) for $D_1$ - $D_5$ . . . . . 20V, -1V
(Terminal 1, 4, 5, 8 or 12 to Terminal 10)
DC Forward Current ($I_F$) . . . . . 25mA
Recurrent Forward Current ($I_F$) . . . . . 100mA
Forward Surge Current ($I_{F(SURGE)}$) . . . . . 100mA

## Operating Conditions

Temperature Range . . . . . -55$^o$C to 125$^o$C

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ ($^o$C/W) | $\theta_{JC}$ ($^o$C/W) |
|---|---|---|
| Metal Can Package | 200 | 120 |
| SOIC Package | 220 | N/A |

Maximum Power Dissipation (Any One Diode) . . . . . 100mW
Maximum Junction Temperature (Metal Can Package) . . . . . 175$^o$C
Maximum Junction Temperature (Plastic Package) . . . . . 150$^o$C
Maximum Storage Temperature Range . . . . . -65$^o$C to 150$^o$C
Maximum Lead Temperature (Soldering 10s) . . . . . 300$^o$C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

$T_A$ = 25$^o$C; Characteristics apply for each diode unit, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| DC Forward Voltage Drop (Figure 1) | $V_F$ | $I_F$ = 50μA | - | 0.65 | 0.69 | V |
| | | $I_F$ = 1mA | - | 0.73 | 0.78 | V |
| | | $I_F$ = 3mA | - | 0.76 | 0.80 | V |
| | | $I_F$ = 10mA | - | 0.81 | 0.90 | V |
| DC Reverse Breakdown Voltage | $V_{(BR)R}$ | $I_R$ = -10μA | 5 | 7 | - | V |
| DC Reverse Breakdown Voltage Between Any Diode Unit and Substrate | $V_{(BR)R}$ | $I_R$ = -10μA | 20 | - | - | V |
| DC Reverse (Leakage) Current (Figure 2) | $I_R$ | $V_R$ = -4V | - | 0.016 | 100 | nA |
| DC Reverse (Leakage) Current Between Any Diode Unit and Substrate (Figure 3) | $I_R$ | $V_R$ = -10V | - | 0.022 | 100 | nA |
| Magnitude of Diode Offset Voltage (Note 2) (Figure 1) | $\lvert V_{F1} - V_{F2} \rvert$ | $I_F$ = 1mA | - | 0.5 | 5.0 | mV |
| Temperature Coefficient of $\lvert V_{F1} - V_{F2} \rvert$ (Figure 4) | $\frac{\Delta \lvert V_{F1} - V_{F2} \rvert}{\Delta T}$ | $I_F$ = 1mA | - | 1.0 | - | μV/$^o$C |
| Temperature Coefficient of Forward Drop (Figure 5) | $\frac{\Delta V_F}{\Delta T}$ | $I_F$ = 1mA | - | -1.9 | - | mV/$^o$C |
| DC Forward Voltage Drop for Anode-to-Substrate Diode ($D_S$) | $V_F$ | $I_F$ = 1mA | - | 0.65 | - | V |
| Reverse Recovery Time | $t_{RR}$ | $I_F$ = 10mA, $I_R$ = -10mA | - | 1.0 | - | ns |
| Diode Resistance (Figure 6) | $R_D$ | f = 1kHz, $I_F$ = 1mA | 25 | 30 | 45 | Ω |
| Diode Capacitance (Figure 7) | $C_D$ | $V_R$ = -2V, $I_F$ = 0 | - | 0.65 | - | pF |
| Diode-to-Substrate Capacitance (Figure 8) | $C_{DI}$ | $V_{DI}$ = 4V, $I_F$ = 0 | - | 3.2 | - | pF |

NOTE:

2. Magnitude of Diode Offset Voltage is the difference in DC Forward Voltage Drops of any two diode units.

## Typical Performance Curves

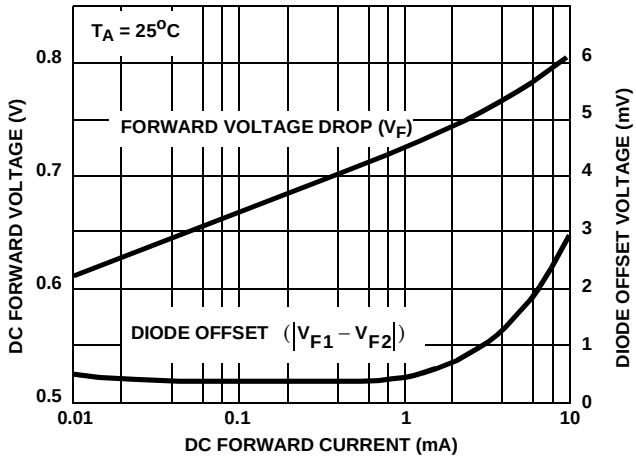



FIGURE 1. DC FORWARD VOLTAGE DROP (ANY DIODE) AND DIODE OFFSET VOLTAGE vs DC FORWARD CURRENT

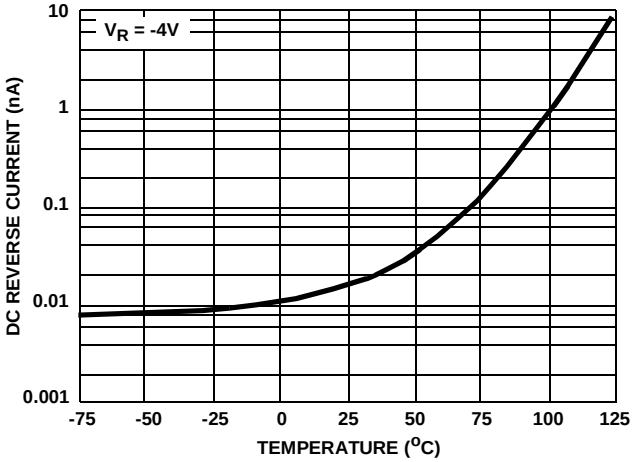



FIGURE 2. DC REVERSE (LEAKAGE) CURRENT ($D_1$ - $D_5$) vs TEMPERATURE

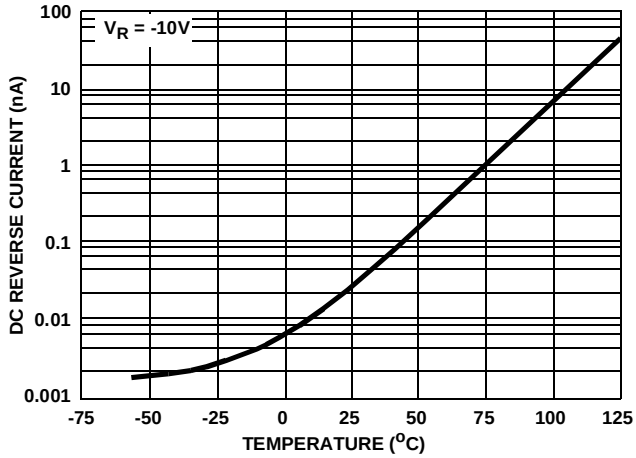



FIGURE 3. DC REVERSE (LEAKAGE) CURRENT BETWEEN $D_1$, $D_2$, $D_3$, $D_4$, $D_5$ AND SUBSTRATE vs TEMPERATURE

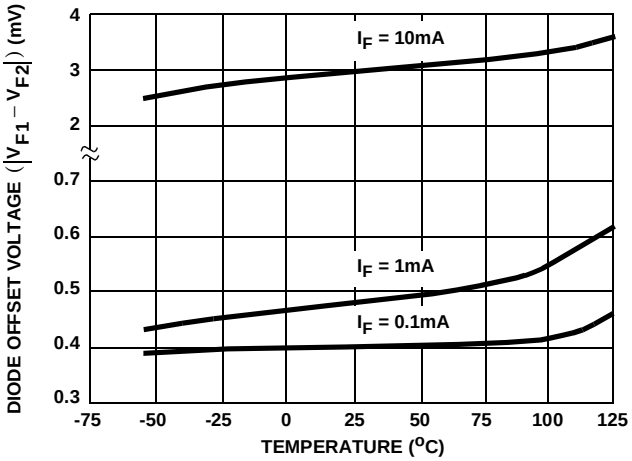



FIGURE 4. DIODE OFFSET VOLTAGE (ANY DIODE) vs TEMPERATURE

## Typical Performance Curves (Continued)

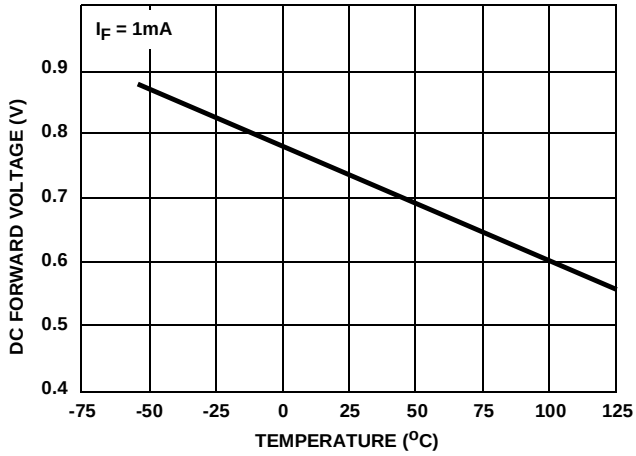



FIGURE 5. DC FORWARD VOLTAGE DROP (ANY DIODE) vs TEMPERATURE

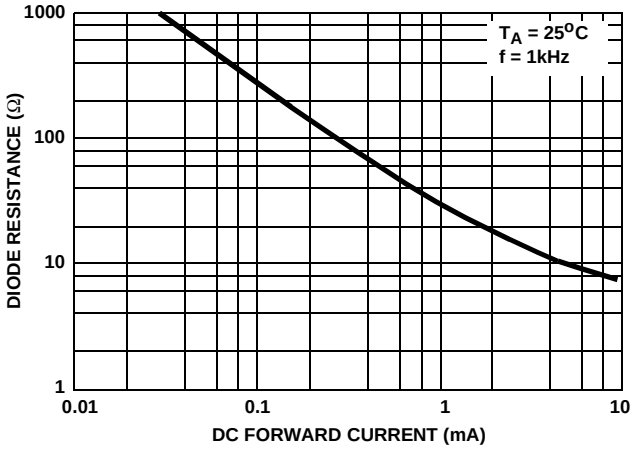



FIGURE 6. DIODE RESISTANCE (ANY DIODE) vs DC FORWARD CURRENT

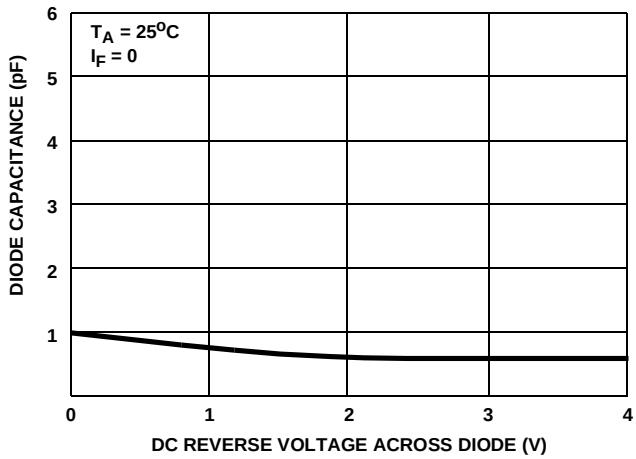



FIGURE 7. DIODE CAPACITANCE ($D_1$ - $D_5$) vs REVERSE VOLTAGE

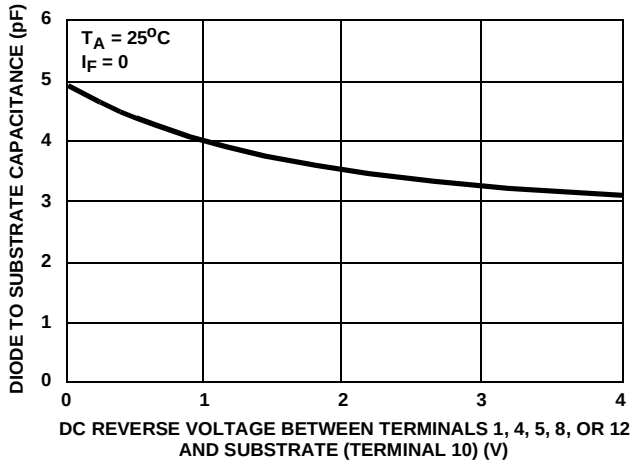



FIGURE 8. DIODE-TO-SUBSTRATE CAPACITANCE vs REVERSE VOLTAGE