



# STS12NF30L

## N-channel 30 V, 0.008 $\Omega$ , 12 A STripFET™ II Power MOSFET in SO-8 package

Datasheet — production data

### Features

| Order code | V <sub>DSS</sub> | R <sub>DS(on)</sub> | I <sub>D</sub> |
|------------|------------------|---------------------|----------------|
| STS12NF30L | 30 V             | < 0.009 $\Omega$    | 12 A           |

- Standard outline for easy automated surface mount assembly
- Low threshold drive

### Applications

- Switching application

### Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

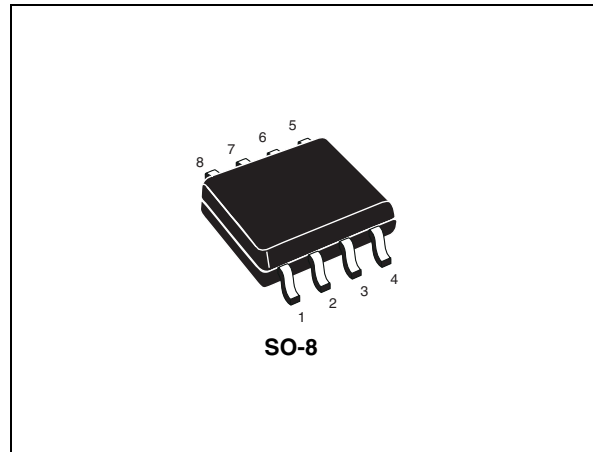


Figure 1. Internal schematic diagram

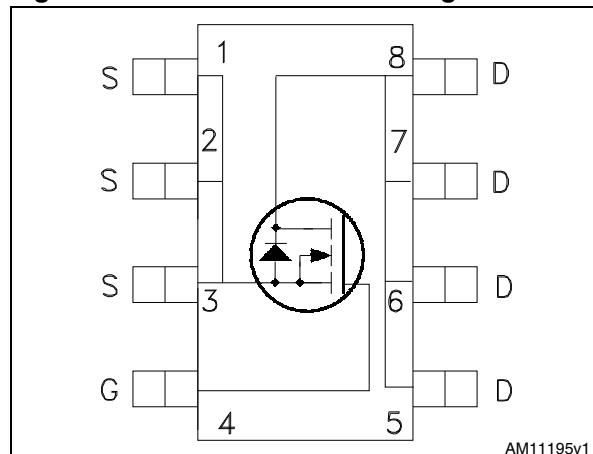


Table 1. Device summary

| Order code | Marking | Package | Packaging     |
|------------|---------|---------|---------------|
| STS12NF30L | 12F30L  | SO-8    | Tape and reel |

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol         | Parameter                                                       | Value      | Unit             |
|----------------|-----------------------------------------------------------------|------------|------------------|
| $V_{DS}$       | Drain-source voltage                                            | 30         | V                |
| $V_{GS}$       | Gate- source voltage                                            | $\pm 16$   | V                |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$  | 12         | A                |
| $I_D$          | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 7.5        | A                |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                          | 48         | A                |
| $P_{TOT}$      | Total dissipation at $T_a = 25\text{ }^\circ\text{C}$           | 2.5        | W                |
| $T_J$          | Maximum operating junction temperature                          | 150        | $^\circ\text{C}$ |
| $T_{stg}$      | Storage temperature                                             | -55 to 150 | $^\circ\text{C}$ |

1. Pulse width limited by safe operating area

**Table 3. Thermal data**

| Symbol            | Parameter                               | Value | Unit               |
|-------------------|-----------------------------------------|-------|--------------------|
| $R_{thj-a}^{(1)}$ | Thermal resistance junction-ambient max | 50    | $^\circ\text{C/W}$ |

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu, t < 10 sec

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

| Symbol        | Parameter                                           | Test conditions                                                                             | Min. | Typ.          | Max.           | Unit                           |
|---------------|-----------------------------------------------------|---------------------------------------------------------------------------------------------|------|---------------|----------------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source<br>Breakdown voltage                   | $I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$                                                     | 30   |               |                | V                              |
| $I_{DSS}$     | Zero gate voltage<br>Drain current ( $V_{GS} = 0$ ) | $V_{DS} = 30\text{ V}$<br>$V_{DS} = 30\text{ V}$ , $T_C = 125\text{ °C}$                    |      |               | 1<br>10        | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage<br>current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 16\text{ V}$                                                                  |      |               | $\pm 100$      | nA                             |
| $V_{GS(th)}$  | Gate threshold voltage                              | $V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$                                                | 1    |               |                | V                              |
| $R_{DS(on)}$  | Static drain-source<br>on-resistance                | $V_{GS} = 10\text{ V}$ , $I_D = 6\text{ A}$<br>$V_{GS} = 4.5\text{ V}$ , $I_D = 6\text{ A}$ |      | 0.008<br>0.01 | 0.009<br>0.011 | $\Omega$<br>$\Omega$           |

**Table 5. Dynamic**

| Symbol    | Parameter                       | Test conditions                                               | Min. | Typ. | Max. | Unit |
|-----------|---------------------------------|---------------------------------------------------------------|------|------|------|------|
| $C_{iss}$ | Input capacitance               |                                                               |      | 2400 |      | pF   |
| $C_{oss}$ | Output capacitance              | $V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0$ | -    | 590  |      | pF   |
| $C_{rss}$ | Reverse transfer<br>capacitance |                                                               |      | 200  |      | pF   |
| $Q_g$     | Total gate charge               | $V_{DD} = 24\text{ V}$ , $I_D = 12\text{ A}$ ,                |      | 35   | 50   | nC   |
| $Q_{gs}$  | Gate-source charge              | $V_{GS} = 4.5\text{ V}$                                       | -    | 9    |      | nC   |
| $Q_{gd}$  | Gate-drain charge               | (see Figure 13)                                               |      | 18   |      | nC   |

**Table 6. Switching times**

| Symbol        | Parameter             | Test conditions                                                                                                      | Min. | Typ. | Max. | Unit |
|---------------|-----------------------|----------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$   | Turn-on delay time    | $V_{DD} = 15\text{ V}$ , $I_D = 6\text{ A}$ ,<br>$R_G = 4.7\ \Omega$ ,<br>$V_{GS} = 4.5\text{ V}$<br>(see Figure 12) | -    | 35   | -    | ns   |
| $t_r$         | Rise time             |                                                                                                                      |      | 90   |      |      |
| $t_{d(off)}$  | Turn-off-delay time   | (see Figure 12)                                                                                                      | -    | 80   | -    | ns   |
| $t_f$         | Fall time             |                                                                                                                      |      | 35   |      | ns   |
| $t_{r(Voff)}$ | Off-voltage rise time | $V_{DD} = 24\text{ V}$ , $I_D = 12\text{ A}$ ,<br>$R_G = 4.7\ \Omega$ , $V_{GS} = 4.5\text{ V}$<br>(see Figure 14)   | -    | 35   | -    | ns   |
| $t_f$         | fall time             |                                                                                                                      |      | 35   |      | ns   |
| $t_c$         | cross-over time       |                                                                                                                      |      | 80   |      | ns   |

**Table 7. Source drain diode**

| Symbol          | Parameter                     | Test conditions                                                                                                                                    | Min. | Typ. | Max | Unit |    |
|-----------------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-----|------|----|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                    | -    |      | 12  | A    |    |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                    | -    |      | 48  | A    |    |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 12\text{ A}, V_{GS} = 0$                                                                                                                 | -    |      | 1.3 | V    |    |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 12\text{ A}, V_{DD} = 15\text{ V}$<br>$di/dt = 100\text{ A}/\mu\text{s},$<br>$T_j = 150\text{ }^\circ\text{C}$<br><i>(see Figure 14)</i> | -    | 114  |     | ns   |    |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                    |      |      |     | 456  | nC |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                    |      |      |     | 8    | A  |

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

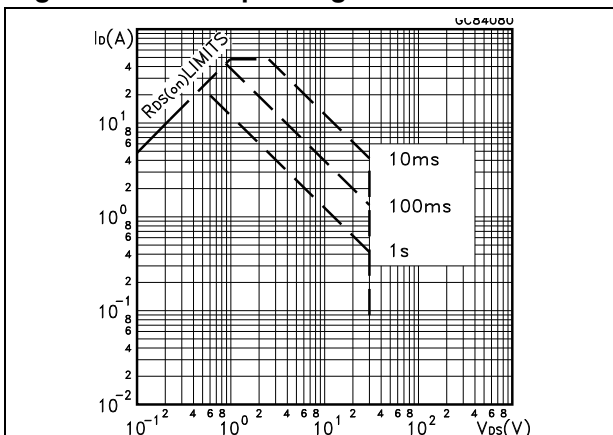


Figure 3. Thermal impedance

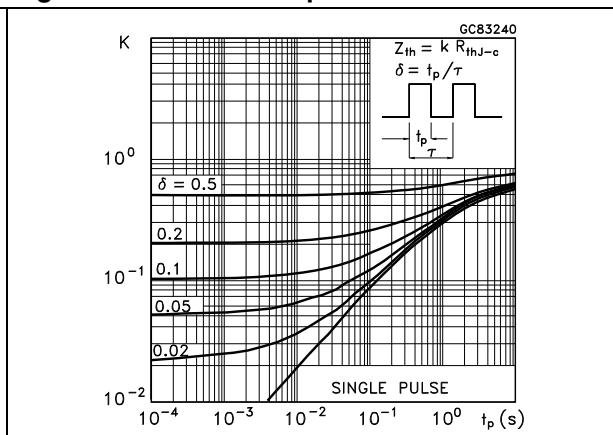


Figure 4. Output characteristics

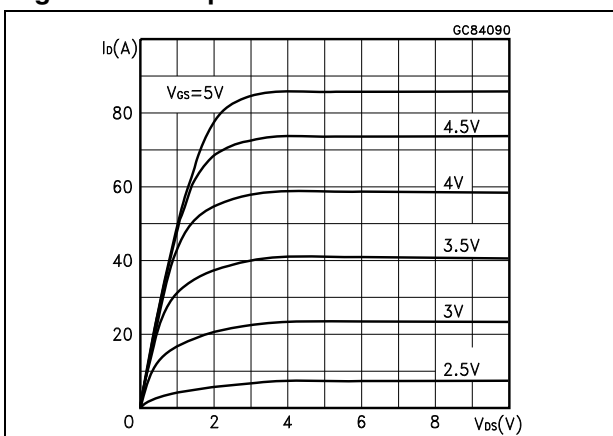


Figure 5. Transfer characteristics

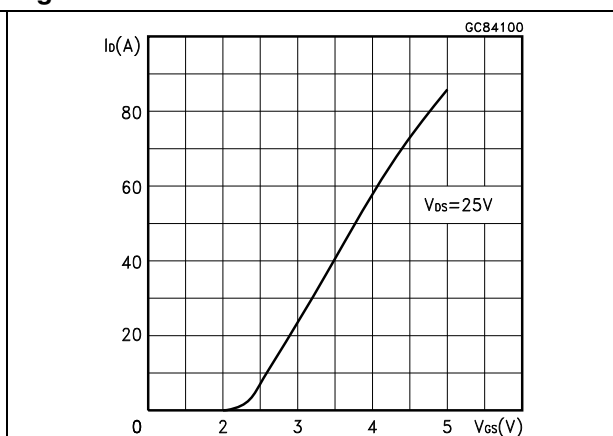


Figure 6. Source-drain diode forward characteristics

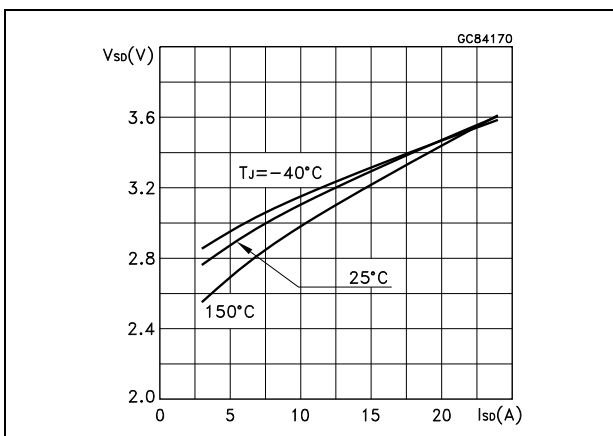


Figure 7. Static drain-source on resistance

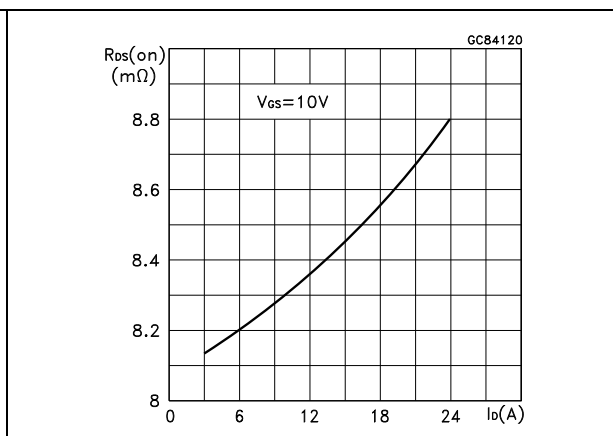


Figure 8. Gate charge vs. gate-source voltage

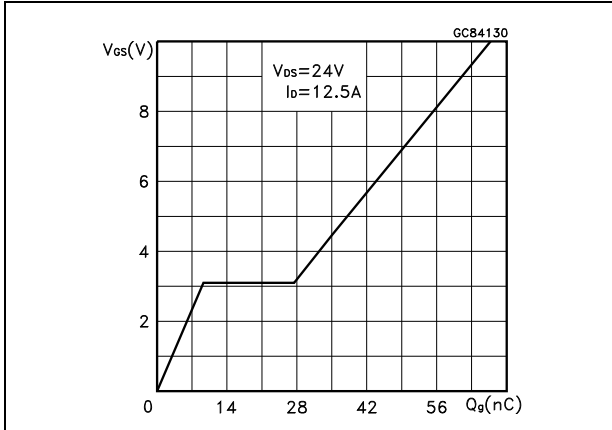


Figure 9. Capacitance variations

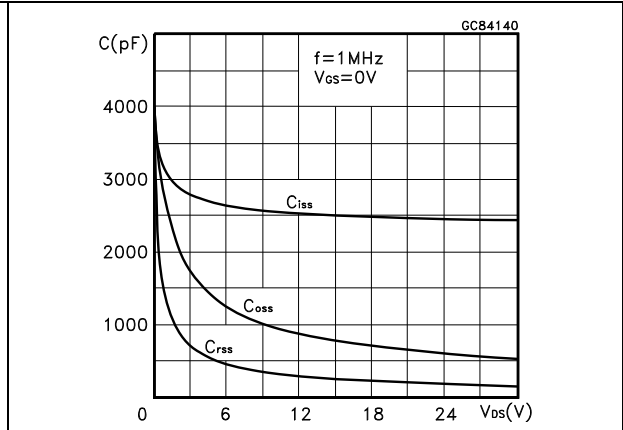


Figure 10. Normalized gate threshold voltage vs. temperature

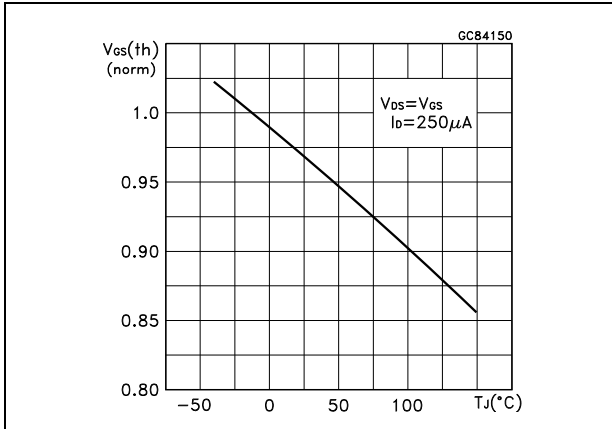
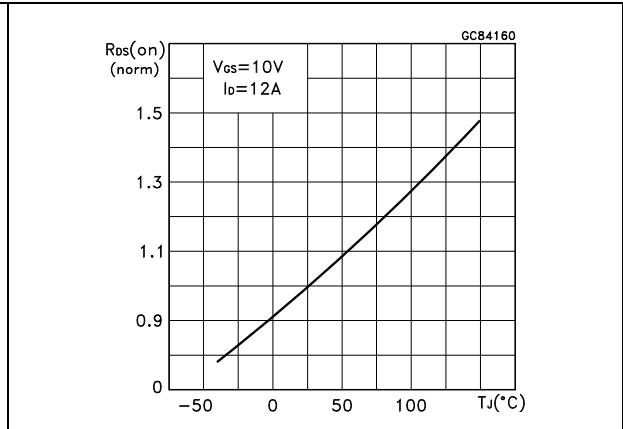
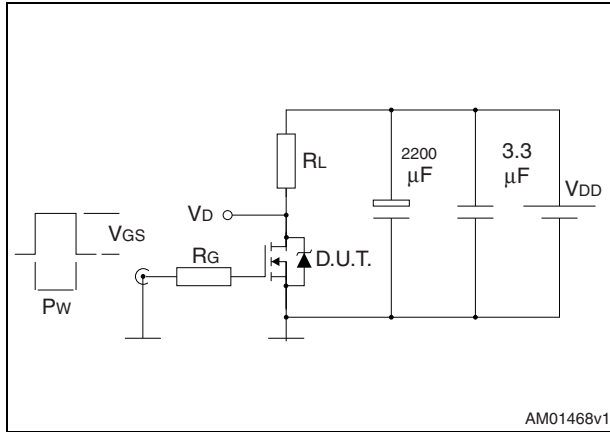


Figure 11. Normalized on-resistance vs. temperature

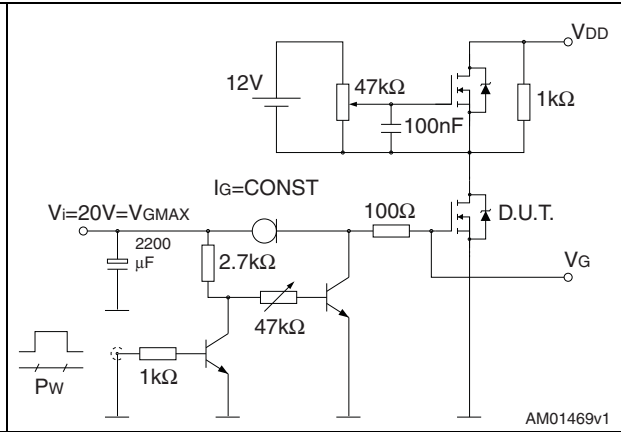


### 3 Test circuit

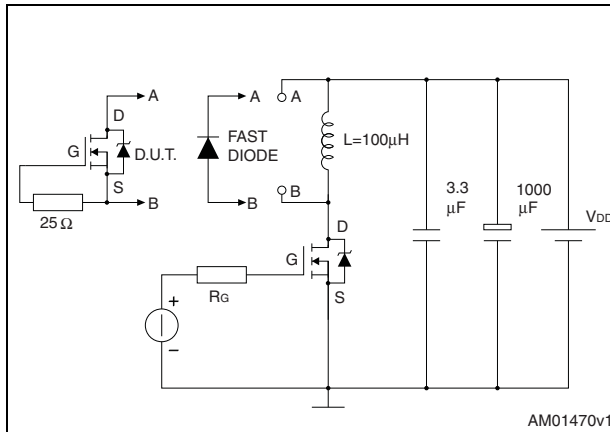
**Figure 12. Switching times test circuit for resistive load**



**Figure 13. Gate charge test circuit**



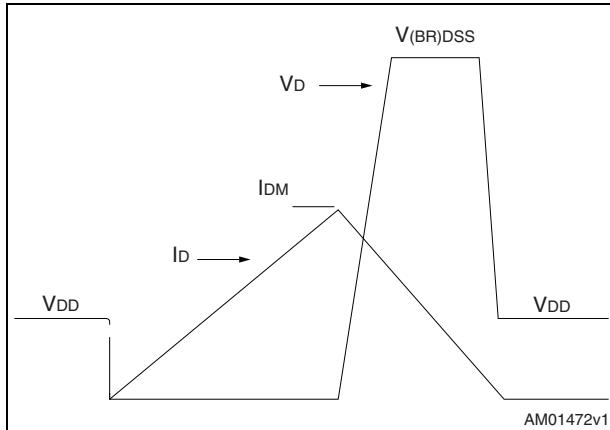
**Figure 14. Test circuit for inductive load switching and diode recovery times**



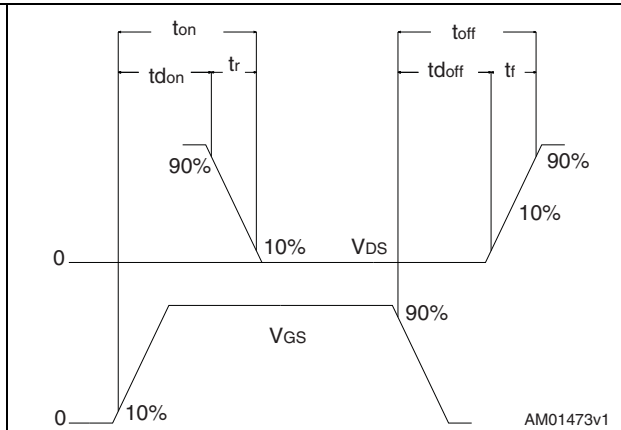
**Figure 15. Unclamped Inductive load test circuit**



**Figure 16. Unclamped inductive waveform**



**Figure 17. Switching time waveform**





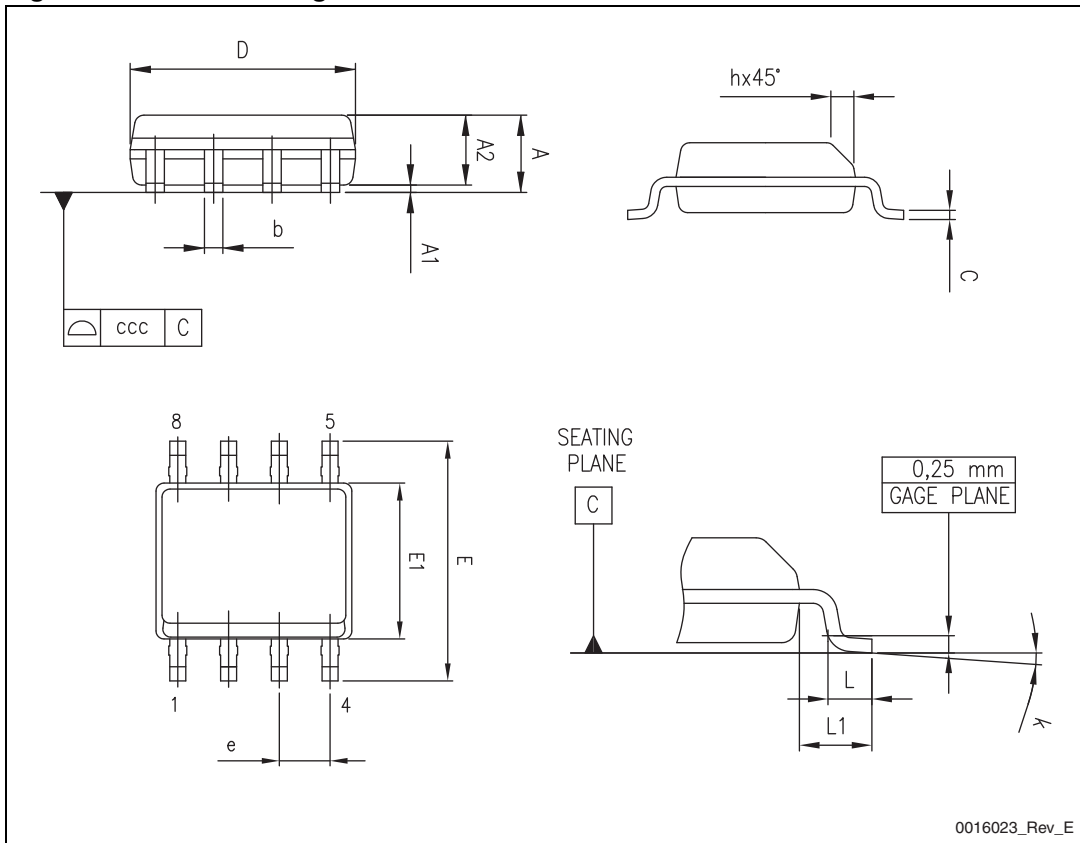
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 8. SO-8 mechanical data

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    |      |      | 1.75 |
| A1   | 0.10 |      | 0.25 |
| A2   | 1.25 |      |      |
| b    | 0.28 |      | 0.48 |
| c    | 0.17 |      | 0.23 |
| D    | 4.80 | 4.90 | 5.00 |
| E    | 5.80 | 6.00 | 6.20 |
| E1   | 3.80 | 3.90 | 4.00 |
| e    |      | 1.27 |      |
| h    | 0.25 |      | 0.50 |
| L    | 0.40 |      | 1.27 |
| L1   |      | 1.04 |      |
| k    | 0°   |      | 8°   |
| ccc  |      |      | 0.10 |

Figure 18. SO-8 drawing



## 5 Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes                                                                            |
|-------------|----------|------------------------------------------------------------------------------------|
| 09-Sep-2004 | 6        | Complete version                                                                   |
| 17-Aug-2006 | 7        | New template, no content change                                                    |
| 31-Jan-2007 | 8        | Typo mistake on <a href="#">Table 2</a> .                                          |
| 08-May-2007 | 9        | Mistake on <a href="#">Table 7</a>                                                 |
| 14-Mar-2012 | 10       | <a href="#">Table 1: Device summary</a> has been corrected.<br>Minor text changes. |

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