



MACRONIX  
INTERNATIONAL Co., LTD.

# MX23C6410

64M-BIT Mask ROM (8/16 Bit Output)  
For SOP and TSOP Packages

## FEATURES

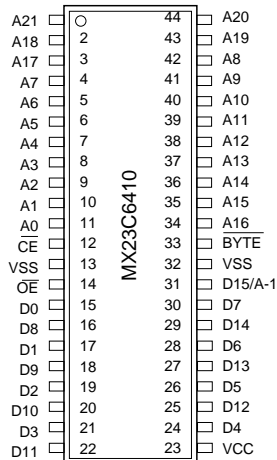
- Bit organization
  - 8M x 8 (byte mode)
  - 4M x 16 (word mode)
- Fast access time
  - Random access: 90ns (max.) for 5V ± 5%
  - 100ns (max.) for 5V ± 10%
- Current
  - Operating: 70mA
  - Standby: 100uA (max.)
- Supply voltage
  - 5V±10%
- Package
  - 44 pin SOP (500 mil)
  - 48 pin TSOP (12mm x 20mm)

## ORDER INFORMATION

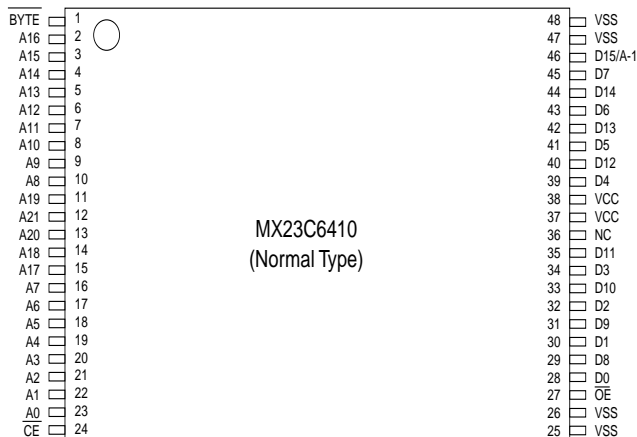
Part No.	Access Time	Package
MX23C6410MC-90	90ns	44 pin SOP
MX23C6410MC-10	100ns	44 pin SOP
MX23C6410MC-12	120ns	44 pin SOP
MX23C6410MC-15	150ns	44 pin SOP
MX23C6410TC-10	100ns	48 pin TSOP
MX23C6410TC-12	120ns	48 pin TSOP
MX23C6410TC-15	150ns	48 pin TSOP
MX23C6410RC-10	100ns	48 pin TSOP (Reverse type)
MX23C6410RC-12	120ns	48 pin TSOP (Reverse type)
MX23C6410RC-15	150ns	48 pin TSOP (Reverse type)

## PIN CONFIGURATION

### 44 SOP



### 48 TSOP (NORMAL TYPE)



### 48 TSOP (REVERSE TYPE)



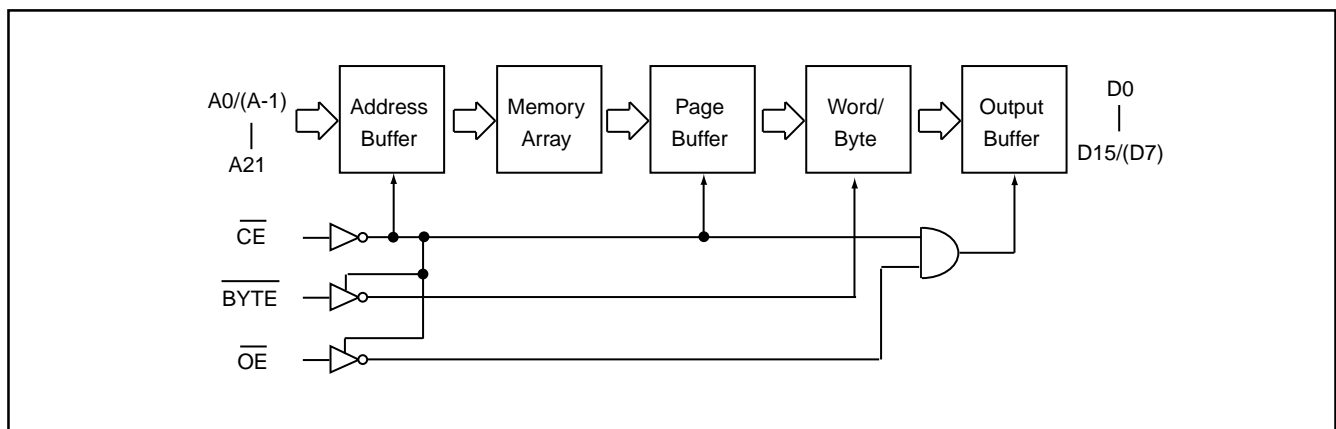
## PIN DESCRIPTION

Symbol	Pin Function
A0~A21	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15 (Word Mode) / LSB Address (Byte Mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
Byte	Word / Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

## MODE SELECTION

$\overline{CE}$	$\overline{OE}$	Byte	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Supply Voltage Relative to VSS	VCC	-0.5V to 6.5V
Voltage on any Pin Relative to VSS	VIN	-0.8V to VCC+2.0V
Ambient Operating Temperature	T <sub>opr</sub>	0°C to 70°C
Storage Temperature	T <sub>stg</sub>	-65°C to 125°C

## DC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 5V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -1.0mA
Output Low Voltage	VOL	-	0.4V	IOL = 2.1mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	70mA	f=5MHz, all output open
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE} = V_{IH}$
Standby Current (cmos)	ISTB2	-	100uA	$\overline{CE} > V_{CC} - 0.2V$
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

## AC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 5V±10%)

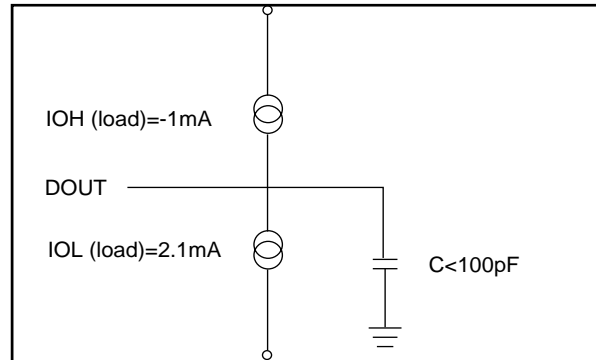
Item	Symbol	<u>23C6410-90*</u>		<u>23C6410-10</u>		<u>23C6410-12</u>		<u>23C6410-15</u>	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	t <sub>RC</sub>	90ns	-	100ns	-	120ns	-	150ns	-
Address Access Time	t <sub>AA</sub>	-	90ns	-	100ns	-	120ns	-	150ns
Chip Enable Access Time	t <sub>ACE</sub>	-	90ns	-	100ns	-	120ns	-	150ns
Output Enable Time	t <sub>OE</sub>	-	45ns	-	50ns	-	60ns	-	70ns
Output Hold After Address	t <sub>OH</sub>	0ns	-	0ns	-	0ns	-	0ns	-
Output High Z Delay	t <sub>HZ</sub>	-	20ns	-	20ns	-	20ns	-	20ns

Note:

- Output high-impedance delay (t<sub>HZ</sub>) is measured from  $\overline{OE}$  or  $\overline{CE}$  going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.
- 90ns speed grade's VCC range : 5V ± 5%.

## AC Test Conditions

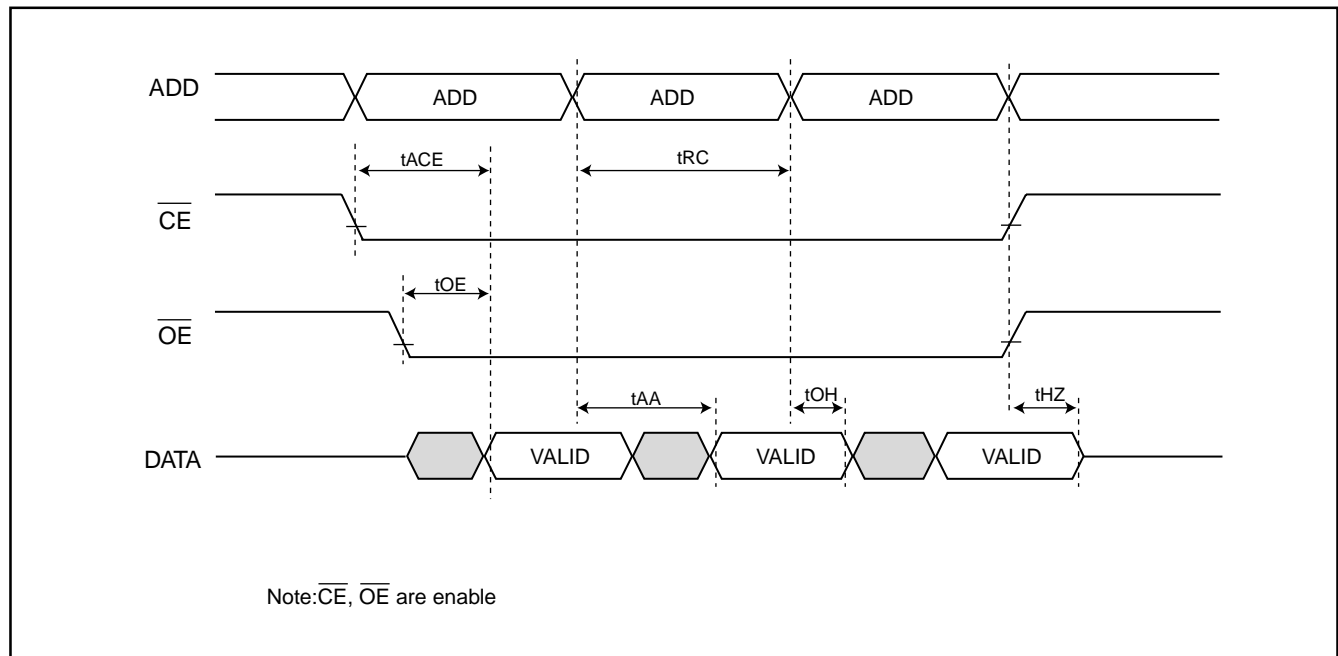
Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure



Note: No output loading is present in tester load board.  
Active loading is used and under software programming control.  
Output loading capacitance includes load board's and all stray capacitance.

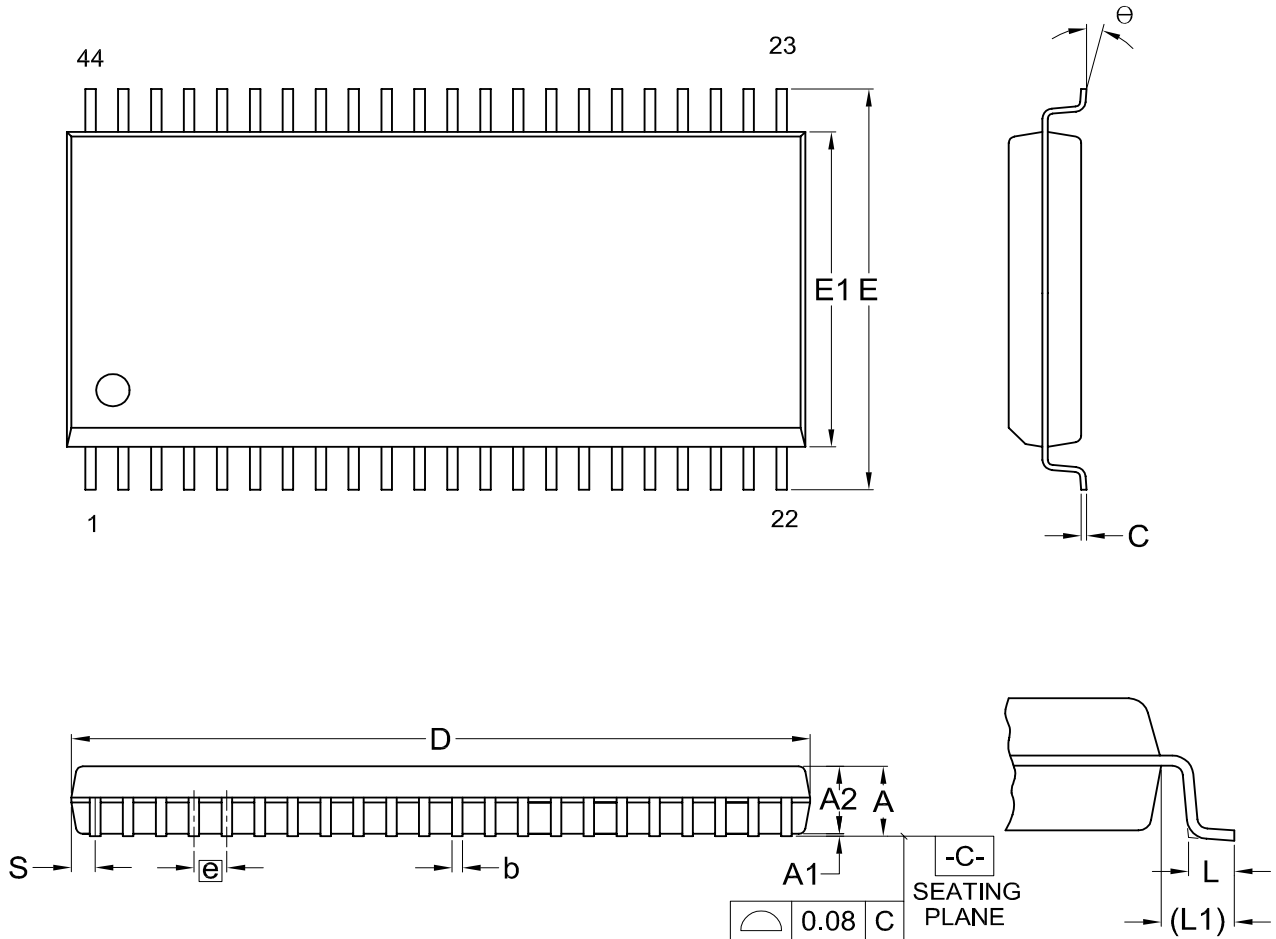
## TIMING DIAGRAM

### RANDOM READ



**PACKAGE INFORMATION**

Title: Package Outline for SOP 44L (500MIL)

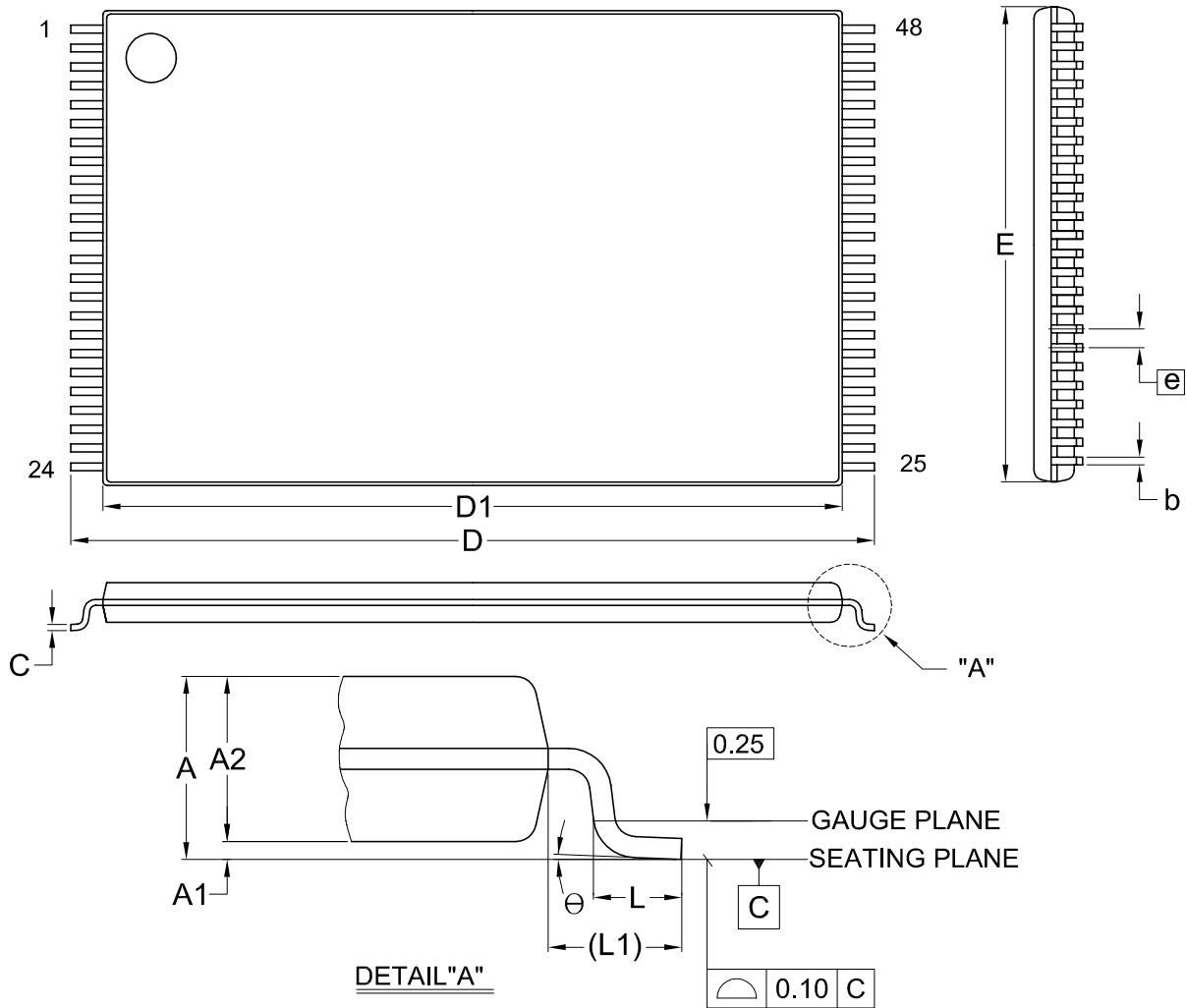


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
UNIT														
mm	Min.	---	0.10	2.59	0.36	0.15	28.37	15.83	12.47		0.56	1.51	0.78	0
	Nom.	---	0.15	2.69	0.41	0.20	28.50	16.03	12.60	1.27	0.76	1.71	0.91	5
	Max.	3.00	0.20	2.80	0.51	0.25	28.63	16.23	12.73		0.96	1.91	1.04	10
Inch	Min.	---	0.004	0.102	0.014	0.006	1.117	0.623	0.491		0.022	0.059	0.031	0
	Nom.	---	0.006	0.106	0.016	0.008	1.122	0.631	0.496	0.050	0.030	0.067	0.036	5
	Max.	0.118	0.008	0.110	0.020	0.010	1.127	0.639	0.501		0.038	0.075	0.041	10

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1405	6	MO-175			11-26-'03

**Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM**

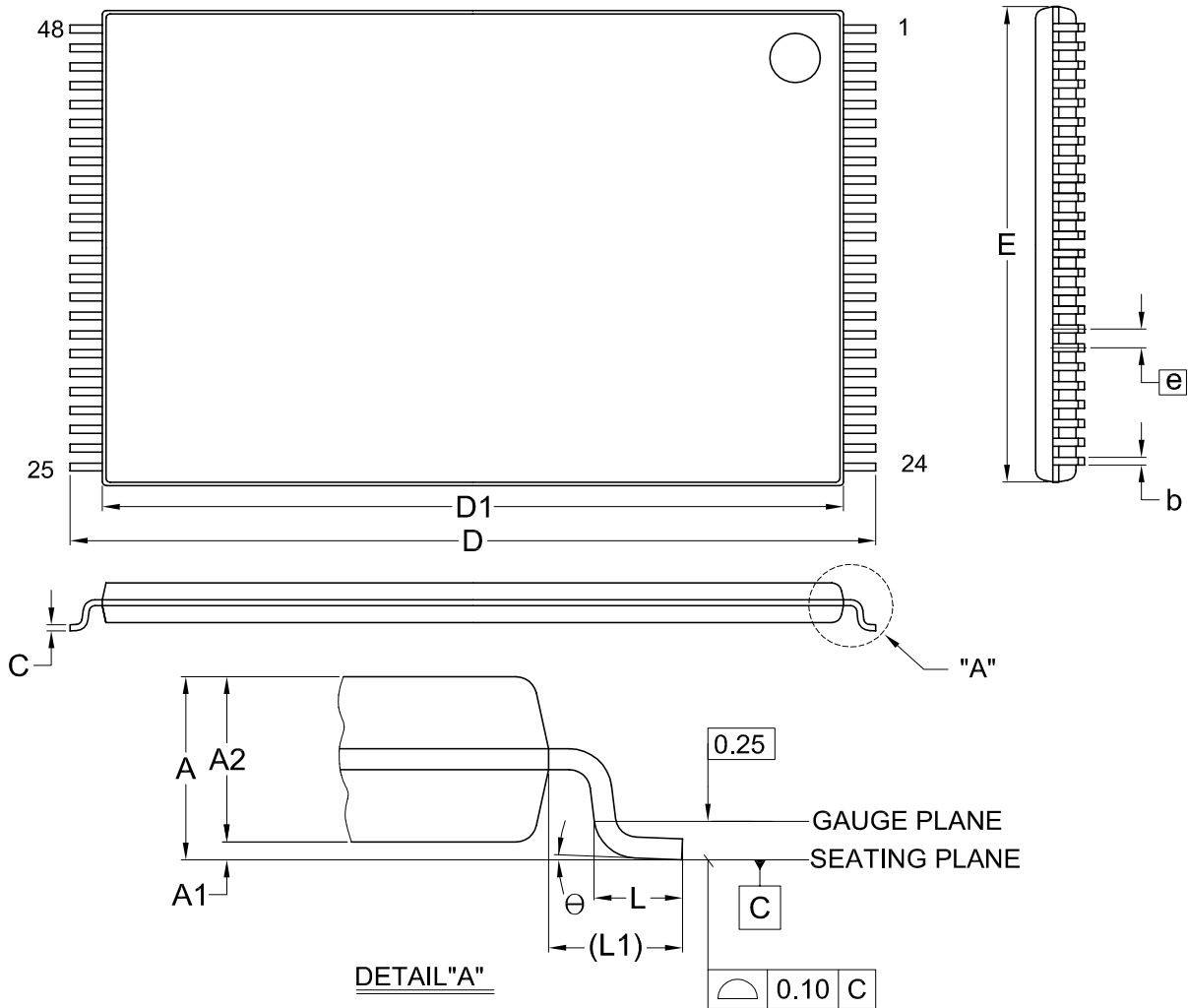


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	D1	E	e	L	L1	θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90	---	0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10	---	0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469	---	0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476	---	0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	8	MO-142			2007/08/03

**Title: Package Outline for TSOP(I) 48L (12X20mm)REVERSE FORM**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	D1	E	e	L	L1	$\Theta$
UNIT													
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90	---	0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10	---	0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469	---	0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476	---	0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607.1	9	MO-142			2007/08/07



**REVISION HISTORY**

<b>Revision</b>	<b>Description</b>	<b>Page</b>	<b>Date</b>
2.1	AC Characteristics: tOH 10ns --> 0ns	P3	FEB/01/1999
2.2	Add Order Information--Note:MX23C6410PC-10 only applies to supply voltage 5V±5%	P1	OCT/02/2000
2.3	Modify Package Information	P5,6,7	OCT/09/2000
2.4	Modify Operating Current:100mA-->70mA	P1,3	JAN/15/2001
2.5	Modify Package Information Added 44-pin TSOP package	P5~7 P1,8	JUL/17/2001
2.6	Move 42-pin PDIP Package to another new data sheet	P1,5	JUL/20/2001
2.7	Removed 44-pin TSOP Package	P1,7	JAN/15/2002
2.8	1. Add supply voltage relative to VSS	P3	JUL/25/2002
2.9	1. Add access time:90ns for 5V± 5%	P1,3	AUG/09/2002
3.0	1. Add 48-TSOP reverse type package information	P7	AUG/21/2002
3.1	Modify Package Information	P5~7	NOV/21/2002





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**MX23C6410**

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