

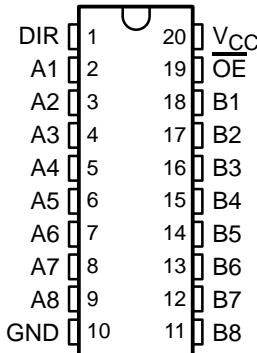
# SN54LS245, SN74LS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDLS146A – OCTOBER 1976 – REVISED FEBRUARY 2002

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce dc Loading on Bus Lines
- Hysteresis at Bus Inputs Improves Noise Margins
- Typical Propagation Delay Times Port to Port, 8 ns

TYPE	$I_{OL}$ (SINK CURRENT)	$I_{OH}$ (SOURCE CURRENT)
SN54LS245	12 mA	-12 mA
SN74LS245	24 mA	-15 mA

SN54LS245 . . . J OR W PACKAGE  
SN74LS245 . . . DB, DW, N, OR NS PACKAGE  
(TOP VIEW)

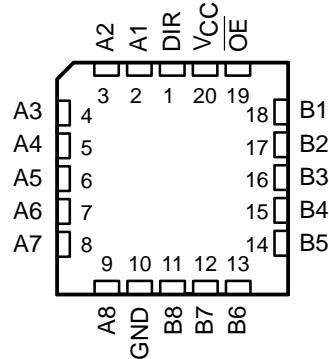


## description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can disable the device so that the buses are effectively isolated.

SN54LS245 . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS245N	SN74LS245N
	SOIC – DW	Tube	SN74LS245DW	LS245
		Tape and reel	SN74LS245DWR	
	SOP – NS	Tape and reel	SN74LS245NSR	74LS245
-55°C to 125°C	SSOP – DB	Tape and reel	SN74LS245DBR	LS245
	CDIP – J	Tube	SN54LS245J	SN54LS245J
		Tube	SNJ54LS245J	SNJ54LS245J
	CFP – W	Tube	SNJ54LS245W	SNJ54LS245W
	LCCC – FK	Tube	SN54LS245FK	SN54LS245FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# SN54LS245, SN74LS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

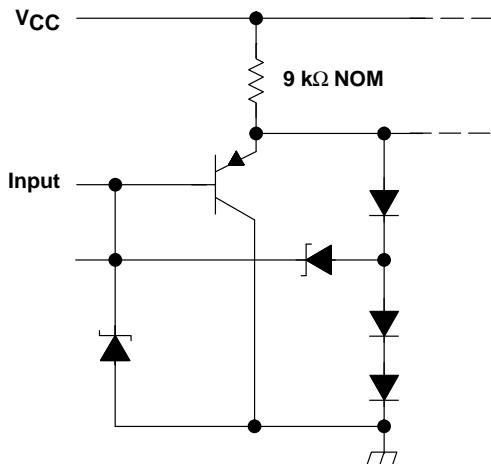
SDLS146A – OCTOBER 1976 – REVISED FEBRUARY 2002

FUNCTION TABLE

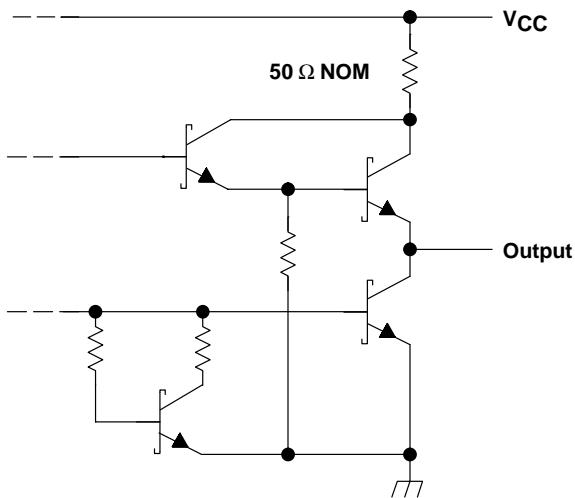
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## schematics of inputs and outputs

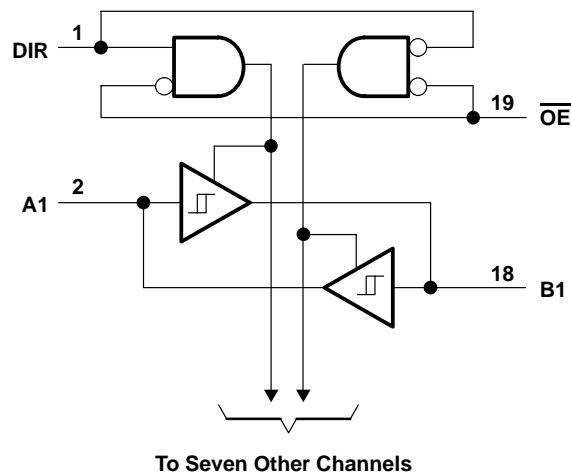
EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



## logic diagram (positive logic)



# **SN54LS245, SN74LS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

SDLS146A – OCTOBER 1976 – REVISED FEBRUARY 2002

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$	.....	7 V
Input voltage, $V_I$ (see Note 1)	.....	7 V
Package thermal impedance, $\theta_{JA}$ (see Note 2):	DB package	70°C/W
	DW package	58°C/W
	N package	69°C/W
	NS package	60°C/W
Storage temperature range, $T_{Stg}$	.....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

#### **recommended operating conditions**

		SN54LS245			SN74LS245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I <sub>OH</sub>	High-level output current			-12			-15	mA
I <sub>OL</sub>	Low-level output current			12			24	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

**SN54LS245, SN74LS245  
OCTAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

SDLS146A – OCTOBER 1976 – REVISED FEBRUARY 2002

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN54LS245			SN74LS245			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub>	High-level input voltage			2		2		V
V <sub>IL</sub>	Low-level input voltage			0.7		0.8		V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5		-1.5	V
Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )	A or B	V <sub>CC</sub> = MIN	0.2	0.4	0.2	0.4		V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> (max)	I <sub>OH</sub> = -3 mA	2.4	3.4	2.4	3.4	V
			I <sub>OH</sub> = MAX	2		2		
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> (max)	I <sub>OL</sub> = 12 mA		0.4		0.4	V
			I <sub>OL</sub> = 24 mA				0.5	
I <sub>OZH</sub>	Off-state output current, high-level voltage applied	V <sub>CC</sub> = MAX, OE at 2 V	V <sub>O</sub> = 2.7 V		20		20	μA
I <sub>OZL</sub>	Off-state output current, low-level voltage applied	V <sub>CC</sub> = MAX, OE at 2 V	V <sub>O</sub> = 0.4 V		-200		-200	μA
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX	V <sub>I</sub> = 5.5 V		0.1		0.1	mA
			V <sub>I</sub> = 7 V		0.1		0.1	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2.7 V		20		20		μA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>IL</sub> = 0.4 V		-0.2		-0.2		mA
I <sub>OS</sub>	Short-circuit output current§	V <sub>CC</sub> = MAX		-40	-225	40	-225	mA
I <sub>CC</sub>	Total, outputs high	V <sub>CC</sub> = MAX		48	70	48	70	mA
	Total, outputs low			62	90	62	90	
	Outputs at high Z			64	95	64	95	

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

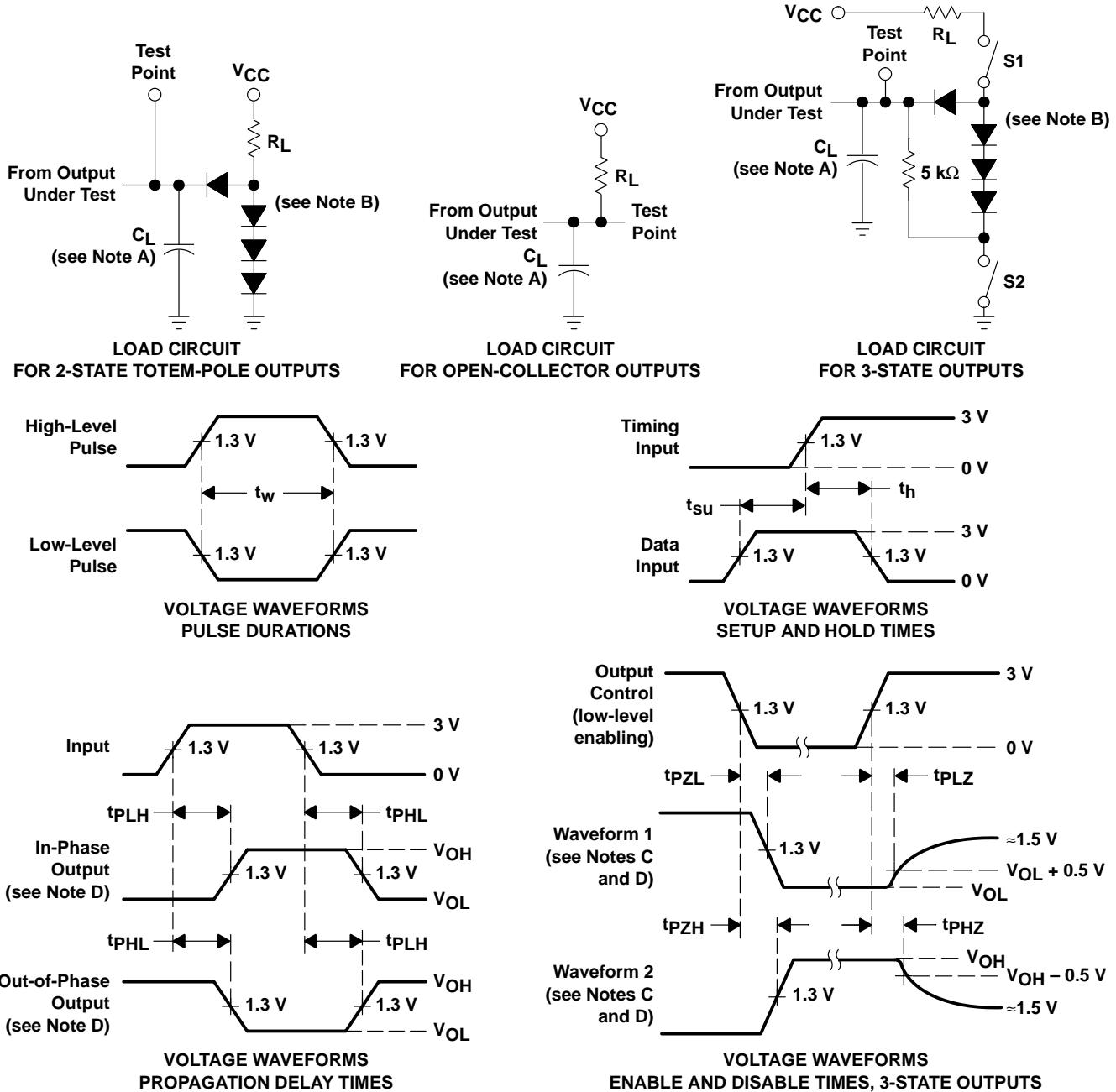
‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 1)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω		8	12	ns
t <sub>PHL</sub>			8	12	
t <sub>PZL</sub>	Output enable time to low level C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω		27	40	ns
t <sub>PZH</sub>			25	40	
t <sub>PLZ</sub>	Output disable time from low level C <sub>L</sub> = 5 pF, R <sub>L</sub> = 667 Ω		15	25	ns
t <sub>PHZ</sub>			15	28	

PARAMETER MEASUREMENT INFORMATION  
SERIES 54LS/74LS DEVICES



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - All diodes are 1N3064 or equivalent.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PZL}$ .
  - Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O \approx 50 \Omega$ ,  $t_r \leq 1.5 \text{ ns}$ ,  $t_f \leq 2.6 \text{ ns}$ .
  - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-8002101VRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
5962-8002101VSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
80021012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
8002101SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32803B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32803BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32803BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SN54LS245J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN74LS245DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS245DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS245DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS245DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS245DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS245DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS245J	OBsolete	CDIP	J	20		TBD	Call TI	Call TI
SN74LS245N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS245N3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI
SN74LS245NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS245NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS245NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS245NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54LS245FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS245J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS245W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

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at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(<sup>3</sup>) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

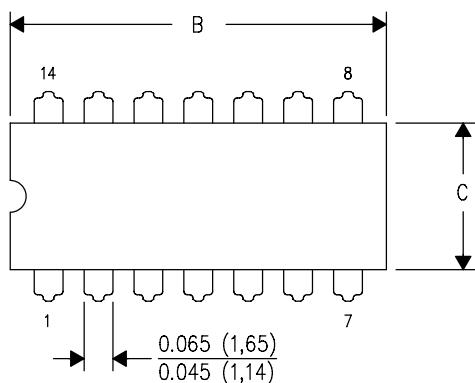
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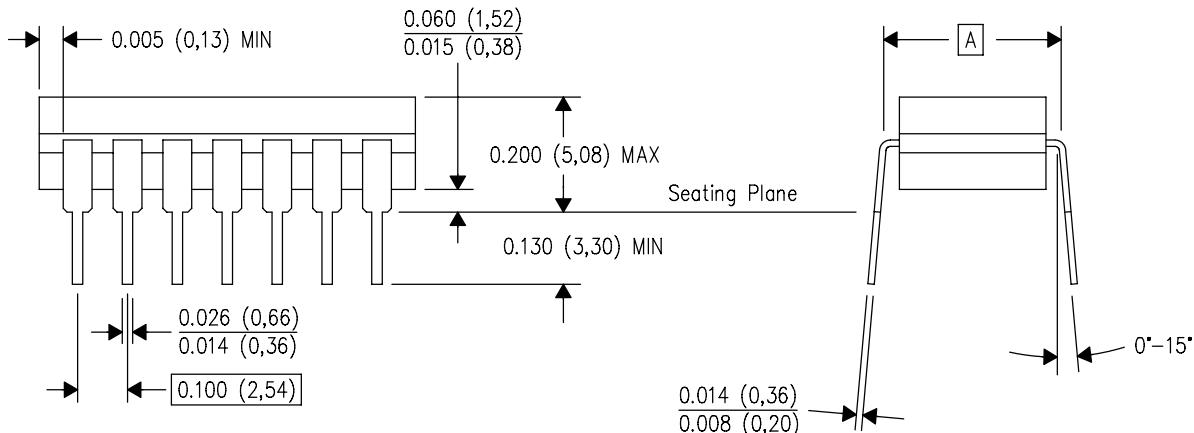
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **\nDIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

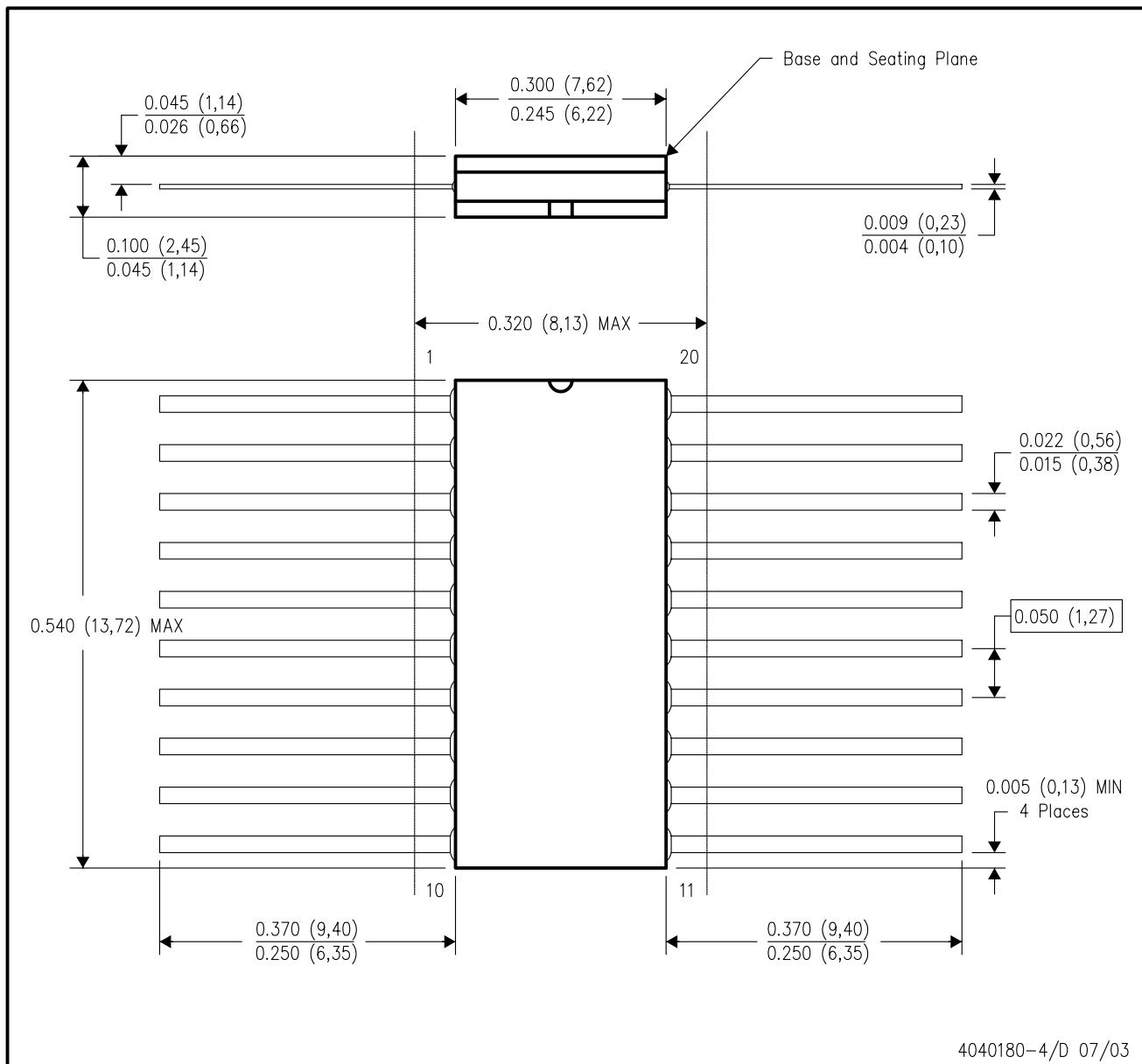


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



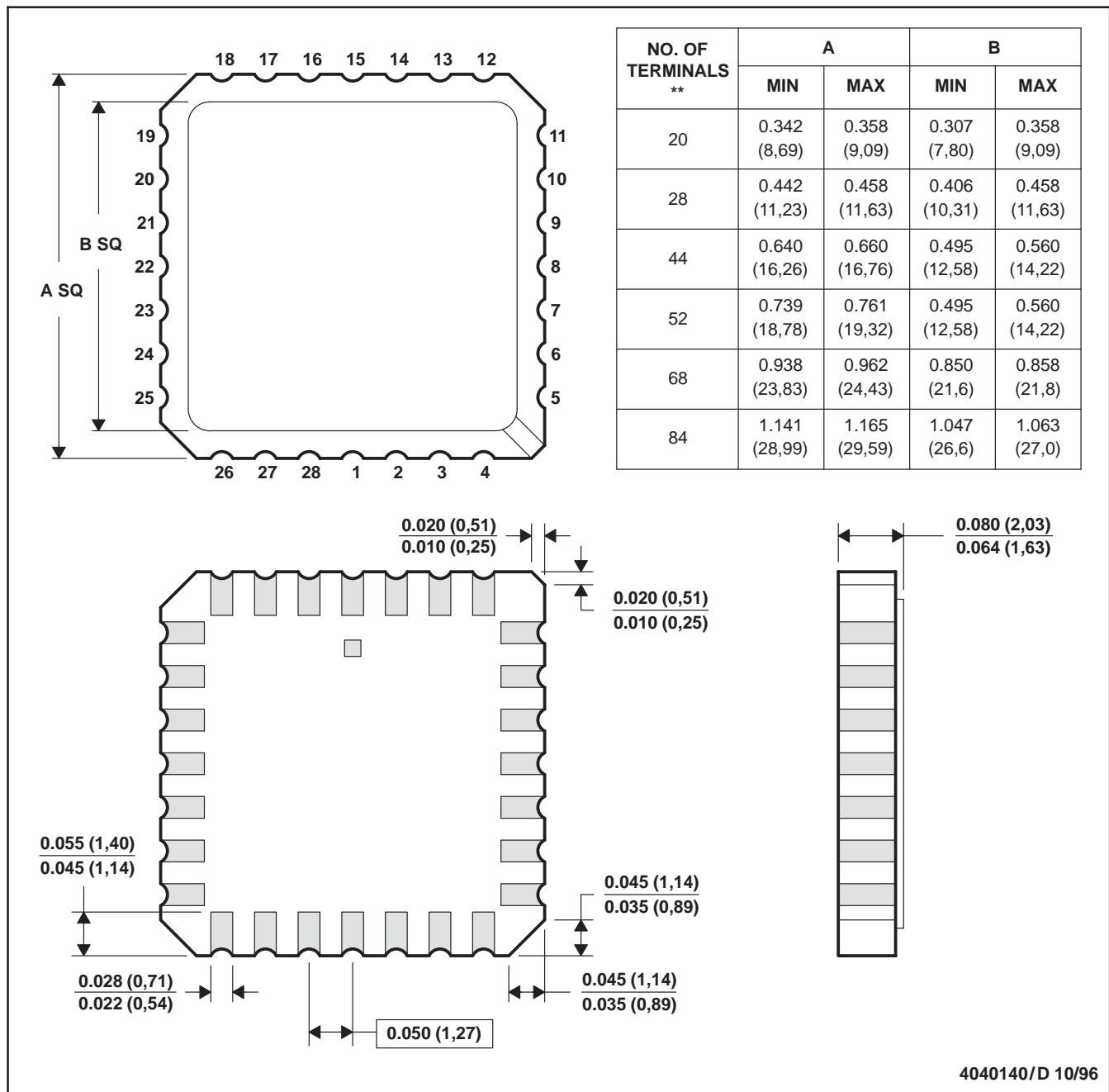
4040180-4/D 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

D. The terminals are gold plated.

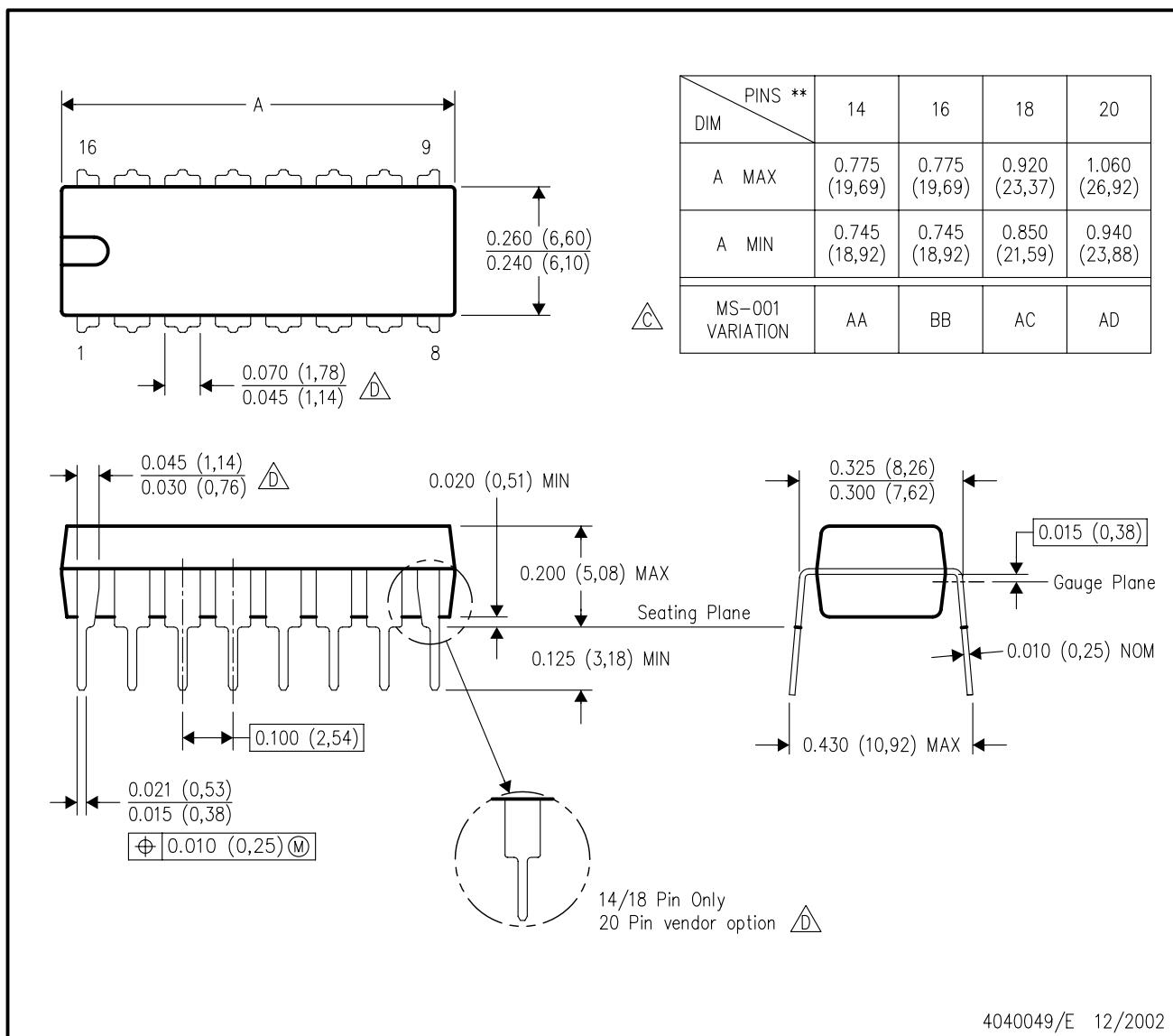
E. Falls within JEDEC MS-004

4040140/D 10/96

## N (R-PDIP-T\*\*)

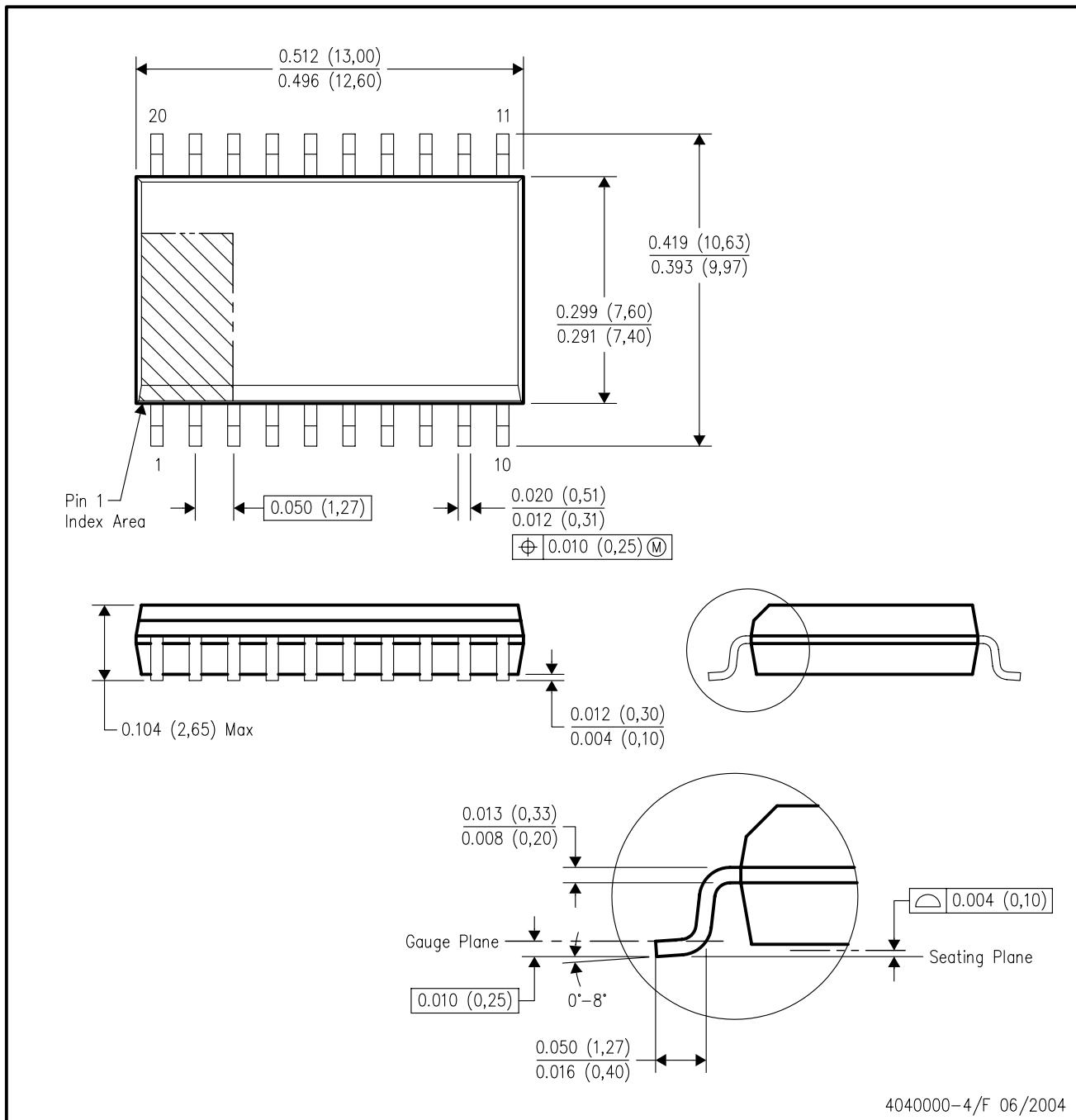
16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



## DW (R-PDSO-G20)

## PLASTIC SMALL-OUTLINE PACKAGE



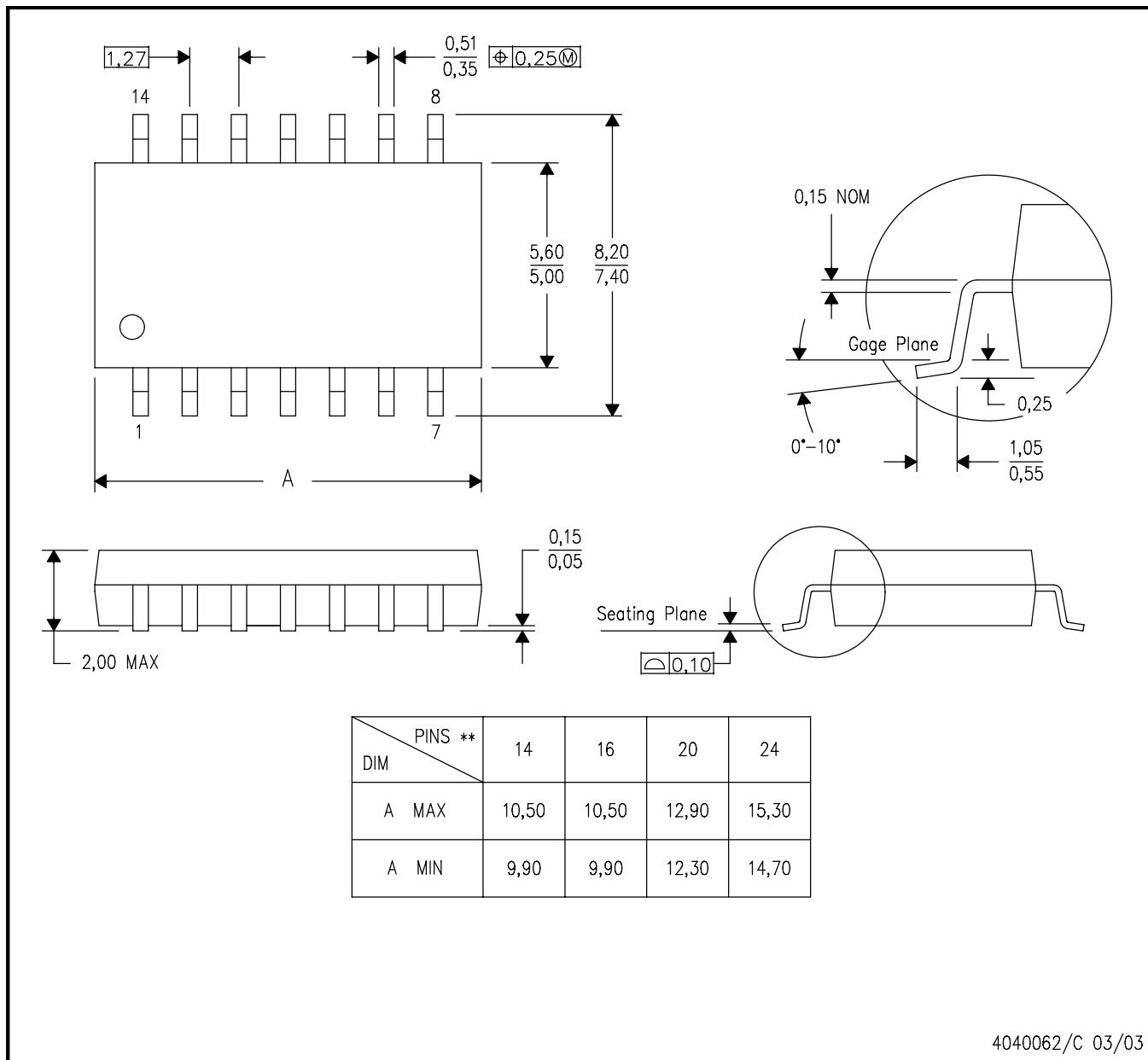
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**

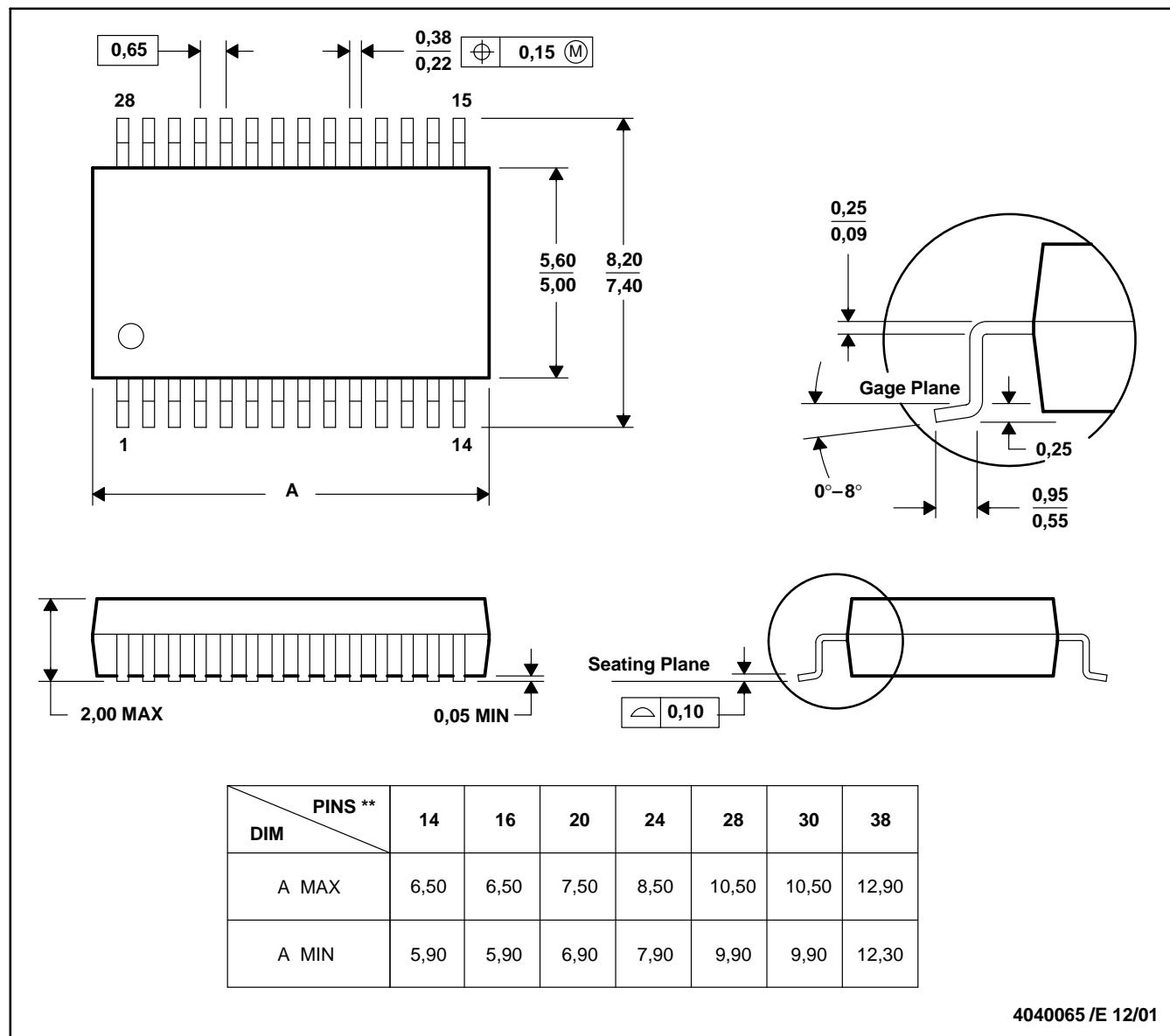


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. Falls within JEDEC MO-150

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View ROHS Compliant Devices clear gif**SN74LS245, Status: ACTIVE**

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 clear gif Features Quality & Pb-Free Data Related Products Tools & Software Samples Pricing/Packaging Inventory Symbols/Footprints Technical Documents Applications Notes Simulation Models Reference Designs**Refine Your Selection**

- Logic: Standard Transceivers

**Support**

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**Datasheet****Octal Bus Transceivers With 3-State Outputs (Rev. A) (sn74ls245.pdf, 513 KB)**01 Nov 2001 [Download](#)

	<b>SN54LS245</b>	<b>SN74LS245</b>
<b>Voltage Nodes(V)</b>	5	5
<b>Vcc range(V)</b>	4.5 to 5.5	4.75 to 5.25
<b>Input Level</b>	TTL	TTL
<b>Output Level</b>	TTL	TTL
<b>Output Drive(mA)</b>		-15/24
<b>No. of Outputs</b>	8	8
<b>Logic</b>	True	True
<b>Static Current</b>		80
<b>tpd max(ns)</b>		12
	<a href="#">Samples</a>	<a href="#">Samples</a>
	<a href="#">Inventory</a>	<a href="#">Inventory</a>

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3-State Outputs Drive Bus Lines Directly  
 PNP Inputs Reduce dc Loading on Bus Lines  
 Hysteresis at Bus Inputs Improves Noise Margins  
 Typical Propagation Delay Times Port to Port, 8 ns

 **Description**

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE)\ input can disable the device so that the buses are effectively isolated.

### Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging			CAD Design Tools		Samples
Device	Status	Temp (°C)	Budget Price (\$US)   QTY	Industry Standard (TI Pkg)   Pins	Top Side Marking	Standard Pack Quantity	Footprints		Samples
SN74LS245DBR	ACTIVE	0 to 70	0.44   1KU	SSOP (DB)   20	View	2000	<input type="checkbox"/>		Purchase Samples
SN74LS245DBRE4	ACTIVE	0 to 70	0.44   1KU	SSOP (DB)   20	View	2000	<input type="checkbox"/>		Purchase Samples
SN74LS245DW	ACTIVE	0 to 70	0.44   1KU	SOIC (DW)   20	View	25	<input type="checkbox"/>		Purchase Samples
SN74LS245DWG4	ACTIVE	0 to 70	0.48   1KU	SOIC (DW)   20	View	25	<input type="checkbox"/>		Purchase Samples
SN74LS245DWR	ACTIVE	0 to 70	0.44   1KU	SOIC (DW)   20	View	2000	<input type="checkbox"/>		Purchase Samples
SN74LS245DWRG4	ACTIVE	0 to 70	0.48   1KU	SOIC (DW)   20	View	2000	<input type="checkbox"/>		Purchase Samples
SN74LS245J	OBsolete	0 to 70		CDIP (J)   20			<input type="checkbox"/>		Not Available
SN74LS245N	ACTIVE	0 to 70	0.44   1KU	PDIP (N)   20	View	20	<input type="checkbox"/>		Purchase Samples
SN74LS245N3	OBsolete	0 to 70		PDIP (N)   20	View		<input type="checkbox"/>		Not Available
SN74LS245NE4	ACTIVE	0 to 70	0.44   1KU	PDIP (N)   20	View	20	<input type="checkbox"/>		Request Free Samples
SN74LS245NSR	ACTIVE	0 to 70	0.44   1KU	SO (NS)   20	View	2000	<input type="checkbox"/>		Purchase Samples
SN74LS245NSRE4	ACTIVE	0 to 70	0.44   1KU	SO (NS)   20	View	2000	<input type="checkbox"/>		Purchase Samples
SN74LS245NSRG4	ACTIVE	0 to 70	0.48   1KU	SO (NS)   20	View	2000	<input type="checkbox"/>		Purchase Samples

### Inventory

			Reported Distributor Inventory				
			As of 9:10 AM GMT, 29 Nov 2005				
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase
SN74LS245DBR	0*	3442   20 Dec	10 Weeks	None Reported <a href="#">View Distributors</a>			
		>10k   27 Dec					
SN74LS245DBRE4	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase
SN74LS245DW	0*	3442   20 Dec	10 Weeks	None Reported <a href="#">View Distributors</a>			
		>10k   27 Dec					
SN74LS245DWG4	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase
SN74LS245DWG4	0*	>10k   30 Jan	9 Weeks	Americas	Avnet	900	<input type="text"/>
					DigiKey	83	<input type="text"/>
					Newark InOne	712	<input type="text"/>
					Abacus Polar	3	<input type="text"/>
				Europe	Avnet-SILICA	>1k	<input type="text"/>
					EBV Elektronik	>1k	<input type="text"/>
					Rutronik	100	<input type="text"/>

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[Choose a Region](#)



<b>SN74LS245DWR</b>	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k   30 Jan	9 Weeks	Americas	DigiKey	>1k	
				Europe	Abacus Polar	>1k	
					Arrow Southern Europe	>1k	
					EBV Elektronik	1k	
<b>SN74LS245DWRG4</b>	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase
	0*	1   30 Nov	9 Weeks	None Reported <a href="#">View Distributors</a>			
		>10k   27 Jan					
<b>SN74LS245N</b>	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase
	0*	1000   7 Dec	10 Weeks	Americas	Avnet	>1k	
		9420   28 Dec			DigiKey	>1k	
					Newark InOne	>1k	
				Europe	Arrow Northern Europe	>1k	
					Avnet-SILICA	>1k	
					EBV Elektronik	>1k	
<b>SN74LS245NE4</b>	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase
	0*	1000   7 Dec	10 Weeks	None Reported <a href="#">View Distributors</a>			
		9420   28 Dec					
<b>SN74LS245NSR</b>	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase
	0*	4665   16 Dec	4 Weeks	None Reported <a href="#">View Distributors</a>			
		>10k   30 Dec					
<b>SN74LS245NSRE4</b>	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase
	0*	4673   16 Dec	8 Weeks	None Reported <a href="#">View Distributors</a>			
		>10k   30 Dec					
<b>SN74LS245NSRG4</b>	As of 9:10 AM GMT, 29 Nov 2005			As of 9:10 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY   Date	Lead Time	Region	Company	In Stock	Purchase
	0*	4704   19 Dec	8 Weeks	None Reported <a href="#">View Distributors</a>			
		>10k   3 Jan					

\* Our information is updated daily, so please check back with us soon if this does not meet your needs. You may also contact your [TI Authorized Distributor](#), including those [listed above](#), for real time stock information.

\*\* Lead time information is not available at this time. However, our information is updated daily so please check back with us soon. Please contact your preferred [TI Authorized Distributor](#) for additional information.

## Quality & Lead (Pb)-Free Data

	Product Content				MTBF/FIT Rate
Device	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details
SN74LS245DBR <input checked="" type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>
SN74LS245DBRE4 <input checked="" type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>
SN74LS245DW <input checked="" type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>
SN74LS245DWG4 <input checked="" type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>
SN74LS245DWR <input checked="" type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>
SN74LS245DWRG4 <input checked="" type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>
SN74LS245N <input checked="" type="checkbox"/>	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	<a href="#">View</a>	<a href="#">View</a>
SN74LS245NE4 <input checked="" type="checkbox"/>	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	<a href="#">View</a>	<a href="#">View</a>
SN74LS245NSR <input checked="" type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>
SN74LS245NSRE4 <input checked="" type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>
SN74LS245NSRG4 <input checked="" type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">View</a>	<a href="#">View</a>

\* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our [Product Information Centers](#) regarding the availability of this information.

## Technical Documents

### Datasheets

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**Octal Bus Transceivers With 3-State Outputs (Rev. A)** ([sn74ls245.pdf](#), 513 KB)

01 Nov 2001 [Download](#)

### Application Notes

**Semiconductor Packing Material Electrostatic Discharge (ESD) Protection** ([szza047.htm](#), 9 KB)

08 Jul 2004 [Abstract](#)

**Shelf-Life Evaluation of Lead-Free Component Finishes** ([szza046.htm](#), 9 KB)

24 May 2004 [Abstract](#)

**Understanding and Interpreting Standard-Logic Data Sheets (Rev. B)** ([szza036b.htm](#), 8 KB)

28 May 2003 [Abstract](#)

**TI IBIS File Creation, Validation, and Distribution Processes** ([szza034.htm](#), 9 KB)

29 Aug 2002 [Abstract](#)

**Designing With Logic (Rev. C)** ([sdya009c.htm](#), 9 KB)

01 Jun 1997 [Abstract](#)

**Designing with the SN54/74LS123 (Rev. A)** ([sdla006a.htm](#), 9 KB)

01 Mar 1997 [Abstract](#)

**Live Insertion** ([sdya012.htm](#), 9 KB)

01 Oct 1996 [Abstract](#)

**Input and Output Characteristics of Digital Integrated Circuits** ([sdya010.htm](#), 9 KB)

01 Oct 1996 [Abstract](#)

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### User Guides

**LOGIC Pocket Data Book** ([scyd013.pdf](#), 4835 KB)

05 Dec 2002 [Download](#)

### Simulation Models

#### IBIS Model

**IBIS Model of SN74LS245 (Rev. B)** ([sdlm009b.ibs](#), 41 KB)

22 Nov 2004 [ibis / zip](#)

### More Literature

**Logic Selection Guide 2005 (Rev. X)** ([sdyu001x.pdf](#), 6909 KB)

15 Mar 2005 [Download](#)

**Military Semiconductors Selection Guide 2004-2005 (Rev. D)** ([sgyc003d.pdf](#), 964 KB)

10 Aug 2004 [Download](#)

**Logic Cross-Reference (Rev. A)** ([scyb017a.pdf](#), 2938 KB)

07 Oct 2003 [Download](#)

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