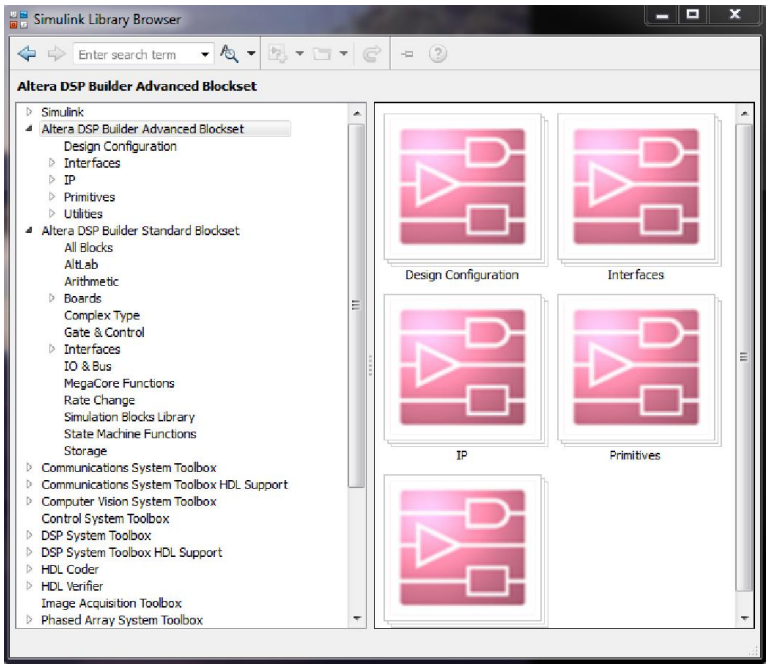
DSP Builder for Intel FPGAs

Auto-generate HDL for Intel FPGAs in a Model-Based Design Workflow

Highlights

- Target Intel FPGAs without hardware design experience
- High-quality automatic code generation, implementation, and verification
- Auto-generate SystemVerilog or VHDL from Simulink models
- Single environment to design algorithm and set desired data rate, clock frequency, and target device
- Address last minute design specification changes in minutes
- Shorten DSP design cycles
- Flexible “white-box” Fast Fourier transform (FFT) toolkit allows users to build custom FFTs
- Includes a library of optimized Intel FPGA hardware and DSP building blocks for Simulink

Description



DSP Builder for Intel® FPGAs is a high-level design tool that allows engineers to accomplish high performance DSP systems using Model-Based Design. DSP Builder integrates Simulink® with Intel Quartus Prime design software, creating a workflow for configuring Intel

FPGAs. DSP Builder includes both a hardware-optimized Standard Blockset and Advanced Blockset for use within the Simulink Library Browser.

DSP Builder Advanced Blockset is a constraint-driven, behavioral Model-Based Design environment, offering significant advantages in terms of design management and productivity for designing complex signal processing systems. Some of the key features of DSP Builder Advanced Blockset include:

- Constraint-driven design
- Automated resource sharing
- Automated pipelining
- Supports scaler, vector, and complex abstract data types
- Model silicon speeds while translating to HDL
- Support high-performance floating-point designs

Additional resources are available:

- Learn how to target Intel FPGAs Using MathWorks HDL Coder
- Learn how to use DSP Builder Advanced Blockset with HDL Coder

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