

M74ALS163BP

T-45-23-05

PRELIMINARY
 Notice: This is not a final specification.
 Some parameters limits are subject to change.

FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

6249827 MITSUBISHI (DGTL LOGIC)

91D 12422 D

DESCRIPTION

The M74ALS163BP is a semiconductor integrated circuit of a synchronous presettable 4-bit binary (hexadecimal) counter with a synchronous reset input.

FEATURES

- Synchronous reset and load inputs
- Enable inputs and carry output for cascade connection
- Wide operating temperature range ($T_a = -20 \sim +75^\circ\text{C}$)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

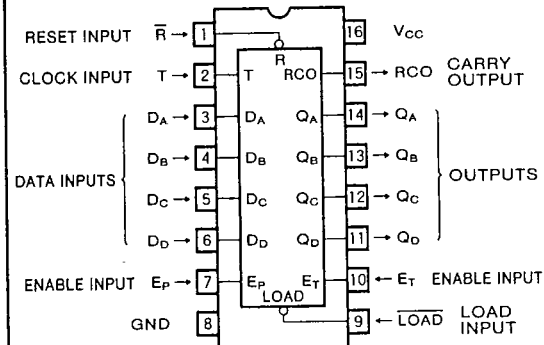
When the count pulse is applied to clock input T, the number of count pulse appears in 4-bit binary code on $Q_A \sim Q_D$ synchronized with the count pulse. Counting occurs as T changes from low-level to high-level.

Preset is synchronized with the count pulse. Irrespective of the enable inputs E_P and E_T , $D_A \sim D_D$ signals appear on $Q_A \sim Q_D$ when load input LOAD is set low and T changes from low to high.

When reset R is set low and T changes from low to high, reset occurs synchronously and $Q_A \sim Q_D$ become low.

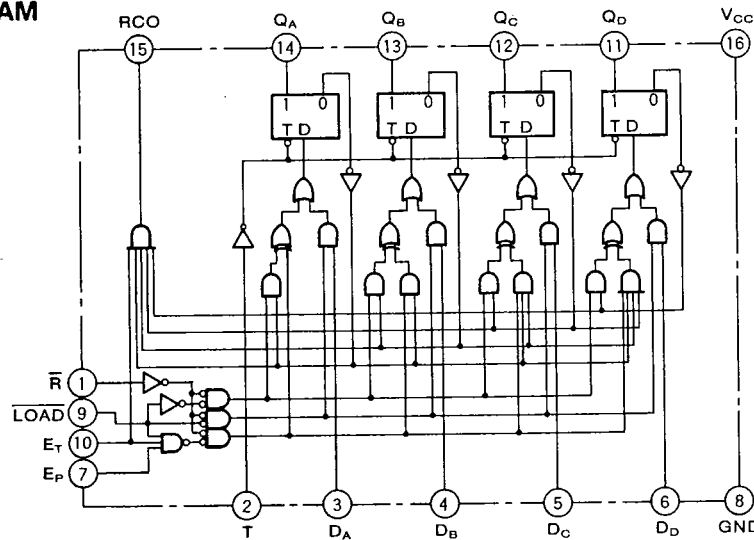
Carry output RCO becomes high only when $Q_A \sim Q_D$ and E_T are high, E_P , E_T and RCO are used when counters are connected in synchronous cascade connection and made an n-bit counter.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

LOGIC DIAGRAM



FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

FUNCTION TABLE (Note 1)

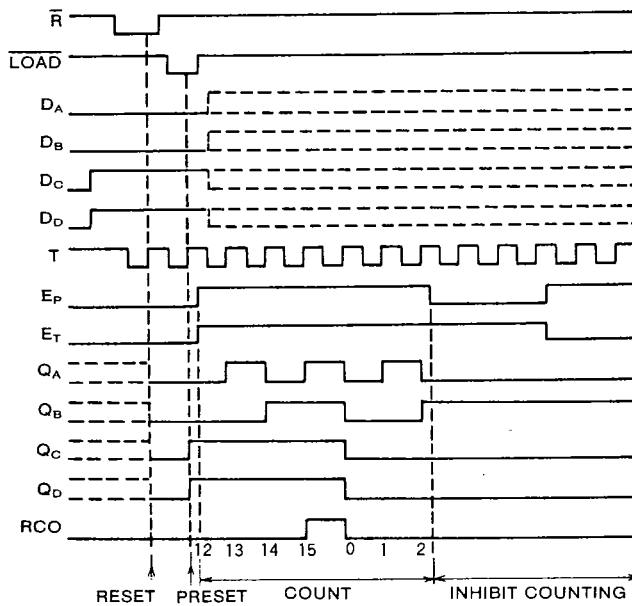
Inputs					Outputs				
\bar{R}	LOAD	E_T	E_P	T	Q_A	Q_B	Q_C	Q_D	RCO
L	X	X	X	↑	L	L	L	L	L
H	L	L	X	↑	D_A	D_B	D_C	D_D	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Inhibit counting				L
H	H	H	L	X	Inhibit counting				L*

Note 1. ↑ : Transition from low to high (positive edge trigger)

* : RCO, usually low, becomes high when Q_A , Q_D and E_T are high, i.e., $RCO=Q_A \cdot Q_D \cdot E_T$.

X : Irrelevant

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.5~+7	V
V_i	Input voltage		-0.5~+7	V
V_o	Output voltage	High-level state	-0.5~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		-20~+75	°C
T_{stg}	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		-0.4	mA
I_{OL}	Low-level output current	0		8	mA
T_{opr}	Operating free-air ambient temperature range	-20		+75	°C

FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

ELECTRICAL CHARACTERISTICS (T_a = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ*	Max		
V _{IC}	Input clamp voltage	V _{CC} =4.5V, I _{IC} =-18mA			-1.2	V	
V _{OH}	High-level output voltage	V _{CC} =4.5~5.5V, I _{OH} =-0.4mA	V _{CC} -2			V	
V _{OL}	Low-level output voltage	V _{CC} =4.5V		I _{OL} =4mA	0.25	0.4	V
				I _{OL} =8mA	0.35	0.5	
I _I	Input current at maximum voltage	V _{CC} =5.5V, V _I =7V			0.1	mA	
I _{IH}	High-level input current	V _{CC} =5.5V, V _I =2.7V			20	μA	
I _{IL}	Low-level input current	V _{CC} =5.5V, V _I =0.4V			-0.2	mA	
I _O	Output current	V _{CC} =5.5V, V _O =2.25V	-30		-112	mA	
I _{CC}	Supply current	V _{CC} =5.5V		12	21	mA	

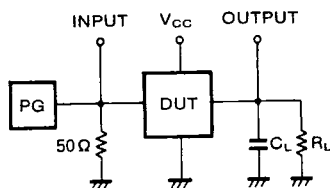
*: All typical values are at V_{CC}=5V, T_a=25°C.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Test conditions/Limits (Note 2)									Unit		
				V _{CC} =5V			V _{CC} =4.5~5.5V			T _a =-20~+75°C			
				C _L =15pF			C _L =50pF						
				R _L =500Ω			R _L =500Ω						
		T _a =25°C			T _a =0~70°C								
		Inputs	Outputs	Typ	Min	Typ*	Max	Min	Typ*	Max			
f _{max}	Maximum clock frequency	T	Q _A ~Q _D		40			37			MHz		
t _{PLH}	Propagation time	T	RCO		5		20	5		21	ns		
t _{PHL}					5		20	5		21			
t _{PLH}		T	Q _A ~Q _D		4		15	4		16	ns		
t _{PHL}					6		20	6		21			
t _{PLH}		E _T	RCO		3		13	3		14	ns		
t _{PHL}					3		13	3		14			

*: All typical values are at V_{CC}=5V, T_a=25°C.

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:

- PRR ≤ 1MHz
- t_r = 2ns, t_f = 2ns
- V_{IH} = 3.5V, V_{IL} = 0.3V
- duty cycle = 50%
- Z_O = 50Ω

(2) C_L includes probe and jig capacitance.

M74ALS163BP

91D 12425 DT-45-23-05

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FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

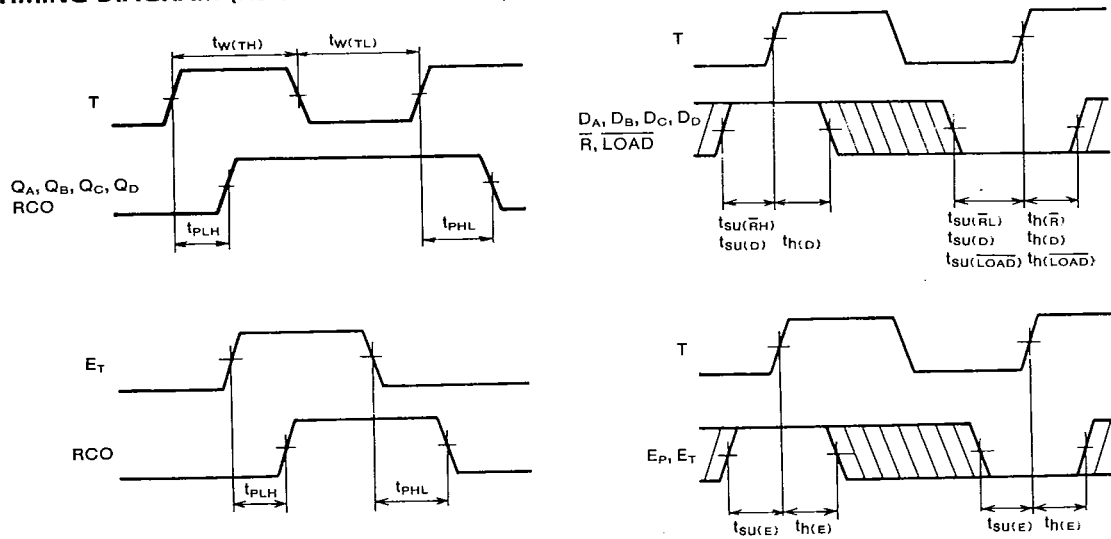
TIMING REQUIREMENTS ($V_{CC}=4.5V\sim 5.5V$, $C_L=50pF$, $R_L=500\Omega$)

Symbol	Parameter	Limits						Unit	
		$T_a=0\sim 70^\circ C$			$T_a=-20\sim +75^\circ C$				
		Min	Typ*	Max	Min	Typ*	Max		
$t_{w(TH)}$	Pulse width	T "H"	12.5			13.5			ns
$t_{w(TL)}$		T "L"	12.5			13.5			
$t_{su(D)}$	Setup time before T \uparrow	$D_A\sim D_D$	15			16		ns	
$t_{su(LOAD)}$		LOAD "L"	15			16			
$t_{su(RL)}$		\bar{R} "L"	15			16			
$t_{su(RH)}$		R_D "H" (inactive)	10			11			
$t_{su(E)}$		E_P, E_T	15			16			
$t_h(D)$	Hold time after T \uparrow	$D_A\sim D_D$	0			1		ns	
$t_h(LOAD)$		LOAD "L"	0			1			
$t_h(\bar{R})$		\bar{R} "L"	0			1			
$t_h(E)$		E_P, E_T	0			1			

*: All typical values are at $V_{CC}=5V$, $T_a=25^\circ C$.

\uparrow : Transition from low to high

TIMING DIAGRAM (Reference level=1.3V)



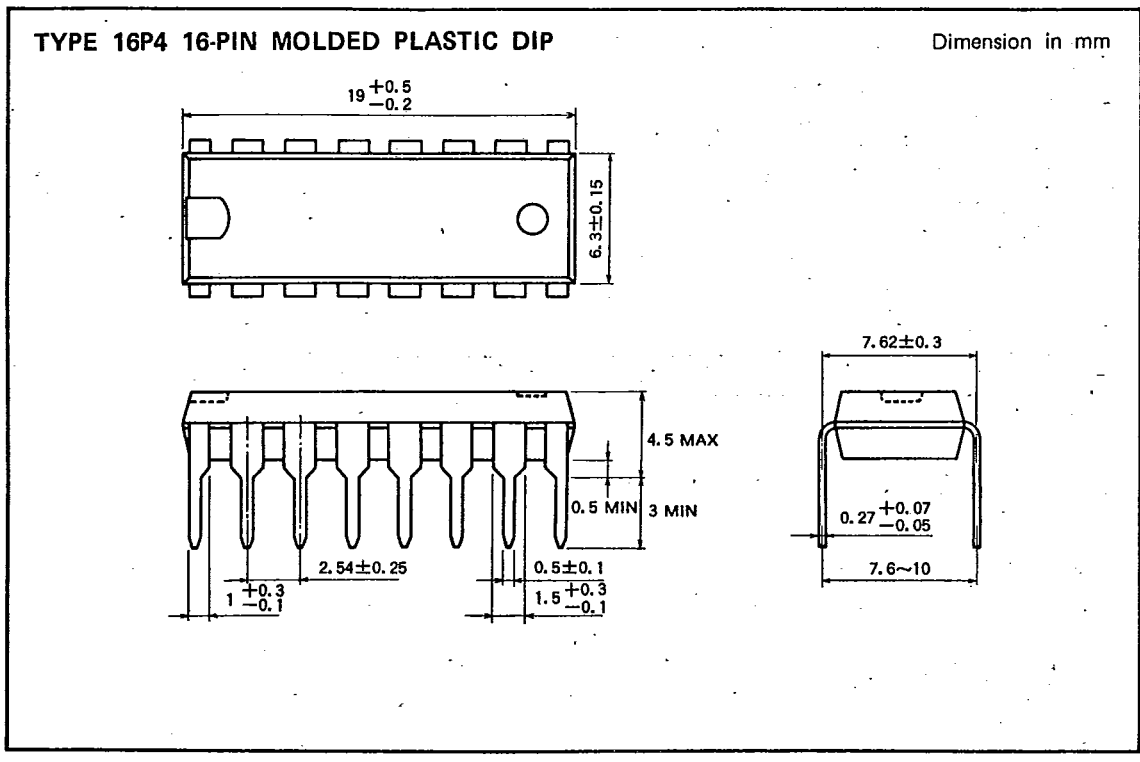
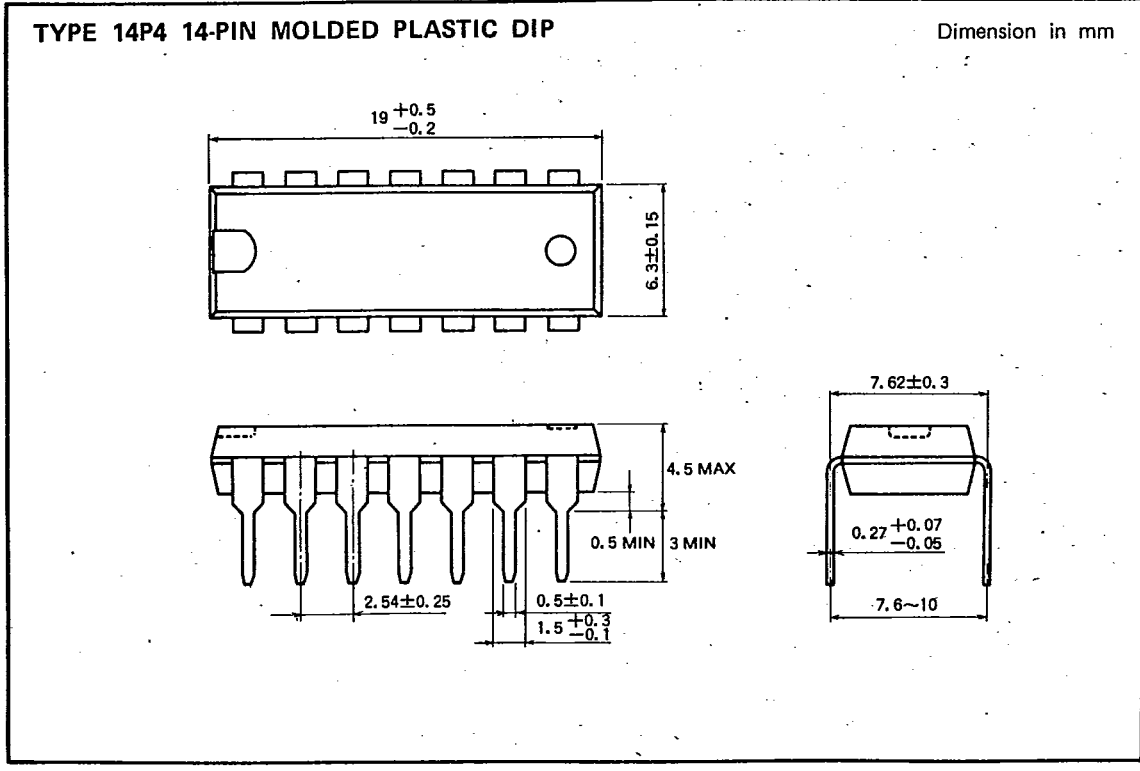
Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

PACKAGE OUTLINES

MITSUBISHI {DGTL LOGIC}

91D 12323

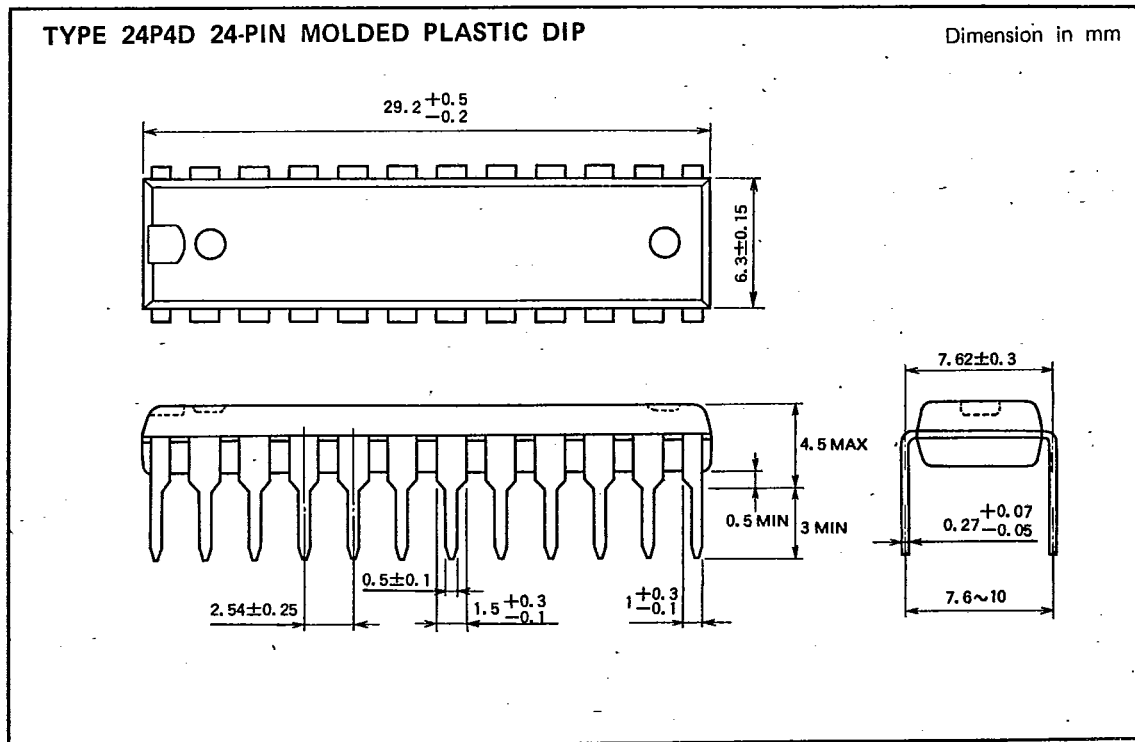
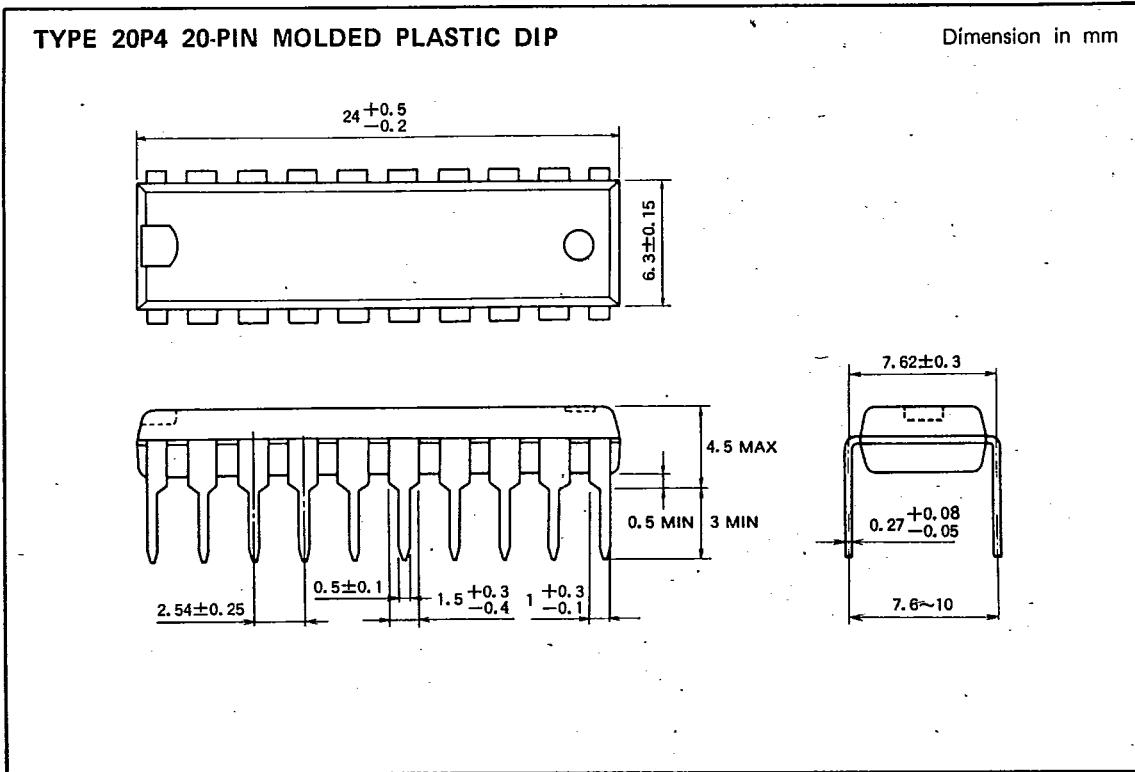
D T-9020



PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)

91D 12324 D T-90-20



TYPE DESIGNATION TABLE

MITSUBISHI (DGTL LOGIC)

91D D ■ 6249827 0012784 7 ■ MIT3

T-90-20

ALSTTL SERIES SOP TYPE DESIGNATION TABLE

Type		Circuit function	Package Outlines
M74ALS00ADP	*	Quadruple 2-Input Positive NAND Gate	14P2P
M74ALS02DP	*	Quadruple 2-Input Positive NOR Gate	14P2P
M74ALS04ADP	*	Hex Inverter	14P2P
M74ALS05ADP	**	Hex Inverter with Open Collector Output	14P2P
M74ALS08DP	*	Quadruple 2-Input Positive AND Gate	14P2P
M74ALS09DP	**	Quadruple 2-Input Positive AND Gate with Open Collector Output	14P2P
M74ALS10ADP	*	Triple 3-Input Positive NAND Gate	14P2P
M74ALS11ADP	*	Triple 3-Input Positive AND Gate	14P2P
M74ALS20ADP	**	Dual 4-Input Positive NAND Gate	14P2P
M74ALS27DP	**	Triple 3-Input Positive NOR Gate	14P2P
M74ALS30ADP	**	Single 8-Input Positive NAND Gate	14P2P
M74ALS32DP	*	Quadruple 2-Input Positive OR Gate	14P2P
M74ALS37ADP	**	Quadruple 2-Input Positive NAND Buffer	14P2P
M74ALS38ADP	**	Quadruple 2-Input Positive NAND Buffer with Open Collector Output	14P2P
M74ALS74ADP	*	Dual D-Type Positive Edge-Triggered Flip-Flop with Set and Reset	14P2P
M74ALS109ADP	**	Dual J-K Positive Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS112ADP	*	Dual J-K Negative Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS131DP	**	3-Line to 8-Line Decoder/Demultiplexer with Address Register	16P2P
M74ALS138DP	*	3-Line to 8-Line Decoder/Demultiplexer	16P2P
M74ALS153DP	**	Dual 4-Line to 1-Line Data Selector/Multiplexer with Strobe	16P2P
M74ALS157DP	*	Quadruple 2-Line to 1-Line Data Selector/Multiplexer	16P2P
M74ALS161BDP	**	Synchronous Presettable 4-Bit Binary Counter with Direct Reset	16P2P
M74ALS163BDP	**	Fully Synchronous Presettable 4-Bit Binary Counter	16P2P
M74ALS169BDP	**	Synchronous 4-Bit Binary Counter	16P2P
M74ALS174DP	*	Hex D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS175DP	**	Quadruple D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS193DP	**	Synchronous Presettable Up/Down 4-Bit Binary Counter	16P2P
M74ALS240ADWP	*	Octal Buffer/Line Driver with 3-State Output (Inverted)	20P2V
M74ALS244ADWP	*	Octal Buffer/Line Driver with 3-State Output (Noninverted)	20P2V
M74ALS245ADWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS245A-1DWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS257DP	*	Quadruple 2-Line to 1-Line Data Selector/Multiplexer with 3-State Output	16P2P
M74ALS273DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with Reset	20P2V
M74ALS299DWP	**	8-Bit Universal Shift/Storage Register with 3-State Output	20P2V
M74ALS373DWP	**	Octal D-Type Transparent Latch with 3-State Output	20P2V
M74ALS374DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output	20P2V
M74ALS533DWP	**	Octal D-Type Transparent Latch with 3-State Output (Inverted)	20P2V
M74ALS534DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Inverted)	20P2V
M74ALS561ADWP	**	Synchronous Presettable 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS569ADWP	**	Synchronous Up/Down 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS573ADWP	**	Octal D-Type Transparent Latch with 3-State Output (Noninverted)	20P2V
M74ALS574ADWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Noninverted)	20P2V
M74ALS640ADWP	**	Octal Bus Transceiver with 3-State Output (Inverted)	20P2V
M74ALS642ADWP	**	Octal Bus Transceiver with Open Collector Output (Inverted)	20P2V
M74ALS645ADWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS1034DP	**	Hex Noninverting Buffer	14P2P

*: New product **: Under development

6249827 MITSUBISHI (DGTL LOGIC)

91D 12785 D

MITSUBISHI ALSTTLs

DESCRIPTION

MITSUBISHI (DGTL LOGIC) 91D D ■ 6249827 0012785 9 ■ MIT3

T-90-20

DESCRIPTION

The ALSTTL SOP (Small Outline Package) devices are identical in all respects except for their package outlines to DIP (Dual Inline Package).

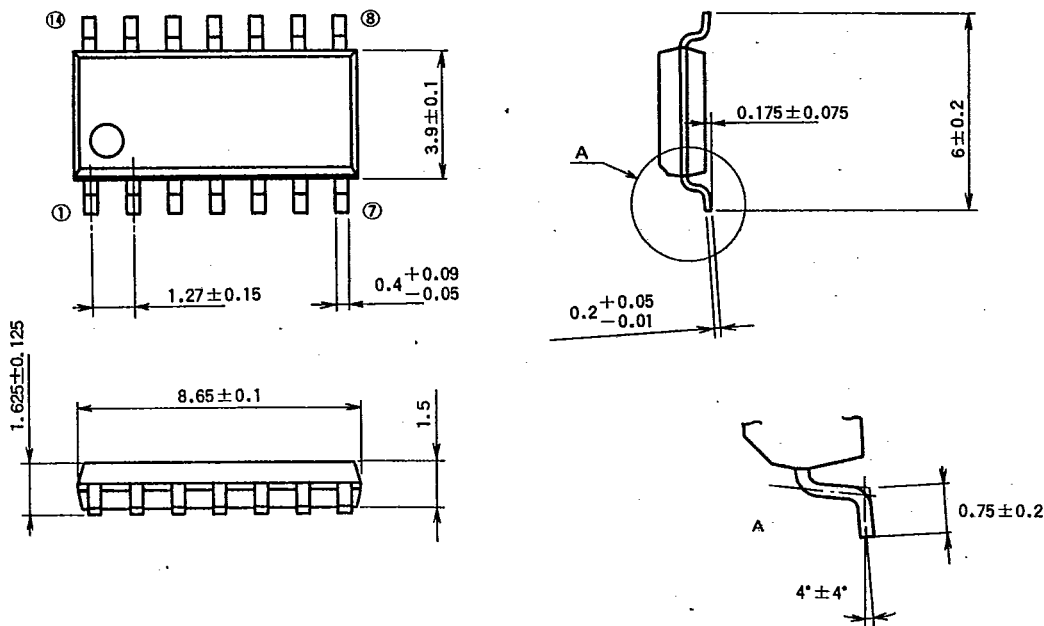
MITSUBISHI ALSTTLs
PACKAGE OUTLINES

MITSUBISHI (DGTL LOGIC) 91D D ■ 6249827 0012786 0 ■ MIT3

T-90-20

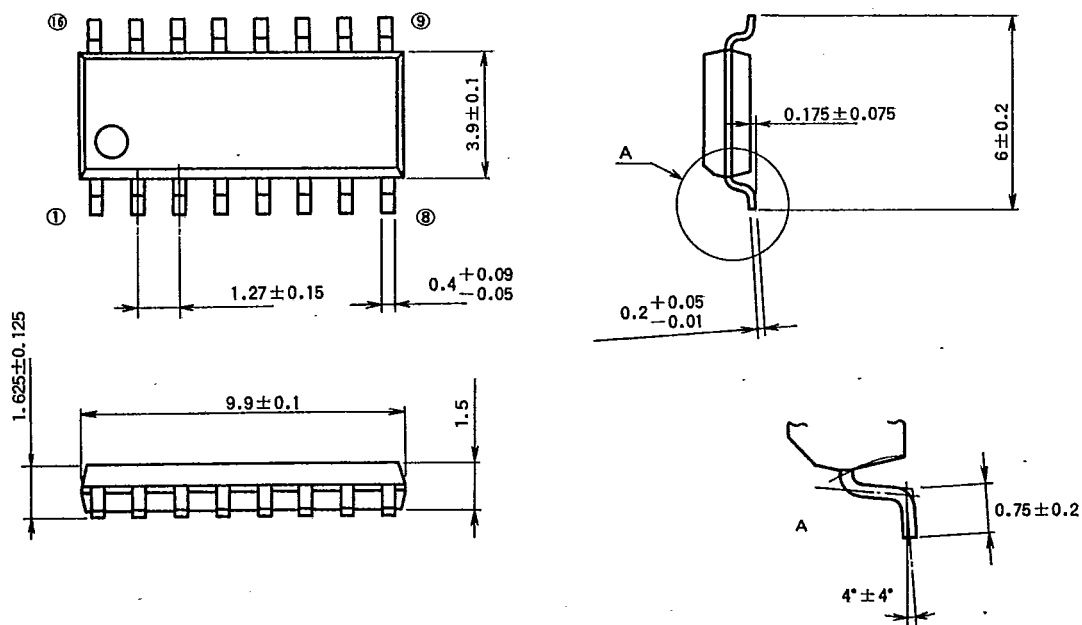
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Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

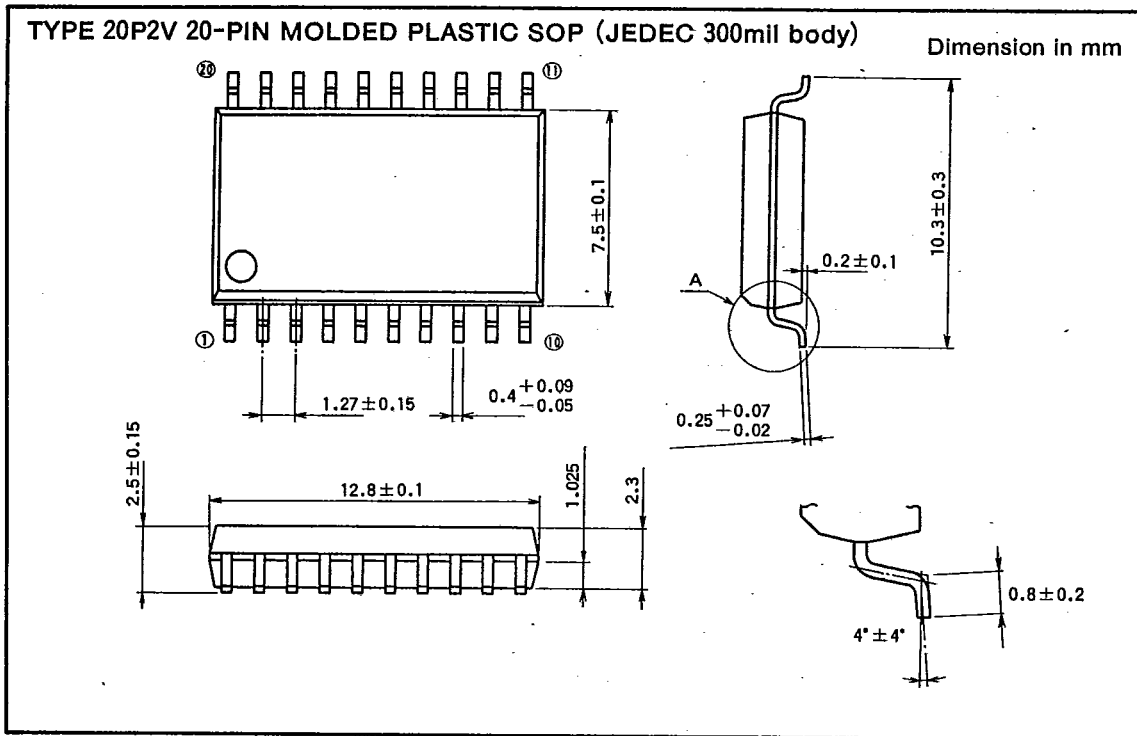
Dimension in mm



MITSUBISHI ALSTTLs
PACKAGE OUTLINES

MITSUBISHI (DGTL LOGIC) 9LD D ■ 6249827 0012787 2 ■ MIT3

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