

# Precision, Rail-to-Rail Input and Output, Zero-Drift Instrumentation Amplifier with Resistor-Programmable Gain

## FEATURES

- 116dB CMRR Independent of Gain
- Maximum Offset Voltage: 10 $\mu$ V
- Maximum Offset Voltage Drift: 50nV/ $^{\circ}$ C
- Rail-to-Rail Input
- Rail-to-Rail Output
- 2-Resistor Programmable Gain
- Supply Operation: 2.7V to  $\pm$ 5.5V
- Typical Noise: 2.5 $\mu$ V<sub>P-P</sub> (0.01Hz to 10Hz)
- Typical Supply Current: 750 $\mu$ A
- Available in an MS8 and 3mm  $\times$  3mm  $\times$  0.8mm DFN Packages

## APPLICATIONS

- Thermocouple Amplifiers
- Electronic Scales
- Medical Instrumentation
- Strain Gauge Amplifiers
- High Resolution Data Acquisition

## DESCRIPTION

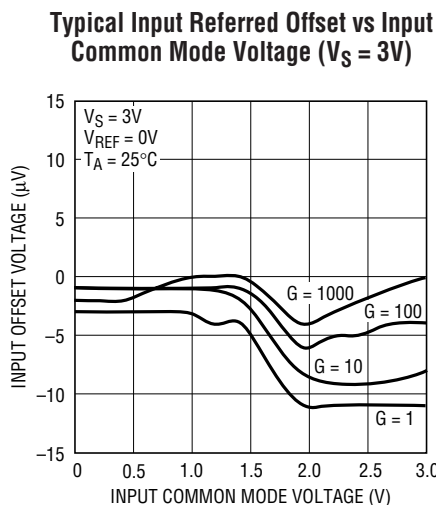
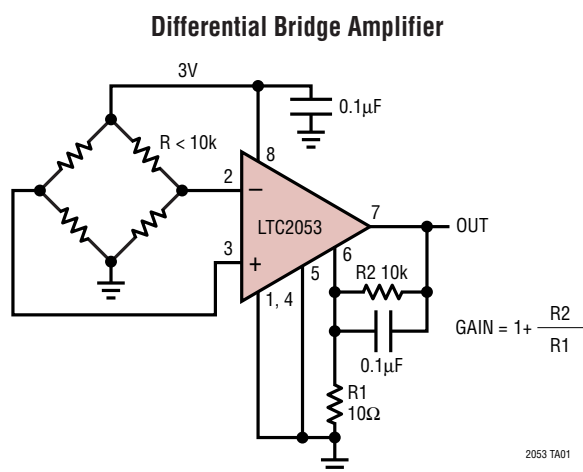
The LTC<sup>®</sup>2053 is a high precision instrumentation amplifier. The CMRR is typically 116dB with a single or dual 5V supply and is independent of gain. The input offset voltage is guaranteed below 10 $\mu$ V with a temperature drift of less than 50nV/ $^{\circ}$ C. The LTC2053 is easy to use; the gain is adjustable with two external resistors, like a traditional op amp.

The LTC2053 uses charge balanced sampled data techniques to convert a differential input voltage into a single ended signal that is in turn amplified by a zero-drift operational amplifier.

The differential inputs operate from rail-to-rail and the single ended output swings from rail-to-rail. The LTC2053 can be used in single supply applications, as low as 2.7V. It can also be used with dual  $\pm$ 5.5V supplies. The LTC2053 is available in an MS8 surface mount package. For space limited applications, the LTC2053 is available in a 3mm  $\times$  3mm  $\times$  0.8mm dual fine pitch leadless package (DFN).

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## TYPICAL APPLICATION



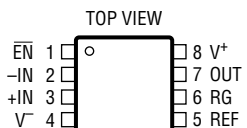
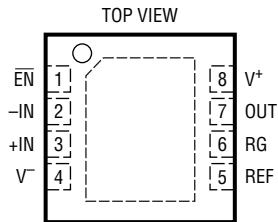
## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage ( $V^+$ to $V^-$ )	11V
Input Current	$\pm 10\text{mA}$
$ V_{IN^+} - V_{REF} $	5.5V
$ V_{IN^-} - V_{REF} $	5.5V
Output Short Circuit Duration	Indefinite

Operating Temperature Range	
LTC2053C	0°C to 70°C
LTC2053I	-40°C to 85°C
LTC2053H	-40°C to 125°C
Storage Temperature Range	
MS8 Package	-65°C to 150°C
DD Package	-65°C to 125°C
Lead Temperature (Soldering, 10 sec)	300°C

## PACKAGE/ORDER INFORMATION

 <p>MS8 PACKAGE 8-LEAD PLASTIC MSOP <math>T_{JMAX} = 150^\circ\text{C}</math>, <math>\theta_{JA} = 200^\circ\text{C/W}</math></p>	ORDER PART NUMBER	 <p>DD PACKAGE 8-LEAD (3mm x 3mm) PLASTIC DFN <math>T_{JMAX} = 125^\circ\text{C}</math>, <math>\theta_{JA} = 160^\circ\text{C/W}</math> UNDERSIDE METAL INTERNALLY CONNECTED TO <math>V^-</math> (PCB CONNECTION OPTIONAL)</p>	ORDER PART NUMBER*
	LTC2053CMS8 LTC2053IMS8 LTC2053HMS8		LTC2053CDD LTC2053IDD LTC2053HDD
	MS8 PART MARKING		DD PART MARKING
	LTVT LTJY LTAFB		LAEQ

\*The temperature grade (C, I, or H) of the LTC2053 in the DFN package is indicated on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $REF = 200\text{mV}$ . Output voltage swing is referenced to  $V^-$ . All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Error	$A_V = 1$	●		0.001	0.01	%
Gain Nonlinearity	$A_V = 1$	●		3	12	ppm
Input Offset Voltage (Note 2)	$V_{CM} = 200\text{mV}$			-5	$\pm 10$	$\mu\text{V}$
Average Input Offset Drift (Note 2)	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	●			$\pm 50$	$\text{nV}/^\circ\text{C}$
	$T_A = 85^\circ\text{C}$ to $125^\circ\text{C}$	●		-1	-2.5	$\mu\text{V}/^\circ\text{C}$
Average Input Bias Current (Note 3)	$V_{CM} = 1.2\text{V}$	●		4	10	nA
Average Input Offset Current (Note 3)	$V_{CM} = 1.2\text{V}$	●		1	3	nA
Input Noise Voltage	DC to 10Hz			2.5		$\mu\text{V}_{P-P}$
Common Mode Rejection Ratio (Notes 4, 5)	$A_V = 1$ , $V_{CM} = 0\text{V}$ to $3\text{V}$ , LTC2053C	●	105	113		dB
	$A_V = 1$ , $V_{CM} = 0.1\text{V}$ to $2.9\text{V}$ , LTC2053I	●	105	113		dB
	$A_V = 1$ , $V_{CM} = 0\text{V}$ to $3\text{V}$ , LTC2053I	●	95	113		dB
	$A_V = 1$ , $V_{CM} = 0.1\text{V}$ to $2.9\text{V}$ , LTC2053H	●	100			dB
	$A_V = 1$ , $V_{CM} = 0\text{V}$ to $3\text{V}$ , LTC2053H	●	90			dB

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $\text{REF} = 200\text{mV}$ . Output voltage swing is referenced to  $V^-$ . All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio (Note 6)	$V_S = 2.7\text{V to } 6\text{V}$	●	110	116		dB
Output Voltage Swing High	$R_L = 2\text{k to } V^-$ $R_L = 10\text{k to } V^-$	●	2.85	2.94		V
		●	2.95	2.98		V
Output Voltage Swing Low		●			20	mV
Supply Current	$V_{\overline{\text{EN}}} \leq 0.5\text{V}$ , No Load	●		0.75	1	mA
Supply Current, Shutdown	$V_{\overline{\text{EN}}} \geq 2.5\text{V}$				10	$\mu\text{A}$
$\overline{\text{EN}}$ Pin Input Low Voltage, $V_{\text{IL}}$					0.5	V
$\overline{\text{EN}}$ Pin Input High Voltage, $V_{\text{IH}}$			2.5			V
$\overline{\text{EN}}$ Pin Input Current	$V_{\overline{\text{EN}}} = V^-$			-0.5	-10	$\mu\text{A}$
Internal Op Amp Gain Bandwidth				200		kHz
Slew Rate				0.2		$\text{V}/\mu\text{s}$
Internal Sampling Frequency				3		kHz

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $\text{REF} = 200\text{mV}$ . Output voltage swing is referenced to  $V^-$ . All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Error	$A_V = 1$	●		0.001	0.01	%
Gain Nonlinearity	$A_V = 1$	●		3	10	ppm
Input Offset Voltage (Note 2)	$V_{\text{CM}} = 200\text{mV}$			-5	$\pm 10$	$\mu\text{V}$
Average Input Offset Drift (Note 2)	$T_A = -40^\circ\text{C to } 85^\circ\text{C}$ $T_A = 85^\circ\text{C to } 125^\circ\text{C}$	●			$\pm 50$	$\text{nV}/^\circ\text{C}$
		●		-1	-2.5	$\mu\text{V}/^\circ\text{C}$
Average Input Bias Current (Note 3)	$V_{\text{CM}} = 1.2\text{V}$	●		4	10	nA
Average Input Offset Current (Note 3)	$V_{\text{CM}} = 1.2\text{V}$	●		1	3	nA
Common Mode Rejection Ratio (Notes 4, 5)	$A_V = 1$ , $V_{\text{CM}} = 0\text{V to } 5\text{V}$ , LTC2053C	●	105	116		dB
	$A_V = 1$ , $V_{\text{CM}} = 0.1\text{V to } 4.9\text{V}$ , LTC2053I	●	105	116		dB
	$A_V = 1$ , $V_{\text{CM}} = 0\text{V to } 5\text{V}$ , LTC2053I	●	95	116		dB
	$A_V = 1$ , $V_{\text{CM}} = 0.1\text{V to } 4.9\text{V}$ , LTC2053H	●	100			dB
	$A_V = 1$ , $V_{\text{CM}} = 0\text{V to } 5\text{V}$ , LTC2053H	●	90			dB
Power Supply Rejection Ratio (Note 6)	$V_S = 2.7\text{V to } 6\text{V}$	●	110	116		dB
Output Voltage Swing High	$R_L = 2\text{k to } V^-$ $R_L = 10\text{k to } V^-$	●	4.85	4.94		V
		●	4.95	4.98		V
Output Voltage Swing Low		●			20	mV
Supply Current	$V_{\overline{\text{EN}}} \leq 0.5\text{V}$ , No Load	●		0.85	1.1	mA
Supply Current, Shutdown	$V_{\overline{\text{EN}}} \geq 4.5\text{V}$				10	$\mu\text{A}$
$\overline{\text{EN}}$ Pin Input Low Voltage, $V_{\text{IL}}$					0.5	V
$\overline{\text{EN}}$ Pin Input High Voltage, $V_{\text{IH}}$			4.5			V
$\overline{\text{EN}}$ Pin Input Current	$V_{\overline{\text{EN}}} = V^-$			-1	-10	$\mu\text{A}$
Internal Op Amp Gain Bandwidth				200		kHz
Slew Rate				0.2		$\text{V}/\mu\text{s}$
Internal Sampling Frequency				3		kHz

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = -5\text{V}$ ,  $\text{REF} = 0\text{V}$ .

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Error	$A_V = 1$	●		0.001	0.01	%
Gain Nonlinearity	$A_V = 1$	●		3	10	ppm
Input Offset Voltage (Note 2)	$V_{CM} = 0\text{V}$			10	$\pm 20$	$\mu\text{V}$
Average Input Offset Drift (Note 2)	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	●			$\pm 50$	$\text{nV}/^\circ\text{C}$
	$T_A = 85^\circ\text{C}$ to $125^\circ\text{C}$	●		-1	-2.5	$\mu\text{V}/^\circ\text{C}$
Average Input Bias Current (Note 3)	$V_{CM} = 1\text{V}$	●		4	10	$\text{nA}$
Average Input Offset Current (Note 3)	$V_{CM} = 1\text{V}$	●		1	3	$\text{nA}$
Common Mode Rejection Ratio (Notes 4, 5)	$A_V = 1$ , $V_{CM} = -5\text{V}$ to $5\text{V}$ , LTC2053C	●	105	118		$\text{dB}$
	$A_V = 1$ , $V_{CM} = -4.9\text{V}$ to $4.9\text{V}$ , LTC2053I	●	105	118		$\text{dB}$
	$A_V = 1$ , $V_{CM} = -5\text{V}$ to $5\text{V}$ , LTC2053I	●	95	118		$\text{dB}$
	$A_V = 1$ , $V_{CM} = -4.9\text{V}$ to $4.9\text{V}$ , LTC2053H	●	100			$\text{dB}$
	$A_V = 1$ , $V_{CM} = -5\text{V}$ to $5\text{V}$ , LTC2053H	●	90			$\text{dB}$
Power Supply Rejection Ratio (Note 6)	$V_S = 2.7\text{V}$ to $11\text{V}$	●	110	116		$\text{dB}$
Maximum Output Voltage Swing	$R_L = 2\text{k}$ to GND, LTC2053C, LTC2053I	●	$\pm 4.5$	$\pm 4.8$		$\text{V}$
	$R_L = 10\text{k}$ to GND, LTC2053C, LTC2053I, LTC2053H	●	$\pm 4.6$	$\pm 4.9$		$\text{V}$
	$R_L = 2\text{k}$ to GND, LTC2053H	●	$\pm 4.4$	$\pm 4.8$		$\text{V}$
Supply Current	$V_{EN} \leq -4.5\text{V}$ , No Load	●		0.95	1.3	$\text{mA}$
Supply Current, Shutdown	$V_{EN} \geq 4.5\text{V}$				20	$\mu\text{A}$
$\overline{\text{EN}}$ Pin Input Low Voltage, $V_{IL}$					-4.5	$\text{V}$
$\overline{\text{EN}}$ Pin Input High Voltage, $V_{IH}$			4.5			$\text{V}$
$\overline{\text{EN}}$ Pin Input Current	$V_{EN} = V^-$			-3	-20	$\mu\text{A}$
Internal Op Amp Gain Bandwidth				200		$\text{kHz}$
Slew Rate				0.2		$\text{V}/\mu\text{s}$
Internal Sampling Frequency				3		$\text{kHz}$

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic test systems.  $V_{OS}$  is measured to a limit determined by test equipment capability.

**Note 3:** If the total source resistance is less than  $10\text{k}$ , no DC errors result from the input bias currents or the mismatch of the input bias currents or the mismatch of the resistances connected to  $-\text{IN}$  and  $+\text{IN}$ .

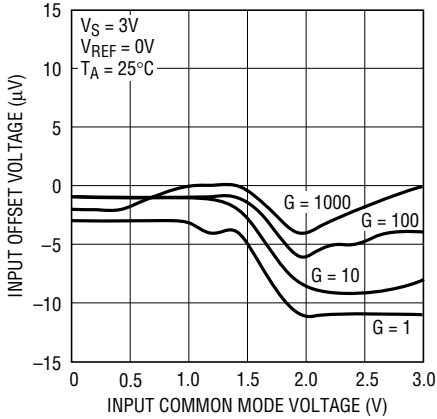
**Note 4:** The CMRR with a voltage gain,  $A_V$ , larger than 10 is  $120\text{dB}$  (typ).

**Note 5:** At temperatures above  $70^\circ\text{C}$ , the common mode rejection ratio lowers when the common mode input voltage is within  $100\text{mV}$  of the supply rails.

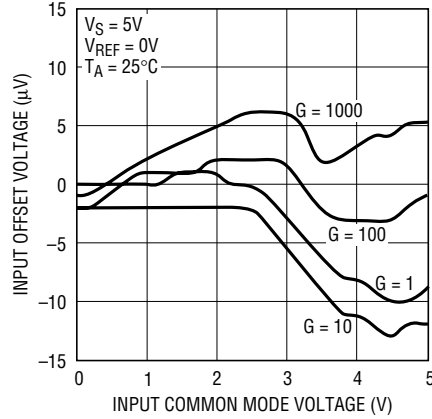
**Note 6:** The power supply rejection ratio (PSRR) measurement accuracy depends on the proximity of the power supply bypass capacitor to the device under test. Because of this, the PSRR is 100% tested to relaxed limits at final test. However, their values are guaranteed by design to meet the data sheet limits.

# TYPICAL PERFORMANCE CHARACTERISTICS

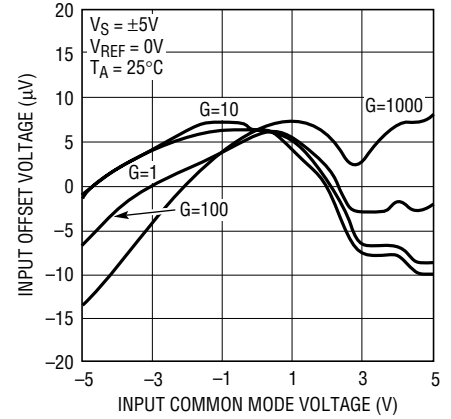
**Input Offset Voltage vs Input Common Mode Voltage**



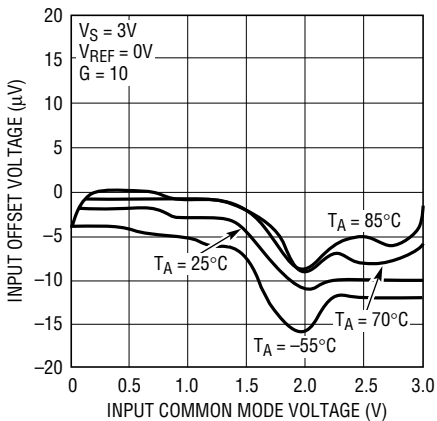
**Input Offset Voltage vs Input Common Mode Voltage**



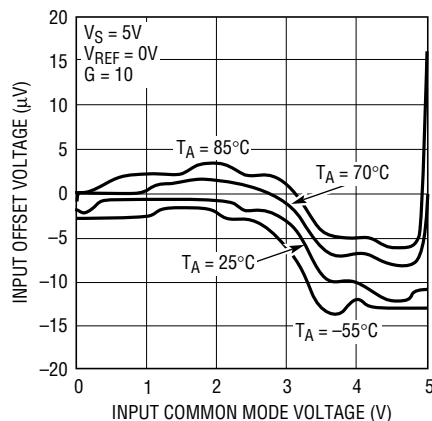
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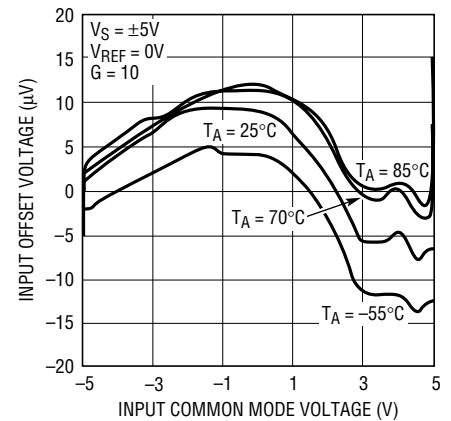
**Input Offset Voltage vs Input Common Mode Voltage**



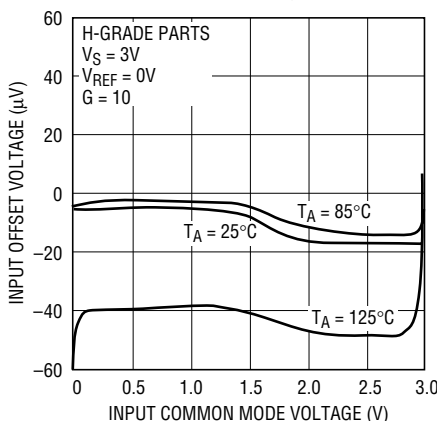
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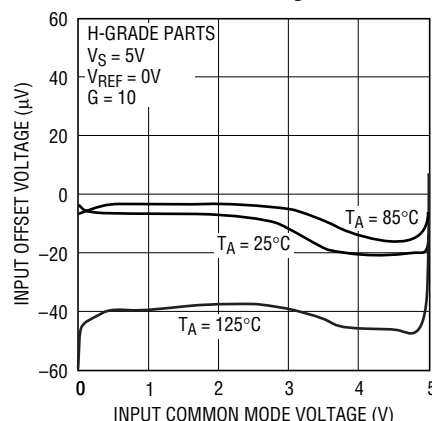
**Input Offset Voltage vs Input Common Mode Voltage**



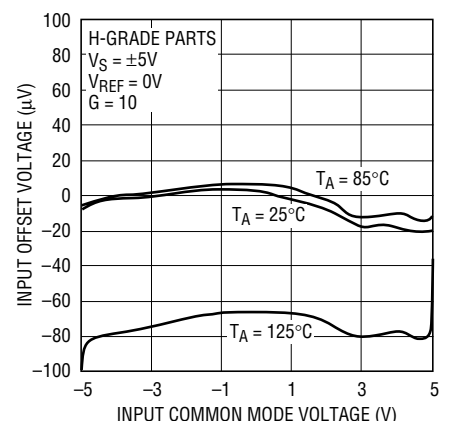
**Input Offset Voltage vs Input Common Mode Voltage**



**Input Offset Voltage vs Input Common Mode Voltage**

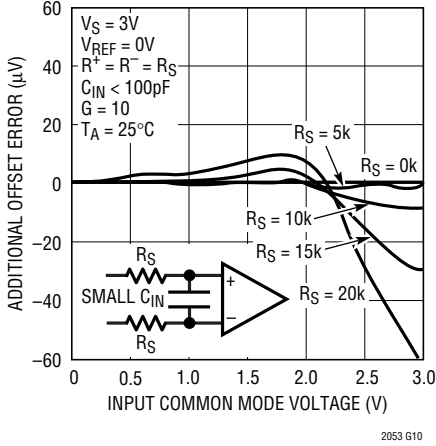


**Input Offset Voltage vs Input Common Mode Voltage**

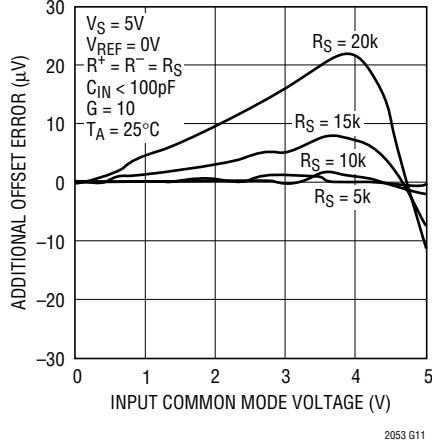


TYPICAL PERFORMANCE CHARACTERISTICS

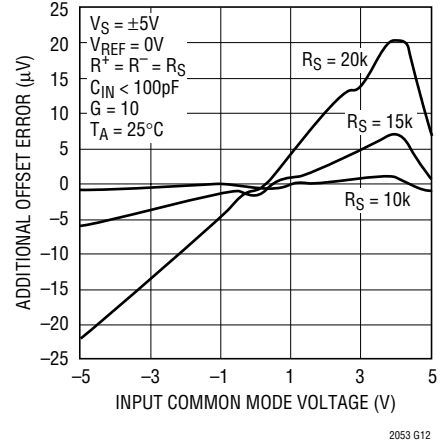
Error Due to Input  $R_S$  vs Input Common Mode ( $C_{IN} < 100pF$ )



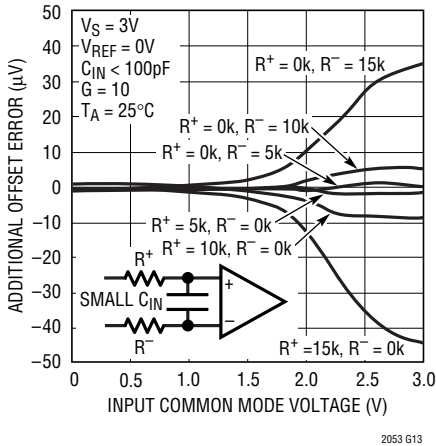
Error Due to Input  $R_S$  vs Input Common Mode ( $C_{IN} < 100pF$ )



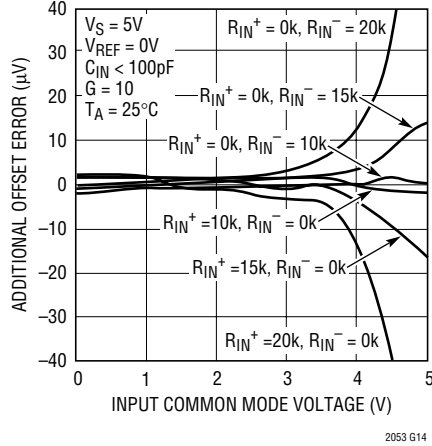
Error Due to Input  $R_S$  vs Input Common Mode ( $C_{IN} < 100pF$ )



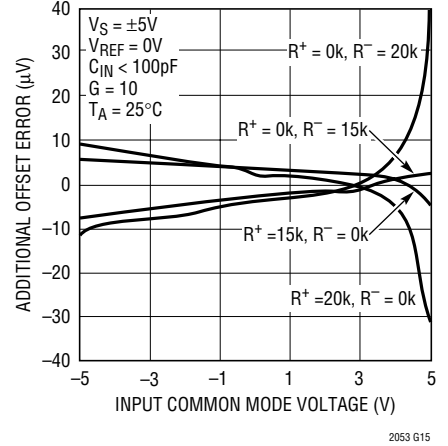
Error Due to Input  $R_S$  Mismatch vs Input Common Mode ( $C_{IN} < 100pF$ )



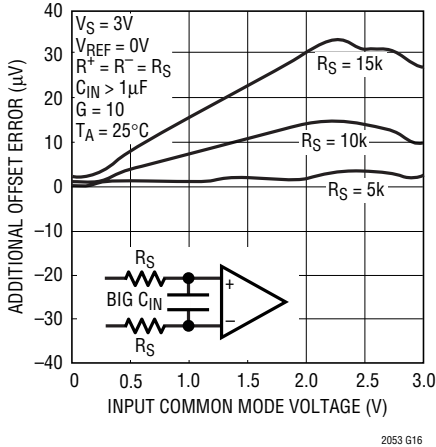
Error Due to Input  $R_S$  Mismatch vs Input Common Mode ( $C_{IN} < 100pF$ )



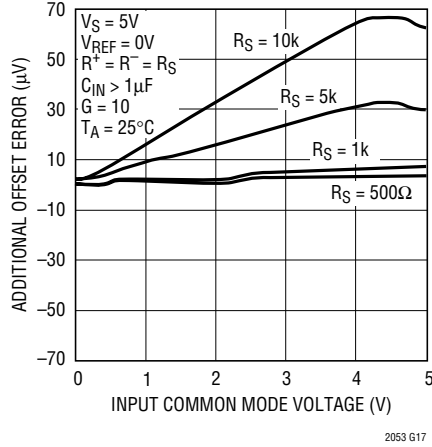
Error Due to Input  $R_S$  Mismatch vs Input Common Mode ( $C_{IN} < 100pF$ )



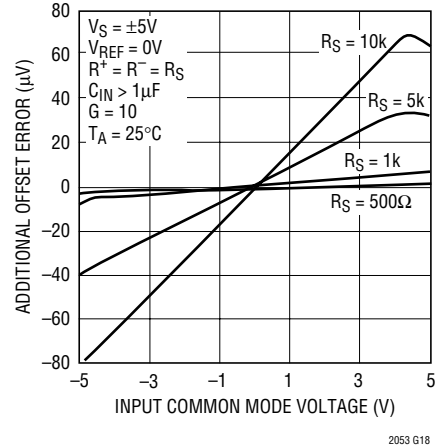
Error Due to Input  $R_S$  vs Input Common Mode ( $C_{IN} > 1\mu F$ )



Error Due to Input  $R_S$  vs Input Common Mode ( $C_{IN} > 1\mu F$ )

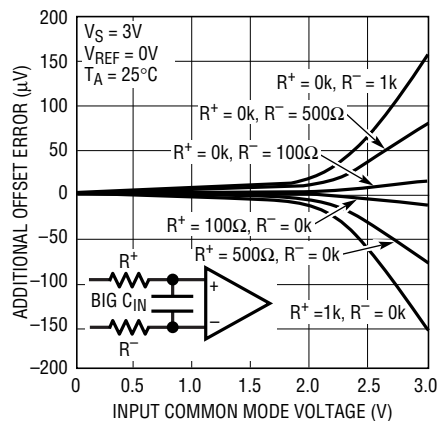


Error Due to Input  $R_S$  vs Input Common Mode ( $C_{IN} > 1\mu F$ )



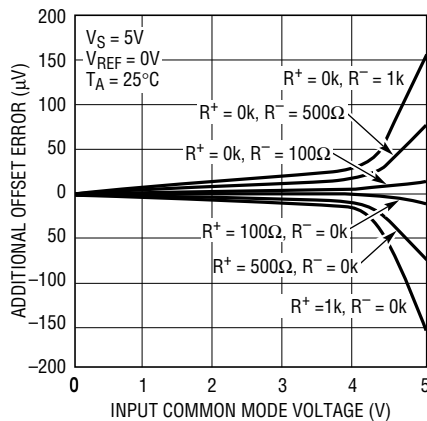
# TYPICAL PERFORMANCE CHARACTERISTICS

**Error Due to Input  $R_S$  Mismatch vs Input Common Mode ( $C_{IN} > 1\mu F$ )**



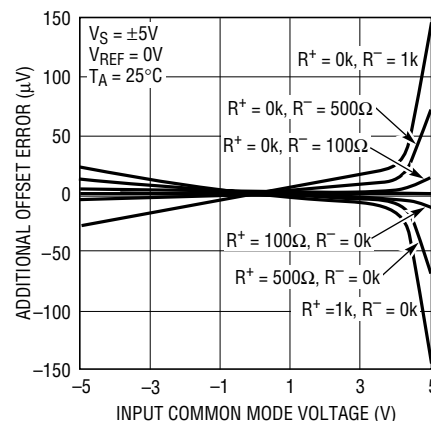
2053 G19

**Error Due to Input  $R_S$  Mismatch vs Input Common Mode ( $C_{IN} > 1\mu F$ )**



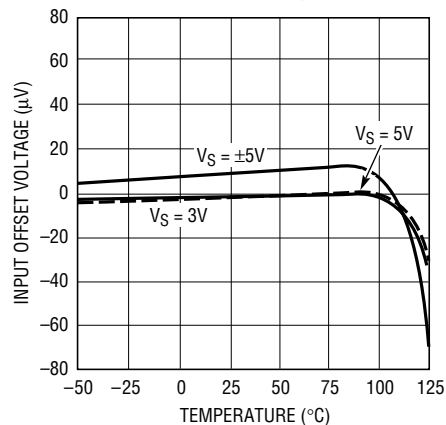
2053 G20

**Error Due to Input  $R_S$  Mismatch vs Input Common Mode ( $C_{IN} > 1\mu F$ )**



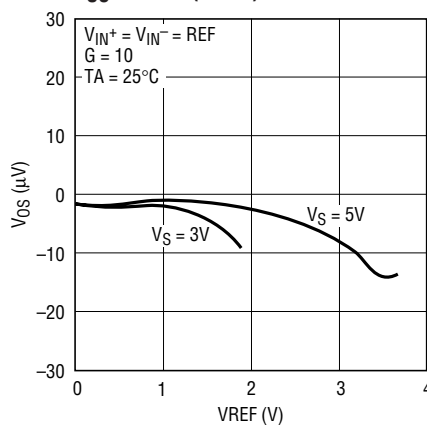
2053 G21

**Offset Voltage vs Temperature**



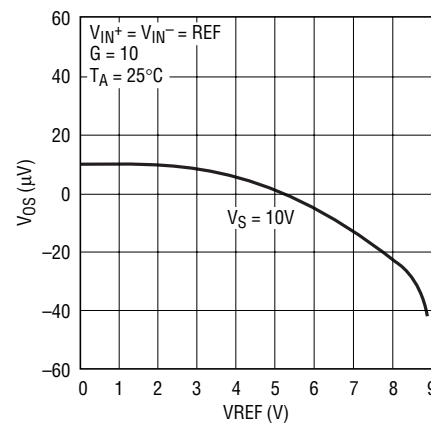
2053 G22

**$V_{OS}$  vs REF (Pin 5)**



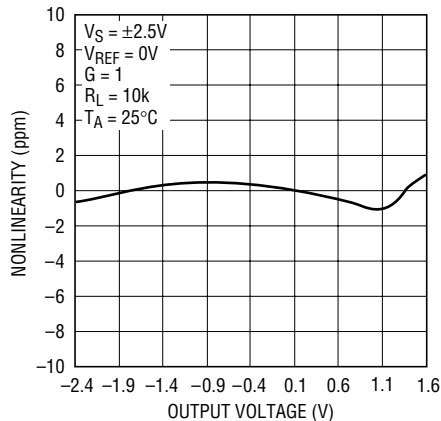
2053 G23

**$V_{OS}$  vs REF (Pin 5)**



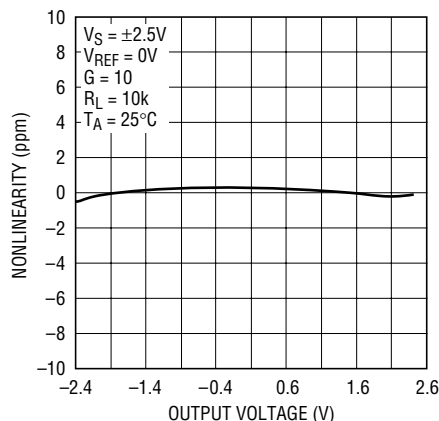
2053 G24

**Gain Nonlinearity, G = 1**



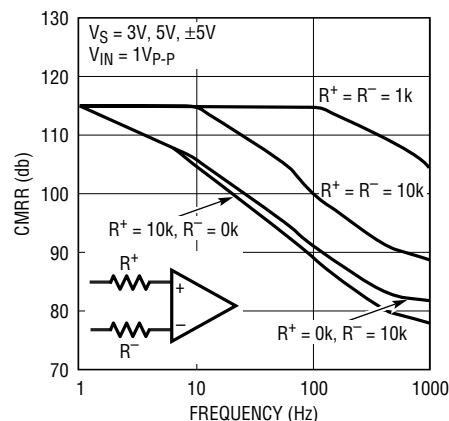
2053 G25

**Gain Nonlinearity, G = 10**



2053 G26

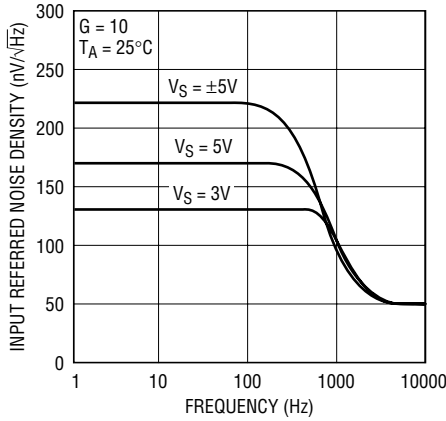
**CMRR vs Frequency**



2053 G27

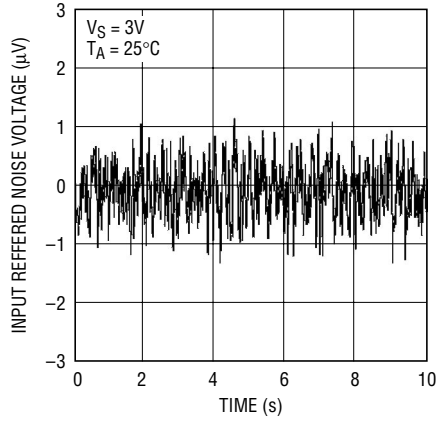
# TYPICAL PERFORMANCE CHARACTERISTICS

**Input Voltage Noise Density vs Frequency**



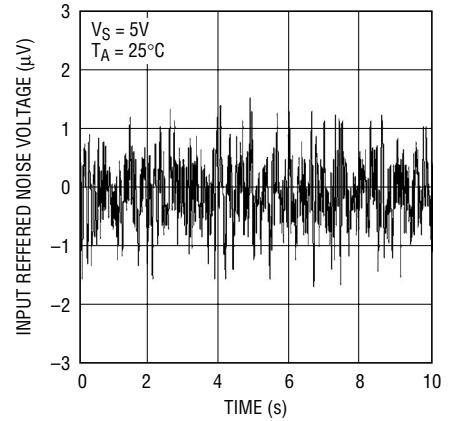
2053 G27

**Input Referred Noise in 10Hz Bandwidth**



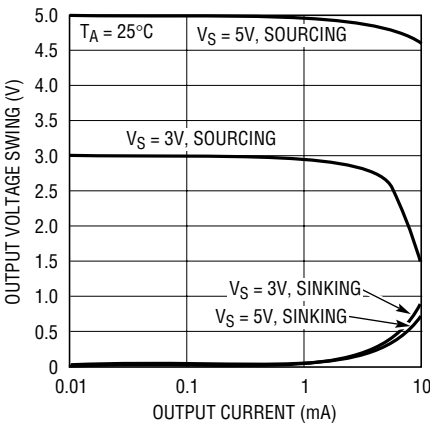
2053 G29

**Input Referred Noise in 10Hz Bandwidth**



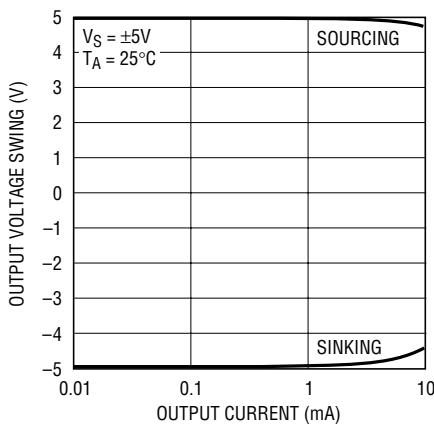
2053 G30

**Output Voltage Swing vs Output Current**



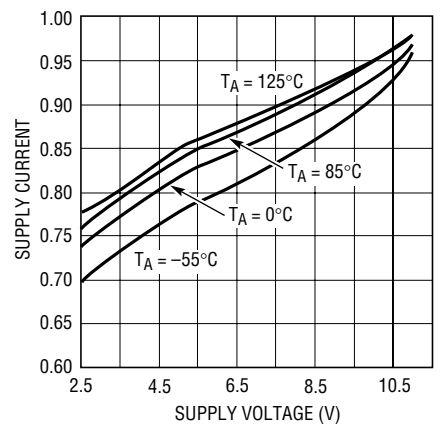
2053 G31

**Output Voltage Swing vs Output Current**



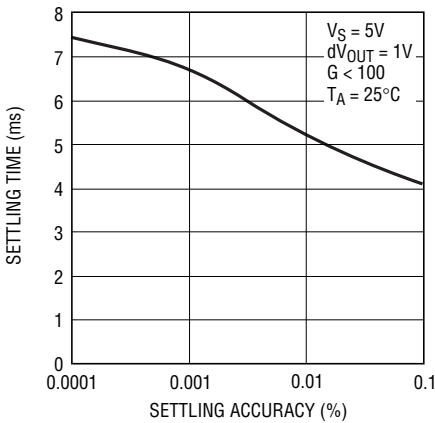
2053 G32

**Supply Current vs Supply Voltage**



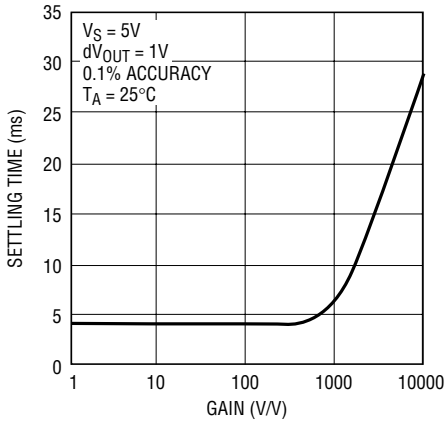
2053 G33

**Low Gain Settling Time vs Settling Accuracy**



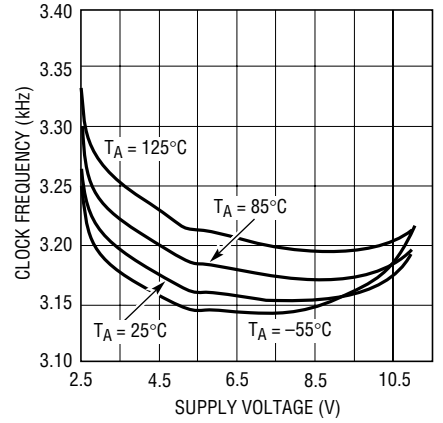
2053 G34

**Settling Time vs Gain**



2053 G35

**Internal Clock Frequency vs Supply Voltage**



2053 G36

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## PIN FUNCTIONS

$\overline{\text{EN}}$  (Pin 1): Active Low Enable Pin.

$-IN$  (Pin 2): Inverting Input.

$+IN$  (Pin 3): Noninverting Input.

$V^-$  (Pin 4): Negative Supply.

REF (Pin 5): Voltage Reference ( $V_{REF}$ ) for Amplifier Output.

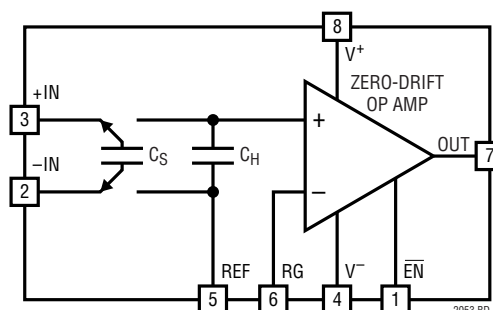
RG (Pin 6): Inverting Input of Internal Op Amp. With a resistor, R2, connected between the OUT pin and the RG pin and a resistor, R1, between the RG pin and the REF pin, the DC gain is given by  $1 + R2 / R1$ .

OUT (Pin 7): Amplifier Output.

$$V_{OUT} = \text{GAIN} (V_{+IN} - V_{-IN}) + V_{REF}$$

$V^+$  (Pin 8): Positive Supply.

## BLOCK DIAGRAM



## APPLICATIONS INFORMATION

### Theory of Operation

The LTC2053 uses an internal capacitor ( $C_S$ ) to sample a differential input signal riding on a DC common mode voltage (see Block Diagram). This capacitor's charge is transferred to a second internal hold capacitor ( $C_H$ ) translating the common mode of the input differential signal to that of the REF pin. The resulting signal is amplified by a zero-drift op amp in the noninverting configuration. The RG pin is the negative input of this op amp and allows external programmability of the DC gain. Simple filtering can be realized by using an external capacitor across the feedback resistor.

### Input Voltage Range

The input common mode voltage range of the LTC2053 is rail-to-rail. However, the following equation limits the size of the differential input voltage:

$$V^- \leq (V_{+IN} - V_{-IN}) + V_{REF} \leq V^+ - 1.3$$

Where  $V_{+IN}$  and  $V_{-IN}$  are the voltages of the  $+IN$  and  $-IN$  pins respectively,  $V_{REF}$  is the voltage at the REF pin and  $V^+$  is the positive supply voltage.

For example, with a 3V single supply and a 0V to 100mV differential input voltage,  $V_{REF}$  must be between 0V and 1.6V.

### $\pm 5$ Volt Operation

When using the LTC2053 with supplies over 5.5V, care must be taken to limit the maximum difference between any of the input pins ( $+IN$  or  $-IN$ ) and the REF pin to 5.5V; if not, the device will be damaged. For example, if rail-to-rail input operation is desired when the supplies are at  $\pm 5V$ , the REF pin should be 0V,  $\pm 0.5V$ . As a second example, if  $V^+$  is 10V and  $V^-$  and REF are at 0V, the inputs should not exceed 5.5V.

## APPLICATIONS INFORMATION

### Settling Time

The sampling rate is 3kHz and the input sampling period during which  $C_S$  is charged to the input differential voltage  $V_{IN}$  is approximately  $150\mu s$ . First assume that on each input sampling period,  $C_S$  is charged fully to  $V_{IN}$ . Since  $C_S = C_H (= 1000pF)$ , a change in the input will settle to N bits of accuracy at the op amp noninverting input after N clock cycles or  $333\mu s(N)$ . The settling time at the OUT pin is also affected by the settling of the internal op amp. Since the gain bandwidth of the internal op amp is typically 200kHz, the settling time is dominated by the switched capacitor front end for gains below 100 (see Typical Performance Characteristics).

### Input Current

Whenever the differential input  $V_{IN}$  changes,  $C_H$  must be charged up to the new input voltage via  $C_S$ . This results in an input charging current during each input sampling period. Eventually,  $C_H$  and  $C_S$  will reach  $V_{IN}$  and, ideally, the input current would go to zero for DC inputs.

In reality, there are additional parasitic capacitors which disturb the charge on  $C_S$  every cycle even if  $V_{IN}$  is a DC voltage. For example, the parasitic bottom plate capacitor on  $C_S$  must be charged from the voltage on the REF pin to the voltage on the  $-IN$  pin every cycle. The resulting input

charging current decays exponentially during each input sampling period with a time constant equal to  $R_S C_S$ . **If the voltage disturbance due to these currents settles before the end of the sampling period, there will be no errors due to source resistance or the source resistance mismatch between  $-IN$  and  $+IN$ . With  $R_S$  less than 10k, no DC errors occur due to this input current.**

In the Typical Performance Characteristics section of this data sheet, there are curves showing the additional error from non-zero source resistance in the inputs. If there are no large capacitors across the inputs, the amplifier is less sensitive to source resistance and source resistance mismatch. When large capacitors are placed across the inputs, the input charging currents described above result in larger DC errors, especially with source resistor mismatches.

### Power Supply Bypassing

The LTC2053 uses a sampled data technique and therefore contains some clocked digital circuitry. It is therefore sensitive to supply bypassing. For single or dual supply operation, a  $0.1\mu F$  ceramic capacitor must be connected between Pin 8 ( $V^+$ ) and Pin 4 ( $V^-$ ) with leads as short as possible.

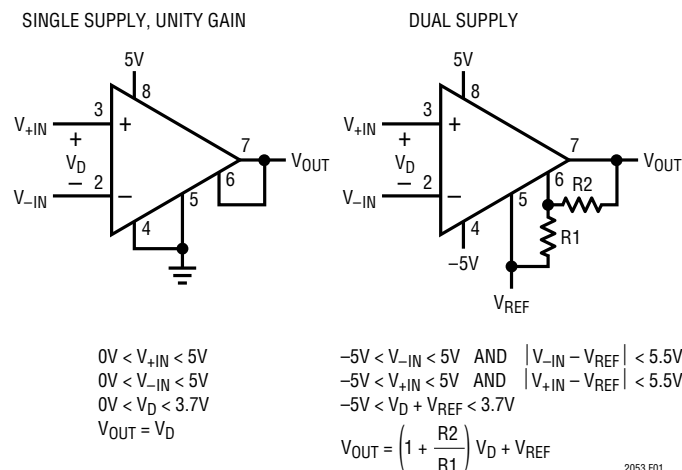
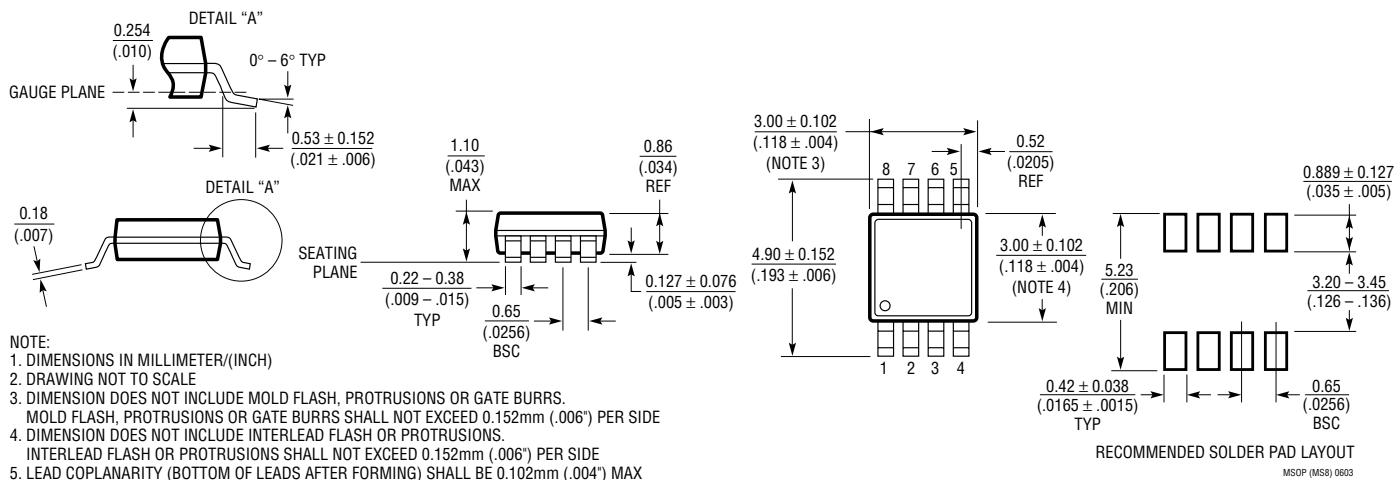


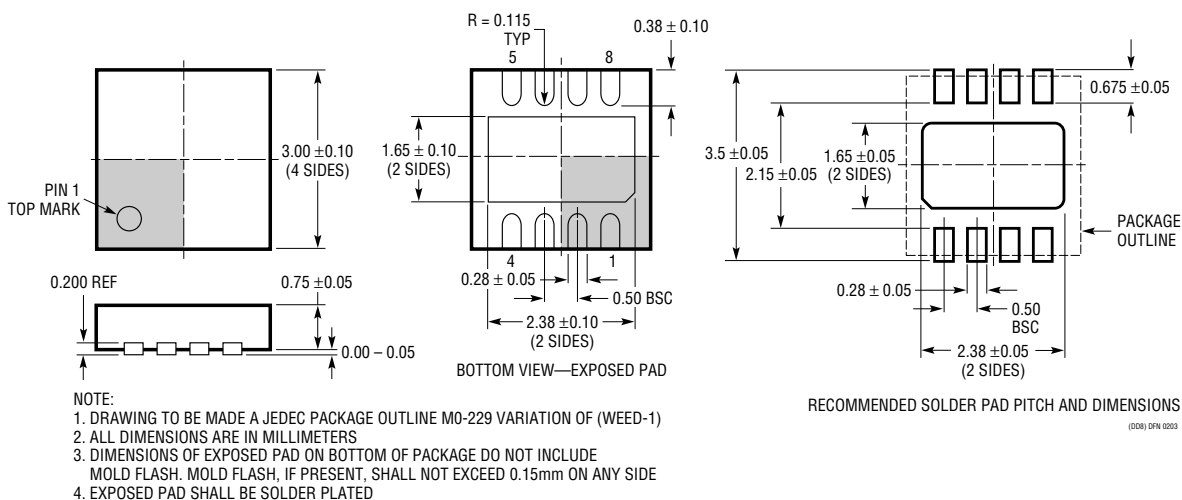
Figure 1

# PACKAGE DESCRIPTION

## MS8 Package 8-Lead Plastic MSOP (Reference LTC DWG # 05-08-1660)

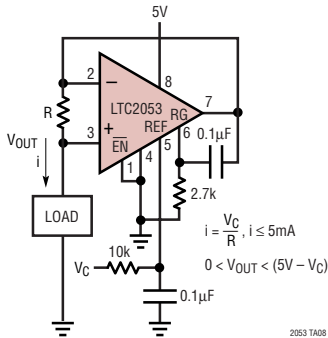


## DD Package 8-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1698)

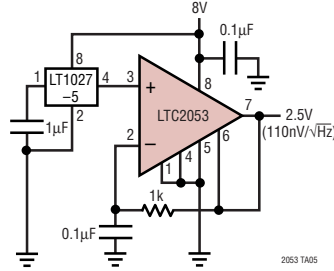


## TYPICAL APPLICATIONS

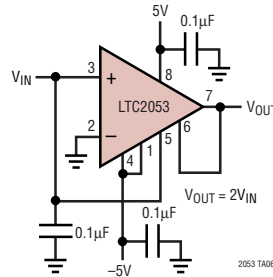
### Precision Current Source



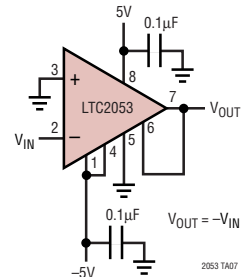
### Precision $\pm 2$ (Low Noise 2.5V Reference)



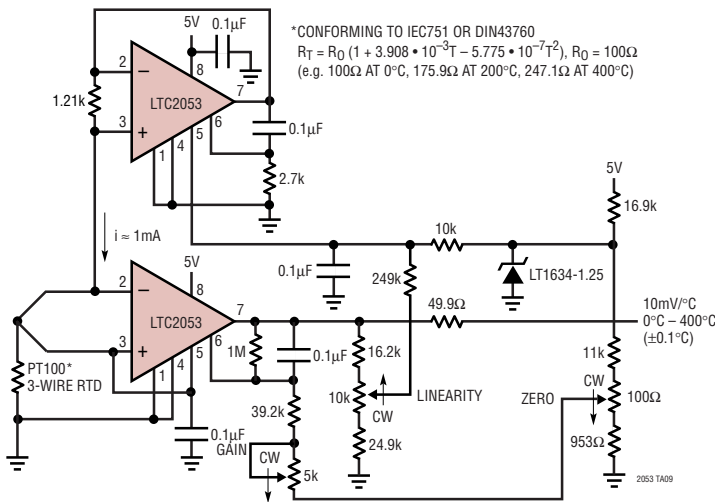
### Precision Doubler (General Purpose)



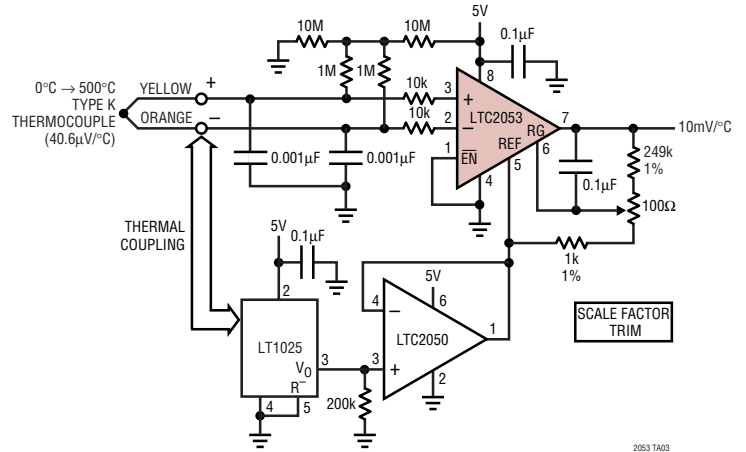
### Precision Inversion (General Purpose)



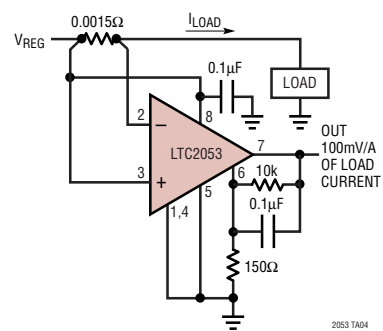
### Linearized Platinum RTD Amplifier



### Differential Thermocouple Amplifier



### High Side Power Supply Current Sense



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1167	Single Resistor Gain Programmable, Precision Instrumentation Amplifier	Single Gain Set Resistor: $G = 1$ to 10,000, Low Noise: $7.5\text{nV}/\sqrt{\text{Hz}}$
LTC2050	Zero-Drift Operation Amplifier	SOT-23 Package
LTC2051	Dual Zero-Drift Operational Amplifier	MS8 Package
LTC6800	Single Supply, Zero Drift, Rail-to-Rail Input and Output Instrumentation Amplifier	MS8 Package, 100µV Max $V_{OS}$ , 250nV/°C Max Drift

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