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**ARTIX-7 FPGA  
Development Board  
AX7A200  
User Manual**



## Version Record

Version	Date	Release By	Description
Rev 1.0	2019-07-10	Rachel Zhou	First Release

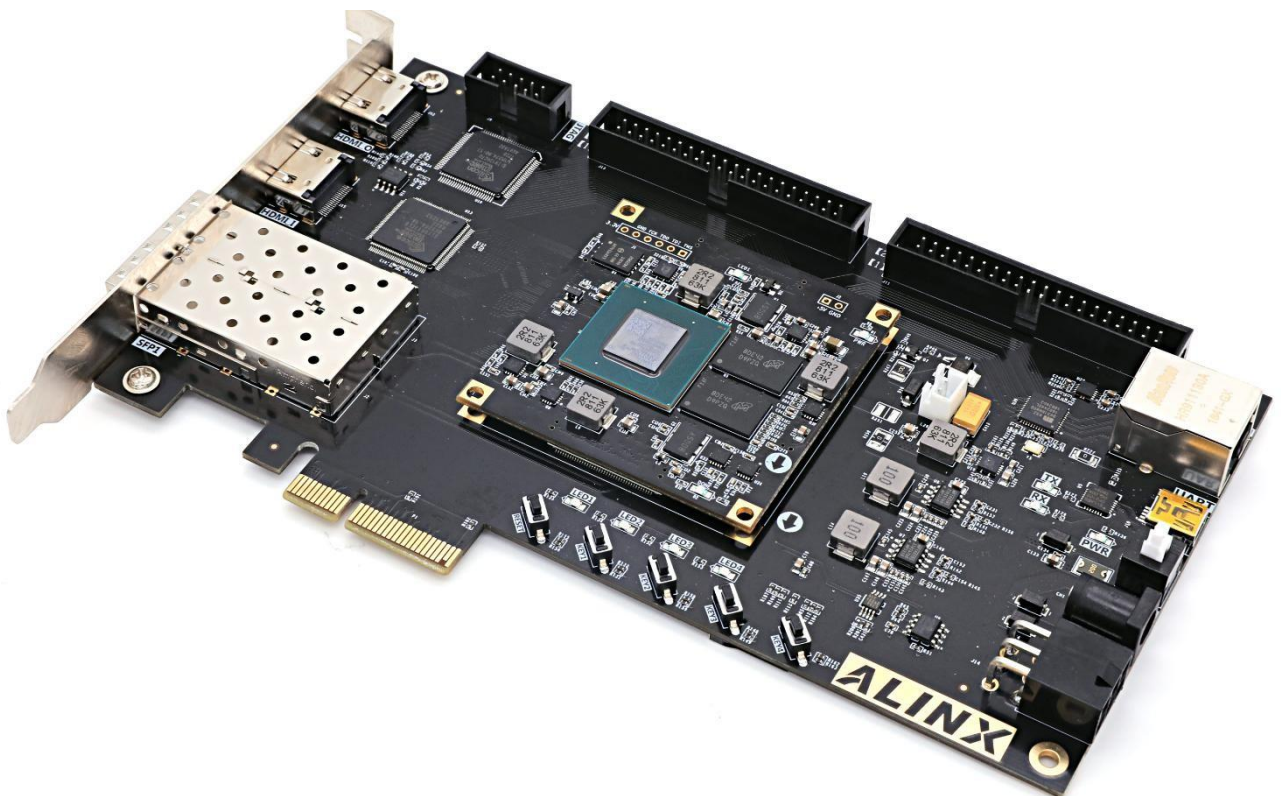
## Table of Contents

Version Record.....	2
Part 1: FPGA Development Board Introduction.....	6
Part 2: AC7A200 Core Board.....	10
Part 2.1: AC7A200 Core Board Introduction.....	10
Part 2.2: FPGA Chip.....	12
Part 2.3: Active Differential Crystal.....	13
Part 2.4: DDR3 DRAM.....	16
Part 2.5: QSPI Flash.....	19
Part 2.6: LED Light on Core Board.....	21
Part 2.7: JTAG Interface.....	22
Part 2.8: Power Interface on the Core Board.....	23
Part 2.9: Board to Board Connectors pin assignment.....	24
Part 2.10: Power Supply.....	31
Part 2.11: Size Dimension.....	34
Part 3: Carrier Board.....	35
Part 3.1: Carrier Board Introduction.....	35
Part 3.2: Gigabit Ethernet Interface.....	36
Part 3.3: SFP Interface.....	38
Part 3.4: PCIe x2 Interface.....	40
Part 3.5: HDMI output interface.....	41
Part 3.6: HDMI Input interface.....	43
Part 3.7: SD Card Slot.....	45
Part 3.8: USB-to-Uart Bridge Connector.....	46
Part 3.9: EEPROM 24LC04.....	48
Part 3.10: Temperature Sensor.....	49
Part 3.11: Expansion Header.....	50
Part 3.12: JTAG Interface.....	53

Part 3.13: Buttons.....	54
Part 3.14: LED Light.....	55
Part 3.15: Power Supply.....	57
Part 3.16: Fan.....	58
Part 3.17: Carrier Board Size Dimension.....	59

This ARTIX-7 FPGA development platform adopts the core board + carrier board mode, which is convenient for users to use the core board for secondary development.

In the design of carrier board, we have extended a wealth of interfaces for users, such as 1 PCIe2 interface, 2 SFP cage, 1 HDMI Output interface, 1 HDMI Input interface, 1 Gigabit Ethernet interfaces, Uart Interface, SD card slot etc. It meets user's requirements for PCIe high-speed data exchange, video transmission processing and industrial control. It is a "Versatile" ARTIX-7 FPGA development platform. It provides the possibility for high-speed video transmission, pre-validation and post-application of network, fiber and PCIe communication and data processing. This product is very suitable for students, engineers and other groups engaged in ARTIX-7 FPGA development.



## Part 1: FPGA Development Board Introduction

The entire structure of the AX7A200 FPGA development board is inherited from our consistent core board + carrier board model. A high-speed inter-board connector is used between the core board and the carrier board.

The core board is mainly composed of FPGA + 2 DDR3 + QSPI FLASH, which undertakes the functions of high-speed data processing and storage of FPGA, high-speed data reading and writing between FPGA and two DDR3s, data bit width is 32 bits, and the bandwidth of the whole system is up to 25Gb./s(800M\*32bit); The two DDR3 capacities are up to 8Gbit, which meets the need for high buffers during data processing. The selected FPGA is the XC7A200T chip of XILINX's ARTIX-7 series, in BGA 484 package. The communication frequency between the XC7A200T and DDR3 reaches 400Mhz and the data rate is 800Mhz, which fully meets the needs of high-speed multi-channel data processing. In addition, the XC7A200T FPGA features four GTP high-speed transceivers with speeds up to 6.6Gb/s per channel, making it ideal for fiber-optic communications and PCIe data communications.

The AX7A200 carrier board expands its rich peripheral interface, including 1 PClex2 interface, 2 SFP Interface, 1 HDMI Output interface, 1 HDMI Input interface, 1 Uart Interface, 1 Gigabit Ethernet interfaces, 1 SD card slot, 2-way 40-pin expansion header, some buttons, LED and EEPROM circuit.

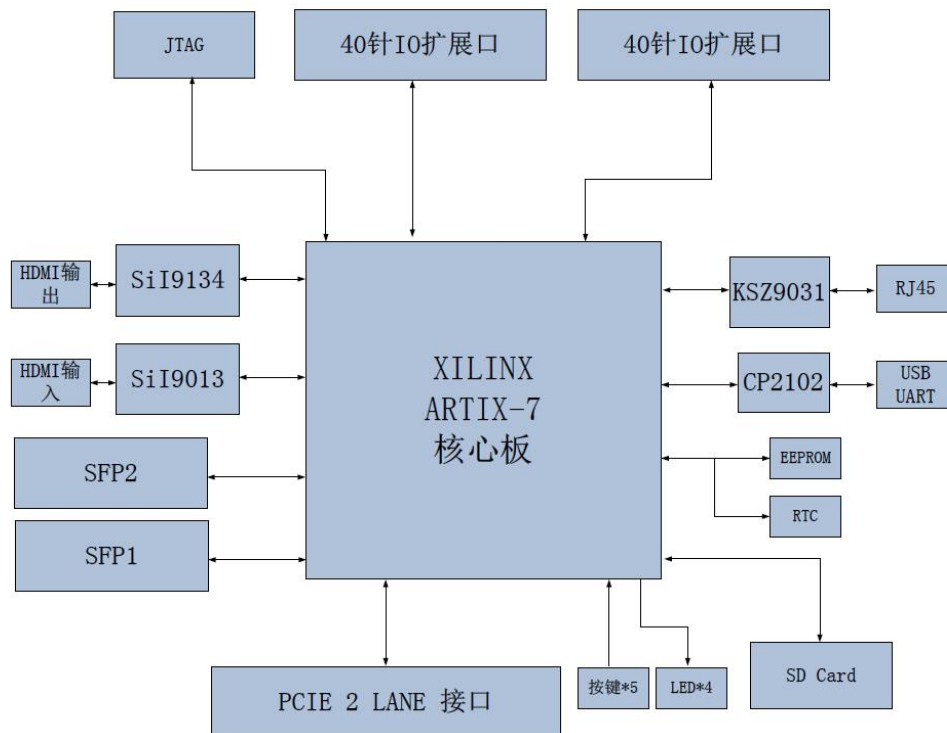


Figure 1-1-1: The Schematic Diagram of the AX7A200

Through this diagram, you can see the interfaces and functions that the AX7102 FPGA Development Board contains:

➤ Artix-7 FPGA core board

The core board consists of XC7A200T + 8Gb DDR3 + 128Mb QSPI FLASH. There are two high-precision Sitime LVDS differential crystals, one at 200MHz and the other at 125MHz, providing stable clock input for FPGA systems and GTP modules.

➤ 1-channel PCIe x2 interface

Supports PCI Express 2.0 standard, provides PCIe x 2 high-speed data transmission interface, single channel communication rate up to 5Gbaud

➤ 2-channel high-speed SFP Interface

The two high-speed transceivers of the GTP transceiver of ARTIX-7 FPGA are connected to the transmission and reception of two optical modules to realize four high-speed optical fiber communication

interfaces. Each fiber optic data communication receives and transmits at speeds up to 6.6 Gb/s.

➤ 1-channel Gigabit Ethernet Interface RJ-45 interface

The Gigabit Ethernet interface chip uses Micrel's KSZ9031RNX Ethernet PHY chip to provide network communication services to users. The KSZ9031RNX chip supports 10/100/1000 Mbps network transmission rates; full duplex and adaptive.

➤ 1-channel HDMI Output interface

Silion Image's SIL9134 HDMI encoding chip is selected to support up to 1080P@60Hz output and support 3D output.

➤ 1-channel HDMI Input interface

Silion Image's SIL9011/ SIL9013 HDMI decoder chip is selected, which supports up to 1080P@60Hz input and supports data output in different formats.

➤ 1-channel USB-to-Uart interface

1-channel USB-to-Uart interface for communication with the computer for user debugging. The serial port chip is the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface is the MINI USB interface.

➤ Micro SD card holder

1-port Micro SD card slot, support SD mode and SPI mode

➤ EEPROM

Onboard an IIC interface EEPROM 24LC04

➤ 2-way 40-pin expansion port

Reserve 2-way 40-pin 0.1inch pitch expansion port can be connected to various AXSOC modules (binocular camera, TFT LCD screen, high-speed AD module, etc.). The expansion port contains 1 channel 5V power supply, 2 channel 3.3V power supply, 3 way ground, 34 IOs port.

➤ JTAG Interface



A 10-pin 0.1 inch spacing standard JTAG ports for FPGA program download and debugging.

➤ Button

4 buttons; 1 reset button (on the core board)

➤ LED Light

5 user LEDs (1 on the core board and 4 on the carrier board)

## Part 2: AC7A200 Core Board

### Part 2.1: AC7A200 Core Board Introduction

AC7A200 (core board model, the same below) FPGA core board, it is based on XILINX's ARTIX-7 series 100T XC7A200T-2FBG484I. It is a high-performance core board with high speed, high bandwidth and high capacity. It is suitable for high-speed data communication, video image processing, high-speed data acquisition etc.

This AC7A200 core board uses two pieces of MICRON's MT41J256M16HA-125 DDR3 chip, each DDR has a capacity of 4Gbit; two DDR chips are combined into a 32-bit data bus width, and the read/write data bandwidth between FPGA and DDR3 is up to 25Gb; such a configuration can meet the needs of high bandwidth data processing.

The AC7A200 core board expands 180 standard IO ports of 3.3V level, 15 standard IO ports of 1.5V level, and 4 pairs of GTP high speed RX/TX differential signals. For users who need a lot of IO, this core board will be a good choice. Moreover, the routing between the FPGA chip and the interface is equal length and differential processing, and the core board size is only 2.36 inch \*2.36 inch, which is very suitable for secondary development.

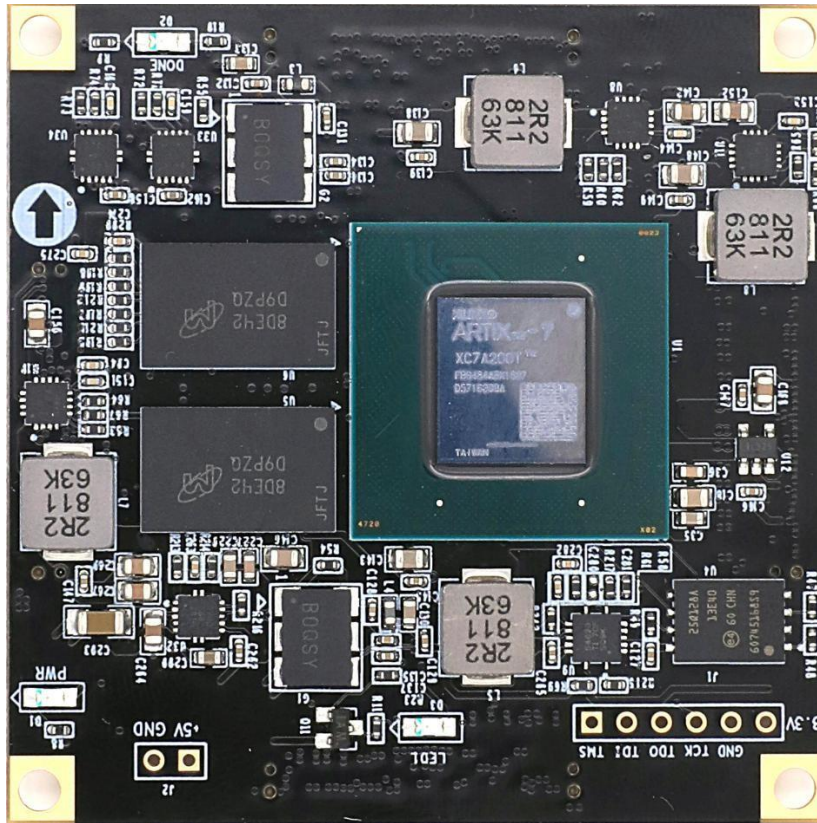


Figure 2-1-1: AC7A200 Core Board (Front View)

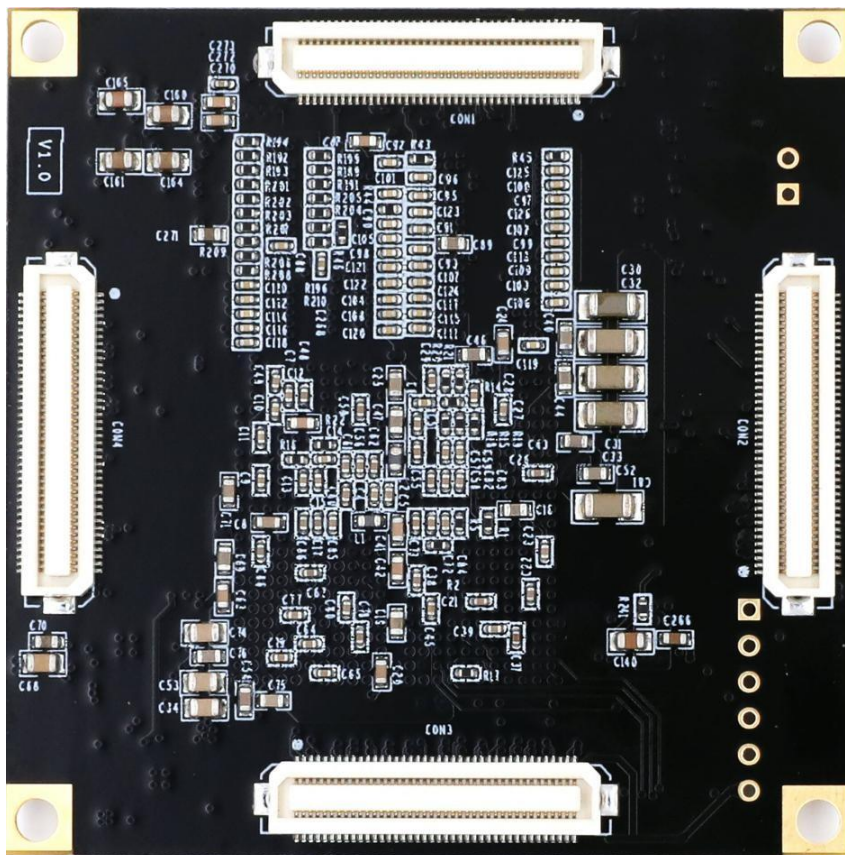


Figure 2-1-2: AC7A200 Core Board (Rear View)

## Part 2.2: FPGA Chip

As mentioned above, the FPGA model we use is XC7A200T-2FBG484I, which belongs to Xilinx's Artix-7 series. The speed grade is 2, and the temperature grade is industry grade. This model is a FGG484 package with 484 pins. Xilinx ARTIX-7 FPGA chip naming rules as below

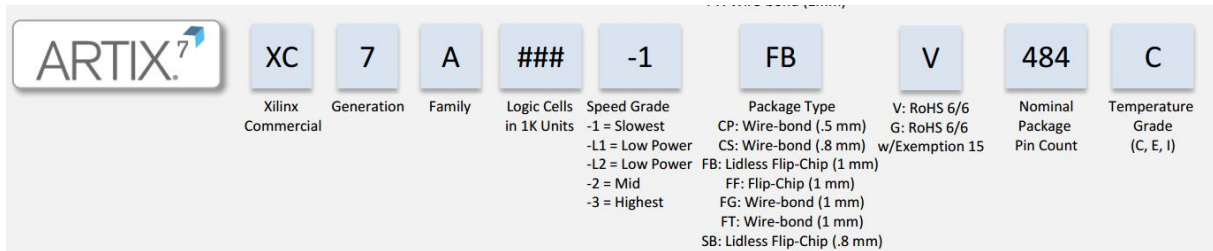


Figure 2-2-1: The Specific Chip Model Definition of ARTIX-7 Series

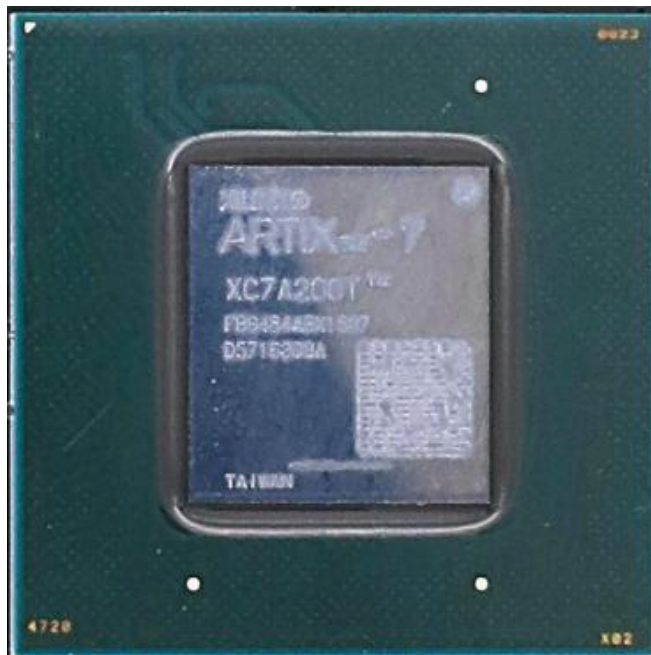


Figure 2-2-2: FPGA chip on board

The main parameters of the FPGA chip XC7A200T are as follows

Name	Specific parameters
Logic Cells	215360
Slices	33650
CLB flip-flops	269200
Block RAM (kb)	13140

DSP Slices	740
PCIe Gen2	1
XADC	1 XADC, 12bit, 1Mbps AD
GTP Transceiver	4 GTP, 6.6Gb/s max
Speed Grade	-2
Temperature Grade	Industrial

## FPGA power supply system

Artix-7 FPGA power supplies are  $V_{CCINT}$ ,  $V_{CCBRAM}$ ,  $V_{CCAUX}$ ,  $V_{CCO}$ ,  $V_{MGTAVCC}$  and  $V_{MGTAVTT}$ .  $V_{CCINT}$  is the FPGA core power supply pin, which needs to be connected to 1.0V;  $V_{CCBRAM}$  is the power supply pin of FPGA Block RAM, connect to 1.0V;  $V_{CCAUX}$  is FPGA auxiliary power supply pin, connect 1.8V;  $V_{CCO}$  is the voltage of each BANK of FPGA, including BANK0, BANK13~16, BANK34~35. On AC7A200 FPGA core board, BANK34 and BANK35 need to be connected to DDR3, the voltage connection of BANK is 1.5V, and the voltage of other BANK is 3.3V. The  $V_{CCO}$  of BANK15 and BANK16 is powered by the LDO, and can be changed by replacing the LDO chip.  $V_{MGTAVCC}$  is the supply voltage of the FPGA internal GTP transceiver, connected to 1.0V;  $V_{MGTAVTT}$  is the termination voltage of the GTP transceiver, connected to 1.2V.

The Artix-7 FPGA system requires that the power-up sequence be power by  $V_{CCINT}$ , then  $V_{CCBRAM}$ , then  $V_{CCAUX}$ , and finally  $V_{CCO}$ . If  $V_{CCINT}$  and  $V_{CCBRAM}$  have the same voltage, they can be powered up at the same time. The order of power outages is reversed. The power-up sequence of the GTP transceiver is  $V_{CCINT}$ , then  $V_{MGTAVCC}$ , then  $V_{MGTAVTT}$ . If  $V_{CCINT}$  and  $V_{MGTAVCC}$  have the same voltage, they can be powered up at the same time. The power-off sequence is just the opposite of the power-on sequence.

## Part 2.3: Active Differential Crystal

The AC7A200 core board is equipped with two Sitime active differential crystals, one is 200MHz, the model is SiT9102-200.00MHz, the system main clock for FPGA and used to generate DDR3 control clock; the other is 125MHz,



model is SiT9102 -125MHz, reference clock input for GTP transceivers.

**Part 2.3.1: 200Mhz Active Differential clock**

G1 in Figure 2-3-1 is the 200M active differential crystal that provides the development board system clock source. The crystal output is connected to the BANK34 global clock pin MRCC (R4 and T4) of the FPGA. This 200Mhz differential clock can be used to drive the user logic in the FPGA. Users can configure the PLLs and DCMs inside the FPGA to generate clocks of different frequencies.

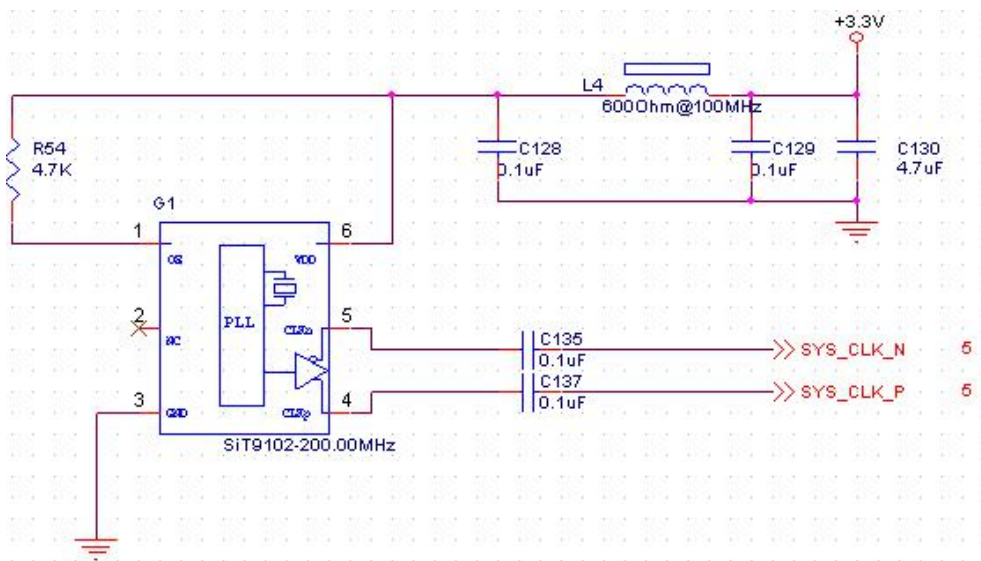


Figure 2-3-1: 200Mhz Active Differential Crystal Schematic



Figure 2-3-2: 200Mhz Active Differential Crystal on the Core Board

**200Mhz Differential Clock Pin Assignment**

Signal Name	FPGA PIN
SYS_CLK_P	R4
SYS_CLK_N	T4

### Part 2.3.2: 125MHz Active Differential Crystal

G2 in Figure 2-3-3 is the 125MHz active differential crystal, which is the reference input clock provided to the GTP module inside the FPGA. The crystal output is connected to the GTP BANK216 clock pins MGTREFCLK0P (F6) and MGTREFCLK0N (E6) of the FPGA.

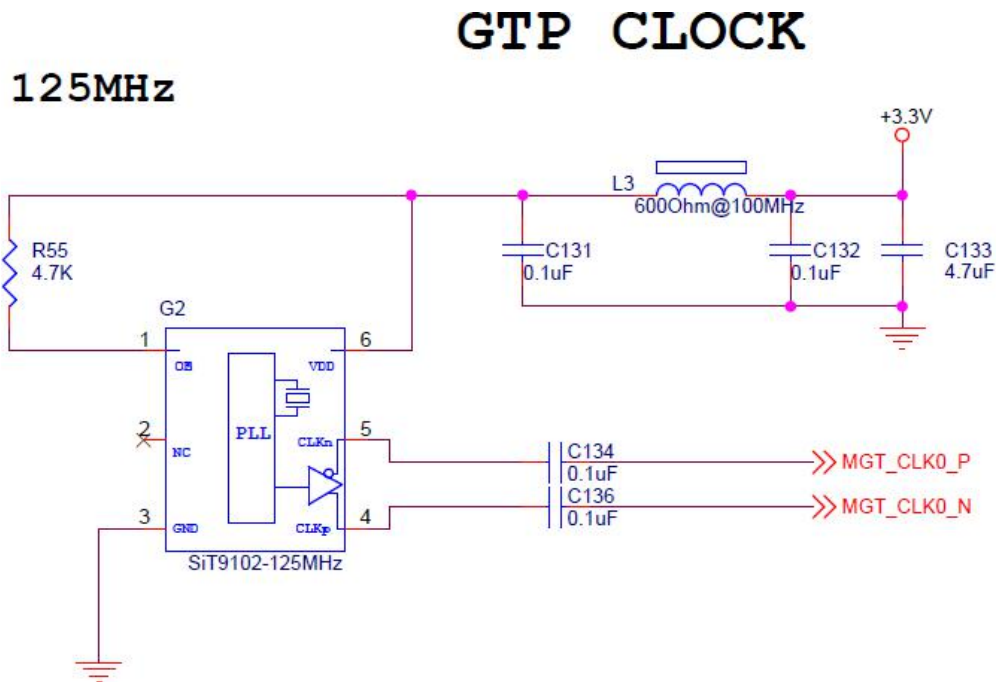


Figure 2-3-3: 125MHz Active Differential Crystal Schematic

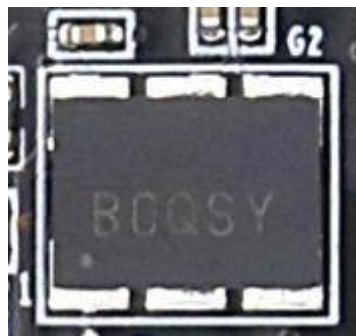


Figure 2-3-4: 125MHz Active Differential Crystal on the Core Board

### 125MHz Differential Clock Pin Assignment

Net Name	FPGA PIN
MGT_CLK0_P	F6
MGT_CLK0_N	E6

## Part 2.4: DDR3 DRAM

The FPGA core board AC7A200 is equipped with two Micron 4Gbit (512MB) DDR3 chips (8Gbit in totally), model is MT41J256M16HA-125 (compatible with MT41K256M16HA-125). The DDR3 SDRAM has a maximum operating speed of 400MHz (data rate 800Mbps). The DDR3 memory system is directly connected to the memory interface of the BANK 34 and BANK35 of the FPGA. The specific configuration of DDR3 SDRAM is shown in Table 2-4-1.

Bit Number	Chip Model	Capacity	Factory
U5,U6	MT41J256M16HA-125	256M x 16bit	Micron

Table 2-4-1: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3. Figure 2-4-1 details the hardware connection of DDR3 DRAM

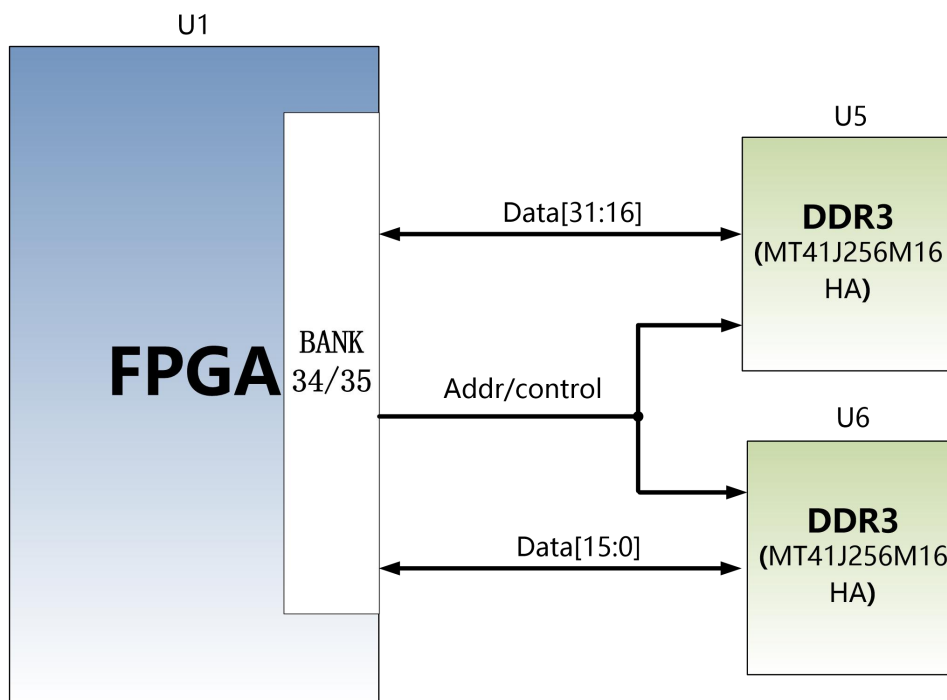


Figure 2-4-1: The DDR3 DRAM Schematic



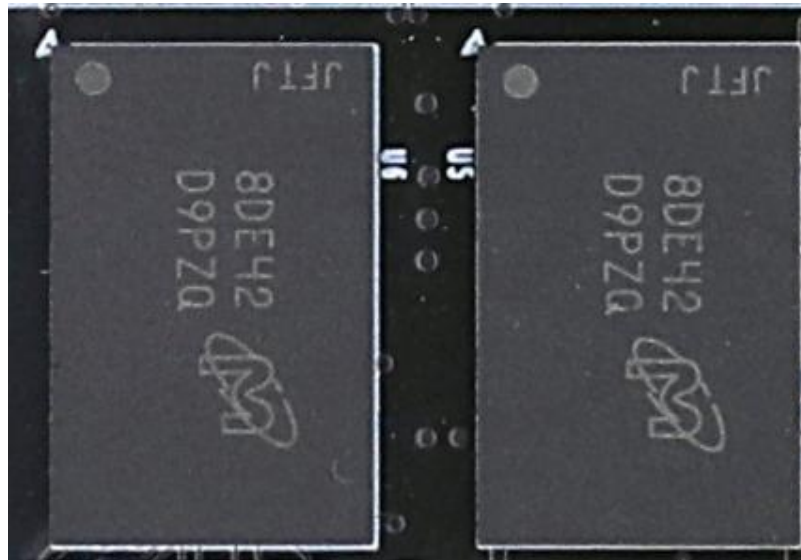


Figure 2-4-2: The DDR3 on the Core Board

**DDR3 DRAM pin assignment:**

Net Name	FPGA PIN Name	FPGA P/N
DDR3_DQS0_P	IO_L3P_T0_DQS_AD5P_35	E1
DDR3_DQS0_N	IO_L3N_T0_DQS_AD5N_35	D1
DDR3_DQS1_P	IO_L9P_T1_DQS_AD7P_35	K2
DDR3_DQS1_N	IO_L9N_T1_DQS_AD7N_35	J2
DDR3_DQS2_P	IO_L15P_T2_DQS_35	M1
DDR3_DQS2_N	IO_L15N_T2_DQS_35	L1
DDR3_DQS3_P	IO_L21P_T3_DQS_35	P5
DDR3_DQS3_N	IO_L21N_T3_DQS_35	P4
DDR3_DQ[0]	IO_L2P_T0_AD12P_35	C2
DDR3_DQ [1]	IO_L5P_T0_AD13P_35	G1
DDR3_DQ [2]	IO_L1N_T0_AD4N_35	A1
DDR3_DQ [3]	IO_L6P_T0_35	F3
DDR3_DQ [4]	IO_L2N_T0_AD12N_35	B2
DDR3_DQ [5]	IO_L5N_T0_AD13N_35	F1
DDR3_DQ [6]	IO_L1P_T0_AD4P_35	B1
DDR3_DQ [7]	IO_L4P_T0_35	E2
DDR3_DQ [8]	IO_L11P_T1_SRCC_35	H3
DDR3_DQ [9]	IO_L11N_T1_SRCC_35	G3
DDR3_DQ [10]	IO_L8P_T1_AD14P_35	H2
DDR3_DQ [11]	IO_L10N_T1_AD15N_35	H5

DDR3_DQ [12]	IO_L7N_T1_AD6N_35	J1
DDR3_DQ [13]	IO_L10P_T1_AD15P_35	J5
DDR3_DQ [14]	IO_L7P_T1_AD6P_35	K1
DDR3_DQ [15]	IO_L12P_T1_MRCC_35	H4
DDR3_DQ [16]	IO_L18N_T2_35	L4
DDR3_DQ [17]	IO_L16P_T2_35	M3
DDR3_DQ [18]	IO_L14P_T2_SRCC_35	L3
DDR3_DQ [19]	IO_L17N_T2_35	J6
DDR3_DQ [20]	IO_L14N_T2_SRCC_35	K3
DDR3_DQ [21]	IO_L17P_T2_35	K6
DDR3_DQ [22]	IO_L13N_T2_MRCC_35	J4
DDR3_DQ [23]	IO_L18P_T2_35	L5
DDR3_DQ [24]	IO_L20N_T3_35	P1
DDR3_DQ [25]	IO_L19P_T3_35	N4
DDR3_DQ [26]	IO_L20P_T3_35	R1
DDR3_DQ [27]	IO_L22N_T3_35	N2
DDR3_DQ [28]	IO_L23P_T3_35	M6
DDR3_DQ [29]	IO_L24N_T3_35	N5
DDR3_DQ [30]	IO_L24P_T3_35	P6
DDR3_DQ [31]	IO_L22P_T3_35	P2
DDR3_DM0	IO_L4N_T0_35	D2
DDR3_DM1	IO_L8N_T1_AD14N_35	G2
DDR3_DM2	IO_L16N_T2_35	M2
DDR3_DM3	IO_L23N_T3_35	M5
DDR3_A[0]	IO_L11N_T1_SRCC_34	AA4
DDR3_A[1]	IO_L8N_T1_34	AB2
DDR3_A[2]	IO_L10P_T1_34	AA5
DDR3_A[3]	IO_L10N_T1_34	AB5
DDR3_A[4]	IO_L7N_T1_34	AB1
DDR3_A[5]	IO_L6P_T0_34	U3
DDR3_A[6]	IO_L5P_T0_34	W1
DDR3_A[7]	IO_L1P_T0_34	T1
DDR3_A[8]	IO_L2N_T0_34	V2
DDR3_A[9]	IO_L2P_T0_34	U2
DDR3_A[10]	IO_L5N_T0_34	Y1
DDR3_A[11]	IO_L4P_T0_34	W2

DDR3_A[12]	IO_L4N_T0_34	Y2
DDR3_A[13]	IO_L1N_T0_34	U1
DDR3_A[14]	IO_L6N_T0_VREF_34	V3
DDR3_BA[0]	IO_L9N_T1_DQS_34	AA3
DDR3_BA[1]	IO_L9P_T1_DQS_34	Y3
DDR3_BA[2]	IO_L11P_T1_SRCC_34	Y4
DDR3_S0	IO_L8P_T1_34	AB3
DDR3_RAS	IO_L12P_T1_MRCC_34	V4
DDR3_CAS	IO_L12N_T1_MRCC_34	W4
DDR3_WE	IO_L7P_T1_34	AA1
DDR3_ODT	IO_L14N_T2_SRCC_34	U5
DDR3_RESET	IO_L15P_T2_DQS_34	W6
DDR3_CLK_P	IO_L3P_T0_DQS_34	R3
DDR3_CLK_N	IO_L3N_T0_DQS_34	R2
DDR3_CKE	IO_L14P_T2_SRCC_34	T5

## Part 2.5: QSPI Flash

The FPGA core board AC7A200 is equipped with one 128Mbit QSPI FLASH, and the model is N25Q128, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, soft core application code and other user data files. The specific models and related parameters of SPI FLASH are shown in Table 2-5-1.

Position	Model	Capacity	Factory
U8	N25Q128	128M Bit	Numonyx

Table 2-5-1: QSPI FLASH Specification

QSPI FLASH is connected to the dedicated pins of BANK0 and BANK14 of the FPGA chip. The clock pin is connected to CCLK0 of BANK0, and other data and chip select signals are connected to D00~D03 and FCS pins of BANK14 respectively. Figure 2-5-1 shows the hardware connection of QSPI Flash.

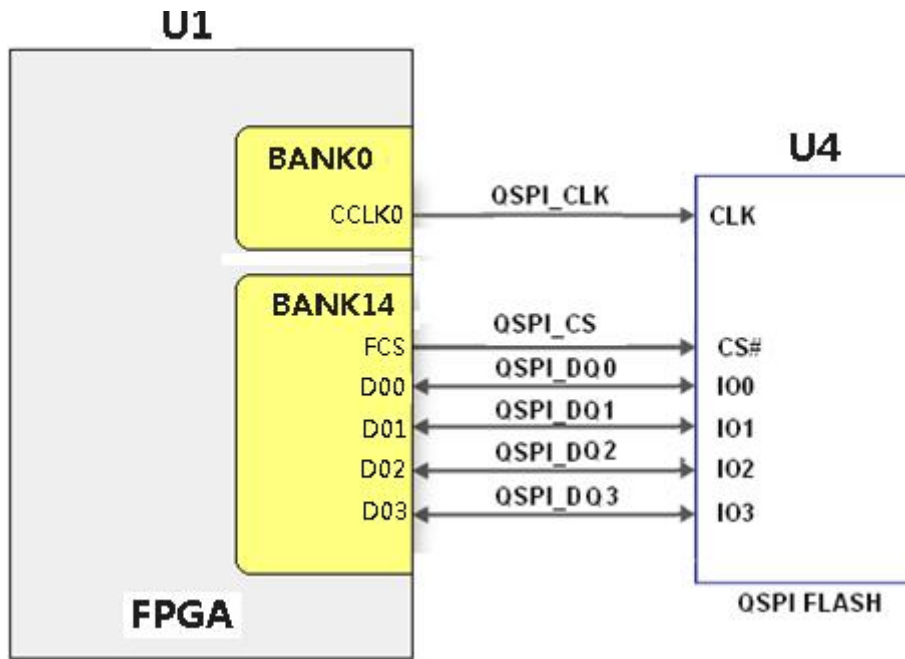


Figure 2-5-1: QSPI Flash Schematic

**QSPI Flash pin assignments:**

Net Name	FPGA PIN Name	FPGA P/N
QSPI_CLK	CCLK_0	L12
QSPI_CS	IO_L6P_T0_FCS_B_14	T19
QSPI_DQ0	IO_L1P_T0_D00_MOSI_14	P22
QSPI_DQ1	IO_L1N_T0_D01_DIN_14	R22
QSPI_DQ2	IO_L2P_T0_D02_14	P21
QSPI_DQ3	IO_L2N_T0_D03_14	R21

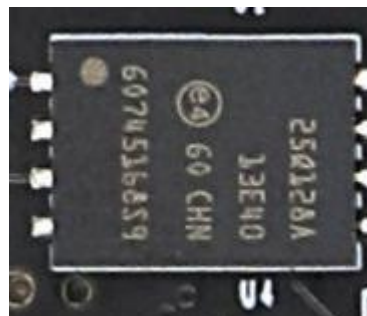


Figure 2-5-1: QSPI FLASH on the Core Board

## Part 2.6: LED Light on Core Board

There are 3 red LED lights on the AC7A200 FPGA core board, one of which is the power indicator light (PWR), one is the configuration LED light (DONE), and one is the user LED light. When the core board is powered, the power indicator will illuminate; when the FPGA is configured, the configuration LED will illuminate. The user LED light is connected to the IO of the BANK34, the user can control the light on and off by the program. When the IO voltage connected to the user LED is high, the user LED is illuminate. When the connection IO voltage is low, the user LED will be extinguished. The schematic diagram of the LED light hardware connection is shown in Figure 2-6-1:

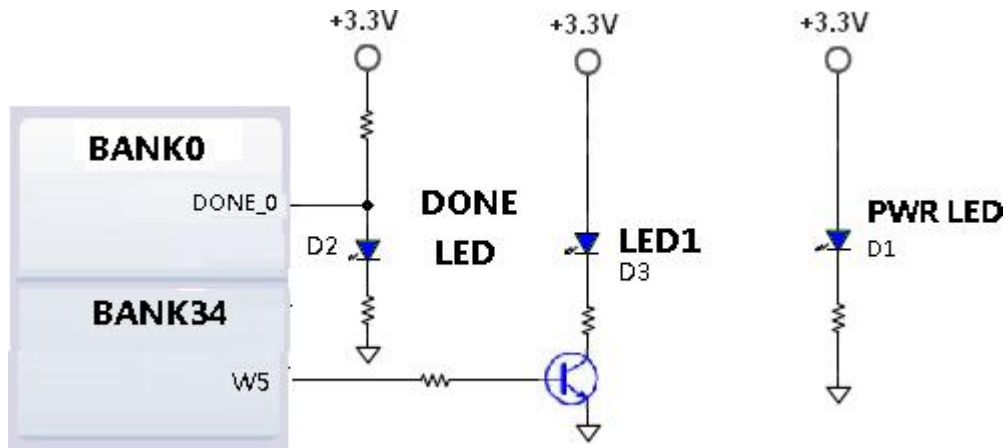


Figure 2-6-1: LED lights on the Core Board Schematic

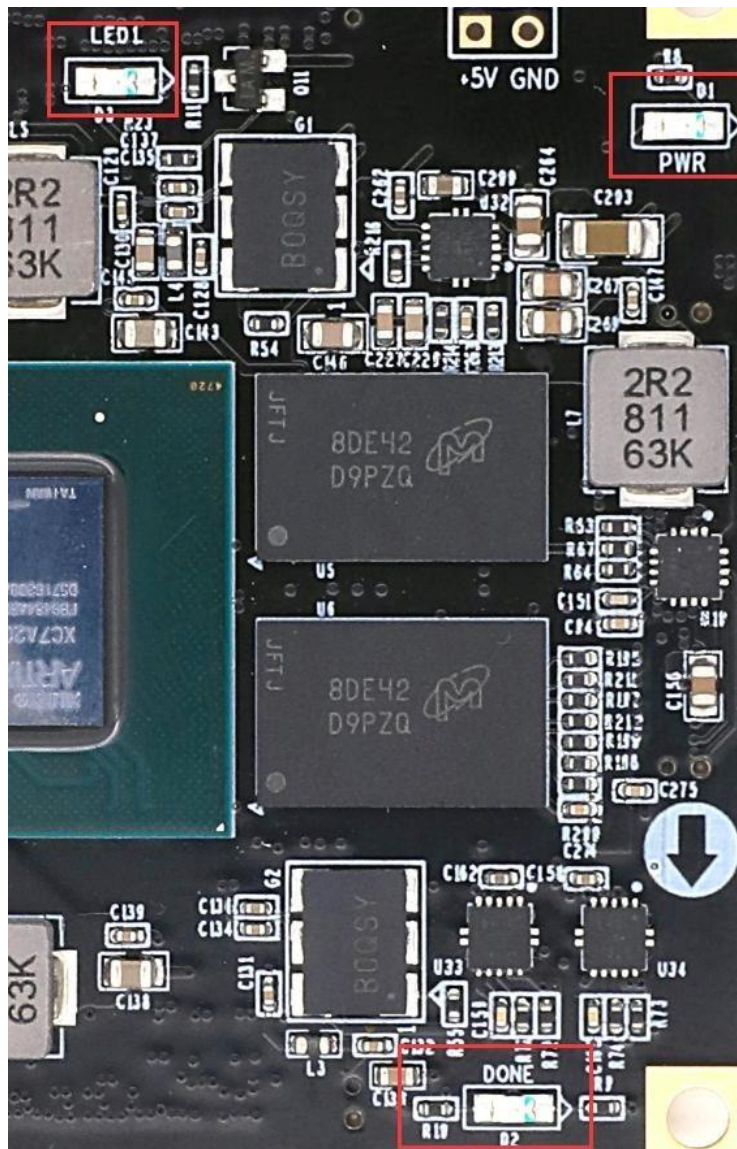


Figure 2-6-2: LED lights on the Core Board

### User LEDs Pin Assignment

Signal Name	FPGA Pin Name	FPGA Pin Number	Description
LED1	IO_L15N_T2_DQS_34	W5	User LED

## Part 2.7: JTAG Interface

The JTAG test socket J1 is reserved on the AC7A200 core board for JTAG download and debugging when the core board is used alone. Figure 2-7-1 is the schematic part of the JTAG port, which involves TMS, TDI, TDO, TCK. ,



GND, +3.3V these six signals.

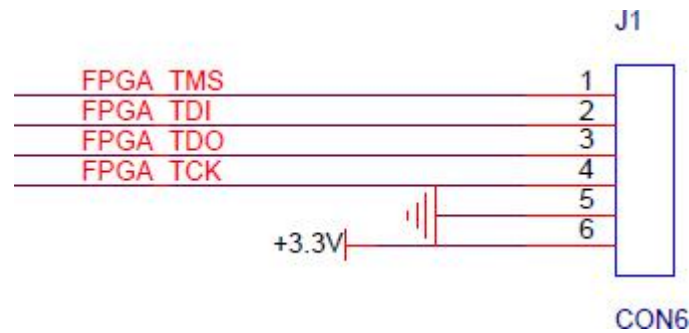


Figure 2-7-1: JTAG Interface Schematic

The JTAG interface J1 on AC7A200 FPGA core board uses a 6-pin 2.54mm pitch single-row test hole. If you need to use the JTAG connector to debug on the core board, you need to solder a 6-pin single-row pin header. Figure 2-7-2 shows the JTAG interface J1 on the AC7A200 FPGA core board.

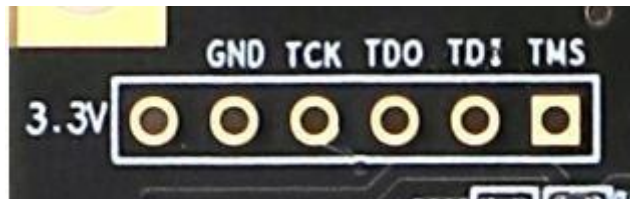


Figure 2-7-2 JTAG Interface on Core Board

## Part 2.8: Power Interface on the Core Board

In order to make the AC7A200 FPGA core board work alone, the core board is reserved 2-pin power supply interface J2. If the user wants to debug the function of the core board separately (without the carrier board), the external device needs to provide +5V to supply power to the core board.

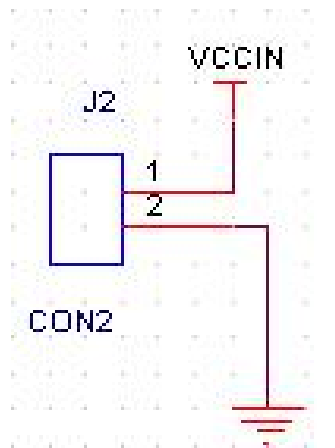


Figure 2-8-1: Power Interface schematic on the Core Board

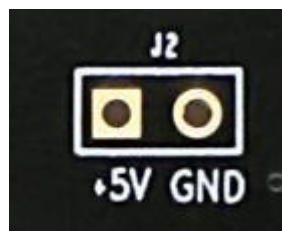


Figure 2-8-2: Power interface on the Core Board

## Part 2.9: Board to Board Connectors pin assignment

The core board has a total of four high-speed board to board connectors. The core board uses four 80-pin inter-board connectors to connect to the carrier board. The IO port of the FPGA is connected to the four connectors by differential routing. The pin spacing of the connectors is 0.5mm, insert to the board to board connectors on the carrier board for high-speed data communication.

### Board to Board Connectors CON1

The 80-pin board to board connectors CON1, which are used to connect with the VCCIN power supply (+5V) and ground on the carrier board, extend the normal IOs of the FPGA. It should be noted here that 15 pins of CON1 are connected to the IO port of BANK34, because the BANK34 connection is connected to DDR3. Therefore, the voltage standard of all IOs of this BANK34 is 1.5V.



**Pin Assignment of Board to Board Connectors CON1**

CON1 PIN	Net Name	FPGA PIN	Voltage Level	CON1 PIN	Net Name	FPGA PIN	Voltage Level
PIN1	VCCIN	-	+5V	PIN2	VCCIN	-	+5V
PIN3	VCCIN	-	+5V	PIN4	VCCIN	-	+5V
PIN5	VCCIN	-	+5V	PIN6	VCCIN	-	+5V
PIN7	VCCIN	-	+5V	PIN8	VCCIN	-	+5V
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	NC	-	NC	PIN12	NC	-	NC
PIN13	NC	-	NC	PIN14	NC	-	NC
PIN15	NC	-	NC	PIN16	B13_L4_P	AA15	3.3V
PIN17	NC	-	NC	PIN18	B13_L4_N	AB15	3.3V
PIN19	GND	-	Ground	PIN20	GND	-	Ground
PIN21	B13_L5_P	Y13	3.3V	PIN22	B13_L1_P	Y16	3.3V
PIN23	B13_L5_N	AA14	3.3V	PIN24	B13_L1_N	AA16	3.3V
PIN25	B13_L7_P	AB11	3.3V	PIN26	B13_L2_P	AB16	3.3V
PIN27	B13_L7_P	AB12	3.3V	PIN28	B13_L2_N	AB17	3.3V
PIN29	GND	-	Ground	PIN30	GND	-	Ground
PIN31	B13_L3_P	AA13	3.3V	PIN32	B13_L6_P	W14	3.3V
PIN33	B13_L3_N	AB13	3.3V	PIN34	B13_L6_N	Y14	3.3V
PIN35	B34_L23_P	Y8	1.5V	PIN36	B34_L20_P	AB7	1.5V
PIN37	B34_L23_N	Y7	1.5V	PIN38	B34_L20_N	AB6	1.5V
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B34_L18_N	AA6	1.5V	PIN42	B34_L21_N	V8	1.5V
PIN43	B34_L18_P	Y6	1.5V	PIN44	B34_L21_P	V9	1.5V
PIN45	B34_L19_P	V7	1.5V	PIN46	B34_L22_P	AA8	1.5V
PIN47	B34_L19_N	W7	1.5V	PIN48	B34_L22_N	AB8	1.5V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	XADC_VN	M9	Analog	PIN52	NC		
PIN53	XADC_VP	L10	Analog	PIN54	B34_L25	U7	1.5V
PIN55	NC	-	NC	PIN56	B34_L24_P	W9	1.5V
PIN57	NC	-	NC	PIN58	B34_L24_N	Y9	1.5V
PIN59	GND	-	Ground	PIN60	GND	-	Ground

PIN61	B16_L1_N	F14	3.3V	PIN62	NC	-	NC
PIN63	B16_L1_P	F13	3.3V	PIN64	NC	-	NC
PIN65	B16_L4_N	E14	3.3V	PIN66	NC	-	NC
PIN67	B16_L4_P	E13	3.3V	PIN68	NC	-	NC
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B16_L6_N	D15	3.3V	PIN72	NC	-	NC
PIN73	B16_L6_P	D14	3.3V	PIN74	NC	-	NC
PIN75	B16_L8_P	C13	3.3V	PIN76	NC	-	NC
PIN77	B16_L8_N	B13	3.3V	PIN78	NC	-	NC
PIN79	NC	-	NC	PIN80	NC	-	NC



Figure 2-9-1: Board to Board Connectors CON1 on the Core Board

### Board to Board Connectors CON2

The 80-pin female connection header CON2 is used to extend the normal IO of the BANK13 and BANK14 of the FPGA. The voltage standards of both BANKs are 3.3V.

### Pin Assignment of Board to Board Connectors CON2

CON2 PIN	Net Name	FPGA PIN	Voltage Level	CON2 PIN	Net Name	FPGA PIN	Voltage Level
PIN1	B13_L16_P	W15	3.3V	PIN2	B14_L16_P	V17	3.3V
PIN3	B13_L16_N	W16	3.3V	PIN4	B14_L16_N	W17	3.3V
PIN5	B13_L15_P	T14	3.3V	PIN6	B13_L14_P	U15	3.3V
PIN7	B13_L15_N	T15	3.3V	PIN8	B13_L14_N	V15	3.3V
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	B13_L13_P	V13	3.3V	PIN12	B14_L10_P	AB21	3.3V
PIN13	B13_L13_N	V14	3.3V	PIN14	B14_L10_N	AB22	3.3V

PIN15	B13_L12_P	W11	3.3V	PIN16	B14_L8_N	AA21	3.3V
PIN17	B13_L12_N	W12	3.3V	PIN18	B14_L8_P	AA20	3.3V
PIN19	GND	-	Ground	PIN20	GND	-	Ground
PIN21	B13_L11_P	Y11	3.3V	PIN22	B14_L15_N	AB20	3.3V
PIN23	B13_L11_N	Y12	3.3V	PIN24	B14_L15_P	AA19	3.3V
PIN25	B13_L10_P	V10	3.3V	PIN26	B14_L17_P	AA18	3.3V
PIN27	B13_L10_N	W10	3.3V	PIN28	B14_L17_N	AB18	3.3V
PIN29	GND	-	Ground	PIN30	GND	-	Ground
PIN31	B13_L9_N	AA11	3.3V	PIN32	B14_L6_N	T20	3.3V
PIN33	B13_L9_P	AA10	3.3V	PIN34	B13_IO0	Y17	3.3V
PIN35	B13_L8_N	AB10	3.3V	PIN36	B14_L7_N	W22	3.3V
PIN37	B13_L8_P	AA9	3.3V	PIN38	B14_L7_P	W21	3.3V
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B14_L11_N	V20	3.3V	PIN42	B14_L4_P	T21	3.3V
PIN43	B14_L11_P	U20	3.3V	PIN44	B14_L4_N	U21	3.3V
PIN45	B14_L14_N	V19	3.3V	PIN46	B14_L9_P	Y21	3.3V
PIN47	B14_L14_P	V18	3.3V	PIN48	B14_L9_N	Y22	3.3V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	B14_L5_N	R19	3.3V	PIN52	B14_L12_N	W20	3.3V
PIN53	B14_L5_P	P19	3.3V	PIN54	B14_L12_P	W19	3.3V
PIN55	B14_L18_N	U18	3.3V	PIN56	B14_L13_N	Y19	3.3V
PIN57	B14_L18_P	U17	3.3V	PIN58	B14_L13_P	Y18	3.3V
PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B13_L17_P	T16	3.3V	PIN62	B14_L3_N	V22	3.3V
PIN63	B13_L17_N	U16	3.3V	PIN64	B14_L3_P	U22	3.3V
PIN65	B14_L21_N	P17	3.3V	PIN66	B14_L20_N	T18	3.3V
PIN67	B14_L21_P	N17	3.3V	PIN68	B14_L20_P	R18	3.3V
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B14_L22_P	P15	3.3V	PIN72	B14_L19_N	R14	3.3V
PIN73	B14_L22_N	R16	3.3V	PIN74	B14_L19_P	P14	3.3V
PIN75	B14_L24_N	R17	3.3V	PIN76	B14_L23_P	N13	3.3V
PIN77	B14_L24_P	P16	3.3V	PIN78	B14_L23_N	N14	3.3V
PIN79	B14_IO0	P20	3.3V	PIN80	B14_IO25	N15	3.3V



Figure 2-9-2: Board to Board Connectors CON2 on the Core Board

### Board to Board Connectors CON3

The 80-pin connector CON3 is used to extend the normal IO of the BANK15 and BANK16 of the FPGA. In addition, four JTAG signals are also connected to the carrier board via the CON3 connector. The voltage standards of BANK15 and BANK16 can be adjusted by an LDO chip. The default installed LDO is 3.3V. If you want to output other standard levels, you can replace it with a suitable LDO.

### Pin Assignment of Board to Board Connectors CON3

CON3 PIN	Net Name	FPGA PIN	Voltage Level	CON3 PIN	Net Name	FPGA PIN	Voltage Level
PIN1	B15_IO0	J16	3.3V	PIN2	B15_IO25	M17	3.3V
PIN3	B16_IO0	F15	3.3V	PIN4	B16_IO25	F21	3.3V
PIN5	B15_L4_P	G17	3.3V	PIN6	B16_L21_N	A21	3.3V
PIN7	B15_L4_N	G18	3.3V	PIN8	B16_L21_P	B21	3.3V
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	B15_L2_P	G15	3.3V	PIN12	B16_L23_P	E21	3.3V
PIN13	B15_L2_N	G16	3.3V	PIN14	B16_L23_N	D21	3.3V
PIN15	B15_L12_P	J19	3.3V	PIN16	B16_L22_P	E22	3.3V
PIN17	B15_L12_N	H19	3.3V	PIN18	B16_L22_N	D22	3.3V
PIN19	GND	-	Ground	PIN20	GND	-	Ground
PIN21	B15_L11_P	J20	3.3V	PIN22	B16_L24_P	G21	3.3V
PIN23	B15_L11_N	J21	3.3V	PIN24	B16_L24_N	G22	3.3V
PIN25	B15_L1_N	G13	3.3V	PIN26	B15_L8_N	G20	3.3V
PIN27	B15_L1_P	H13	3.3V	PIN28	B15_L8_P	H20	3.3V
PIN29	GND	-	Ground	PIN30	GND	-	Ground
PIN31	B15_L5_P	J15	3.3V	PIN32	B15_L7_N	H22	3.3V

PIN33	B15_L5_N	H15	3.3V	PIN34	B15_L7_P	J22	3.3V
PIN35	B15_L3_N	H14	3.3V	PIN36	B15_L9_P	K21	3.3V
PIN37	B15_L3_P	J14	3.3V	PIN38	B15_L9_N	K22	3.3V
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B15_L19_P	K13	3.3V	PIN42	B15_L15_N	M22	3.3V
PIN43	B15_L19_N	K14	3.3V	PIN44	B15_L15_P	N22	3.3V
PIN45	B15_L20_P	M13	3.3V	PIN46	B15_L6_N	H18	3.3V
PIN47	B15_L20_N	L13	3.3V	PIN48	B15_L6_P	H17	3.3V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	B15_L14_P	L19	3.3V	PIN52	B15_L13_N	K19	3.3V
PIN53	B15_L14_N	L20	3.3V	PIN54	B15_L13_P	K18	3.3V
PIN55	B15_L21_P	K17	3.3V	PIN56	B15_L10_P	M21	3.3V
PIN57	B15_L21_N	J17	3.3V	PIN58	B15_L10_N	L21	3.3V
PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B15_L23_P	L16	3.3V	PIN62	B15_L18_P	N20	3.3V
PIN63	B15_L23_N	K16	3.3V	PIN64	B15_L18_N	M20	3.3V
PIN65	B15_L22_P	L14	3.3V	PIN66	B15_L17_N	N19	3.3V
PIN67	B15_L22_N	L15	3.3V	PIN68	B15_L17_P	N18	3.3V
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B15_L24_P	M15	3.3V	PIN72	B15_L16_P	M18	3.3V
PIN73	B15_L24_N	M16	3.3V	PIN74	B15_L16_N	L18	3.3V
PIN75	NC	-		PIN76	NC	-	
PIN77	FPGA_TCK	V12	3.3V	PIN78	FPGA_TDI	R13	3.3V
PIN79	FPGA_TDO	U13	3.3V	PIN80	FPGA_TMS	T13	3.3V

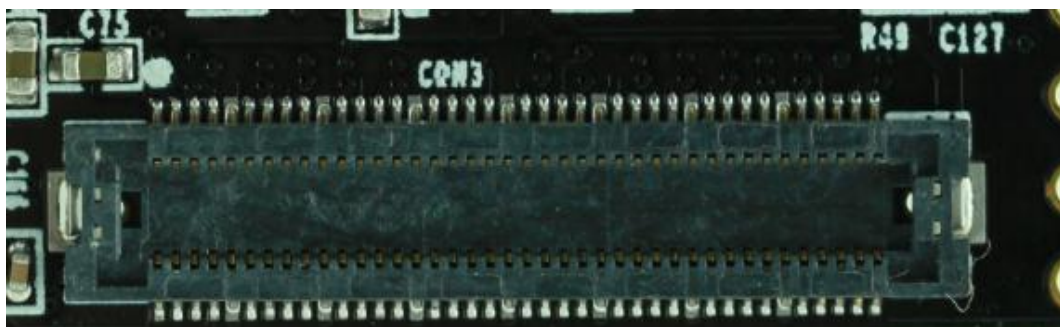


Figure 2-9-3: Board to Board Connectors CON3 on the Core Board

## Board to Board Connectors CON4

The 80-Pin connector CON4 is used to extend the normal IO and GTP high-speed data and clock signals of the FPGA BANK16. The voltage standard of the IO port of BANK16 can be adjusted by an LDO chip. The default installed LDO is 3.3V. If the user wants to output other standard levels, it can be replaced by a suitable LDO. The high-speed data and clock signals of the GTP are strictly differentially routed on the core board. The data lines are equal in length and kept at a certain interval to prevent signal interference.

### Pin Assignment of Board to Board Connectors CON4

CON4 PIN	Net Name	FPGA PIN	Voltage Level	CON4 PIN	Net Name	FPGA PIN	Voltage Level
PIN1	NC	-	-	PIN2		-	-
PIN3	NC	-	-	PIN4		-	-
PIN5	NC	-	-	PIN6		-	-
PIN7	NC	-	-	PIN8		-	-
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	NC	-	-	PIN12	MGT_TX2_P	B6	Diff
PIN13	NC	-	-	PIN14	MGT_TX2_N	A6	Diff
PIN15	GND	-	Ground	PIN16	GND	-	Ground
PIN17	MGT_TX3_P	D7	Diff	PIN18	MGT_RX2_P	B10	Diff
PIN19	MGT_TX3_N	C7	Diff	PIN20	MGT_RX2_N	A10	Diff
PIN21	GND	-	Ground	PIN22	GND	-	Ground
PIN23	MGT_RX3_P	D9	Diff	PIN24	MGT_TX0_P	B4	Diff
PIN25	MGT_RX3_N	C9	Diff	PIN26	MGT_TX0_N	A4	Diff
PIN27	GND	-	Ground	PIN28	GND	-	Ground
PIN29	MGT_TX1_P	D5	Diff	PIN30	MGT_RX0_P	B8	Diff
PIN31	MGT_TX1_N	C5	Diff	PIN32	MGT_RX0_N	A8	Diff
PIN33	GND	-	Ground	PIN34	GND	-	Ground
PIN35	MGT_RX1_P	D11	Diff	PIN36	MGT_CLK1_P	F10	Diff
PIN37	MGT_RX1_N	C11	Diff	PIN38	MGT_CLK1_N	E10	Diff
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B16_L5_P	E16	3.3V	PIN42	B16_L2_P	F16	3.3V

PIN43	B16_L5_N	D16	3.3V	PIN44	B16_L2_N	E17	3.3V
PIN45	B16_L7_P	B15	3.3V	PIN46	B16_L3_P	C14	3.3V
PIN47	B16_L7_N	B16	3.3V	PIN48	B16_L3_N	C15	3.3V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	B16_L9_P	A15	3.3V	PIN52	B16_L10_P	A13	3.3V
PIN53	B16_L9_N	A16	3.3V	PIN54	B16_L10_N	A14	3.3V
PIN55	B16_L11_P	B17	3.3V	PIN56	B16_L12_P	D17	3.3V
PIN57	B16_L11_N	B18	3.3V	PIN58	B16_L12_N	C17	3.3V
PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B16_L13_P	C18	3.3V	PIN62	B16_L14_P	E19	3.3V
PIN63	B16_L13_N	C19	3.3V	PIN64	B16_L14_N	D19	3.3V
PIN65	B16_L15_P	F18	3.3V	PIN66	B16_L16_P	B20	3.3V
PIN67	B16_L15_N	E18	3.3V	PIN68	B16_L16_N	A20	3.3V
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B16_L17_P	A18	3.3V	PIN72	B16_L18_P	F19	3.3V
PIN73	B16_L17_N	A19	3.3V	PIN74	B16_L18_N	F20	3.3V
PIN75	B16_L19_P	D20	3.3V	PIN76	B16_L20_P	C22	3.3V
PIN77	B16_L19_N	C20	3.3V	PIN78	B16_L20_N	B22	3.3V
PIN79	NC	-		PIN80	NC	-	



Figure 2-9-4: Board to Board Connectors CON4 on the Core Board

## Part 2.10: Power Supply

The AC7A200 FPGA core board is powered by DC5V via carrier board, and it is powered by the Mini USB interface when it is used alone. **Please be careful not to supply power by the Mini USB and the carrier board at the same time to avoid damage.** The power supply design diagram on the board is shown in Figure 2-10-1.



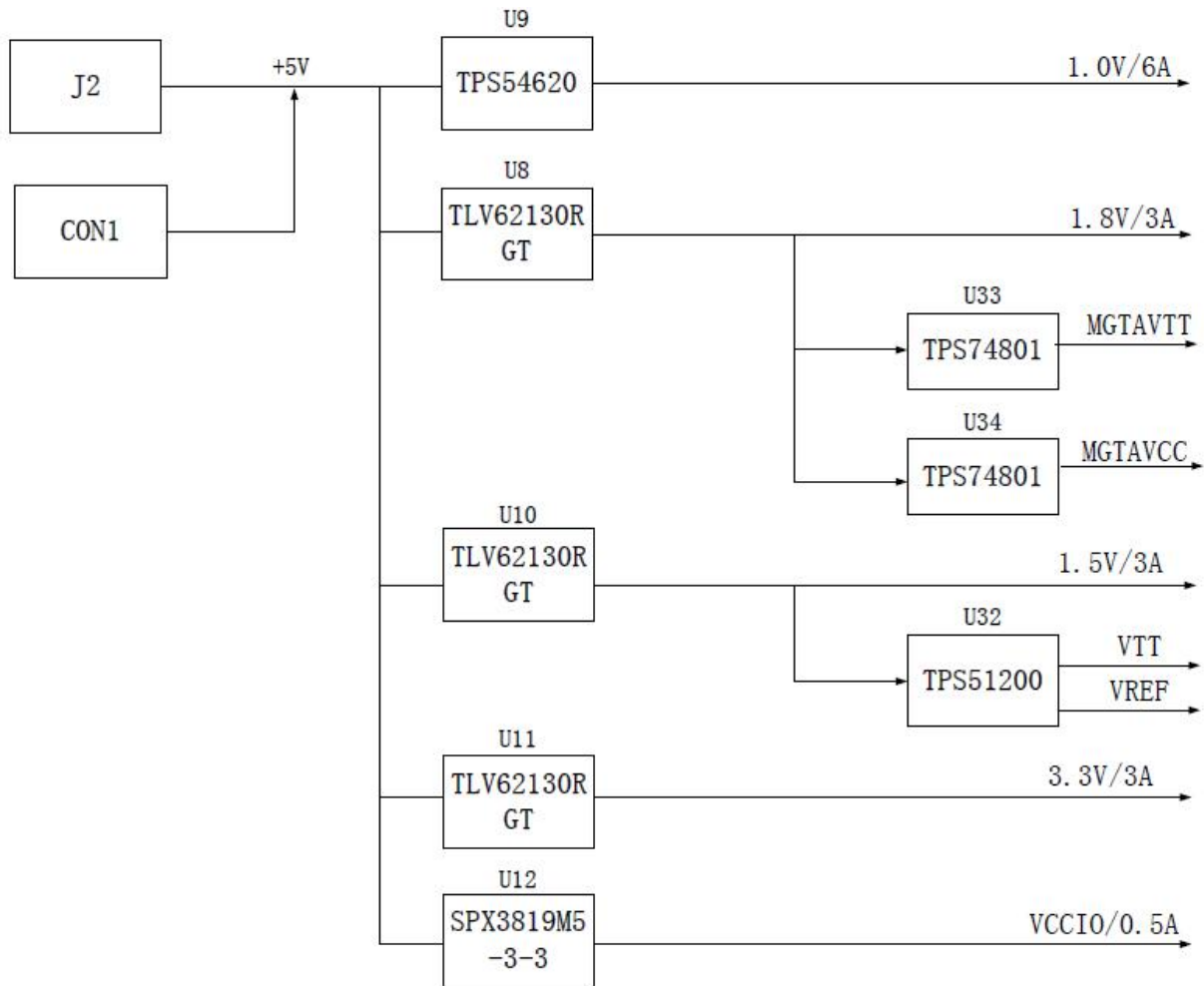


Figure 2-10-1: Power Supply on core board schematic

The core board is powered by +5V and converted to +3.3V, +1.5V, +1.8V, +1.0V four-way power supply through three DC/DC power supply chip TLV62130RGT. The current of +1.0V can be up to 6A, and the other three output currents can be up to 3A. The VCCIO is generated by one LDOSPX3819M5-3-3. VCCIO mainly supplies power to BANK15 and BANK16 of FPGA. Users can change the IO of BANK15,16 to different voltage standards by replacing their LDO chip. The 1.5V generates the VTT and VREF voltages required by DDR3 via TI's TPS51200. The 1.8V power supply of MGTAVTT and MGTAVCC for the GTP transceiver is generated by TI's TPS74801 chip. The functions of each power distribution are shown in the following table:



Power Supply	Function
+1.0V	FPGA Core Voltage
+1.8V	FPGA auxiliary voltage, TPS74801 power supply
+3.3V	VCCIO of Bank0,Bank13 and Bank14 of FPGA,QSIP FLASH, Clock Crystal
+1.5V	DDR3, Bank34 and Bank35 of FPGA
VREF,VTT(+0.75V)	DDR3
CCIP(+3.3V)	FPGA Bank15, Bank16
MGTAVTT(+1.2V)	GTP Transceiver Bank216 of FPGA
MGTAVCC(+1.0V)	GTP Transceiver Bank216 of FPGA

Because the power supply of Artix-7 FPGA has the power-on sequence requirement, in the circuit design, we have designed according to the power requirements of the chip, and the power-on is 1.0V->1.8V->(1.5 V, 3.3V, VCCIO) and 1.0V-> MGTAVCC -> MGTAVTT, the circuit design to ensure the normal operation of the chip.

The power circuit on the AC7A200 FPGA core board is shown in Figure 2-10-2:

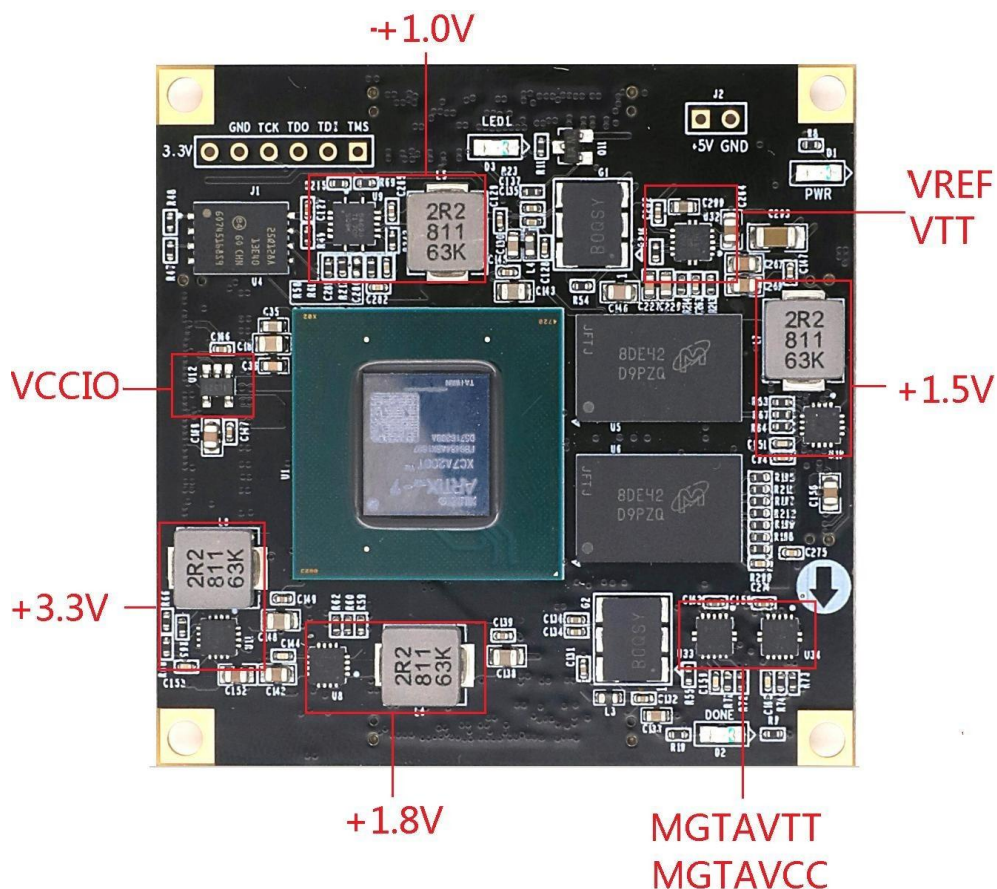


Figure 2-10-2: Power Supply on the AC7A200 FPGA Core Board

## Part 2.11: Size Dimension

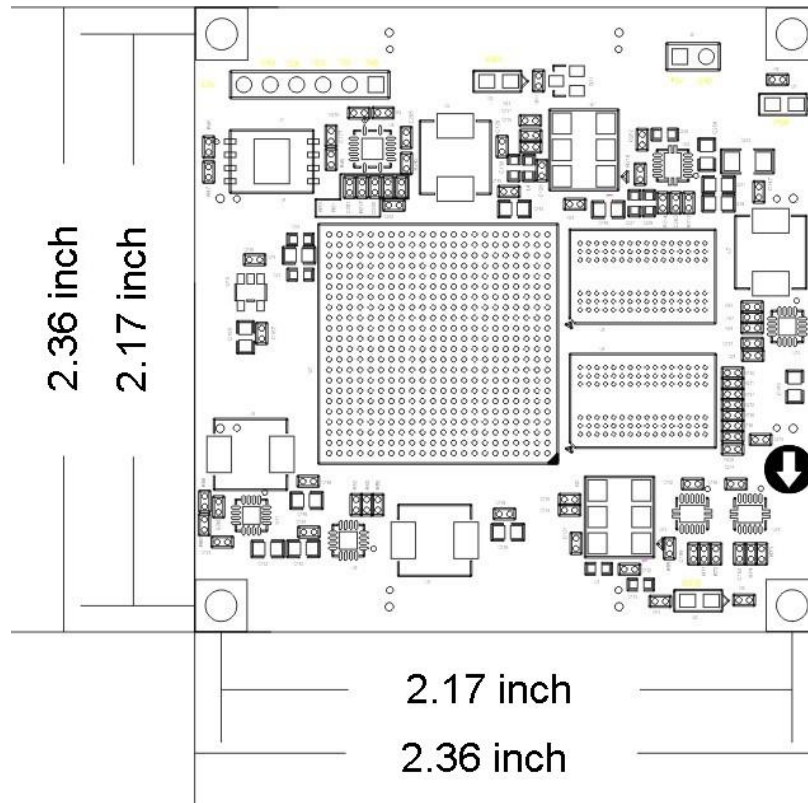


Figure 2-11-1: AC7A200 FPGA Core board (Top view)

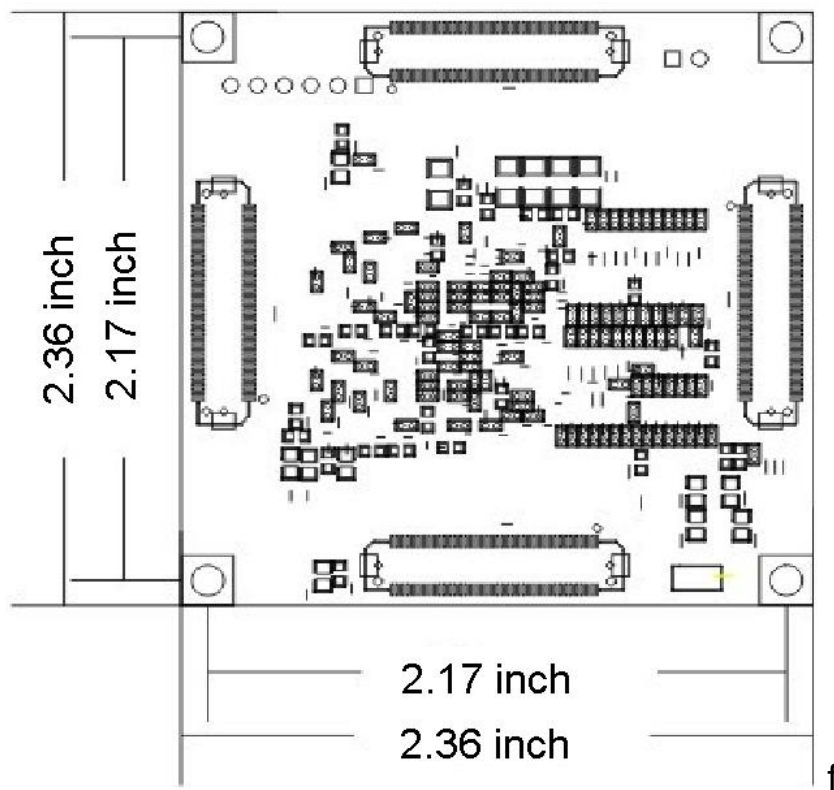
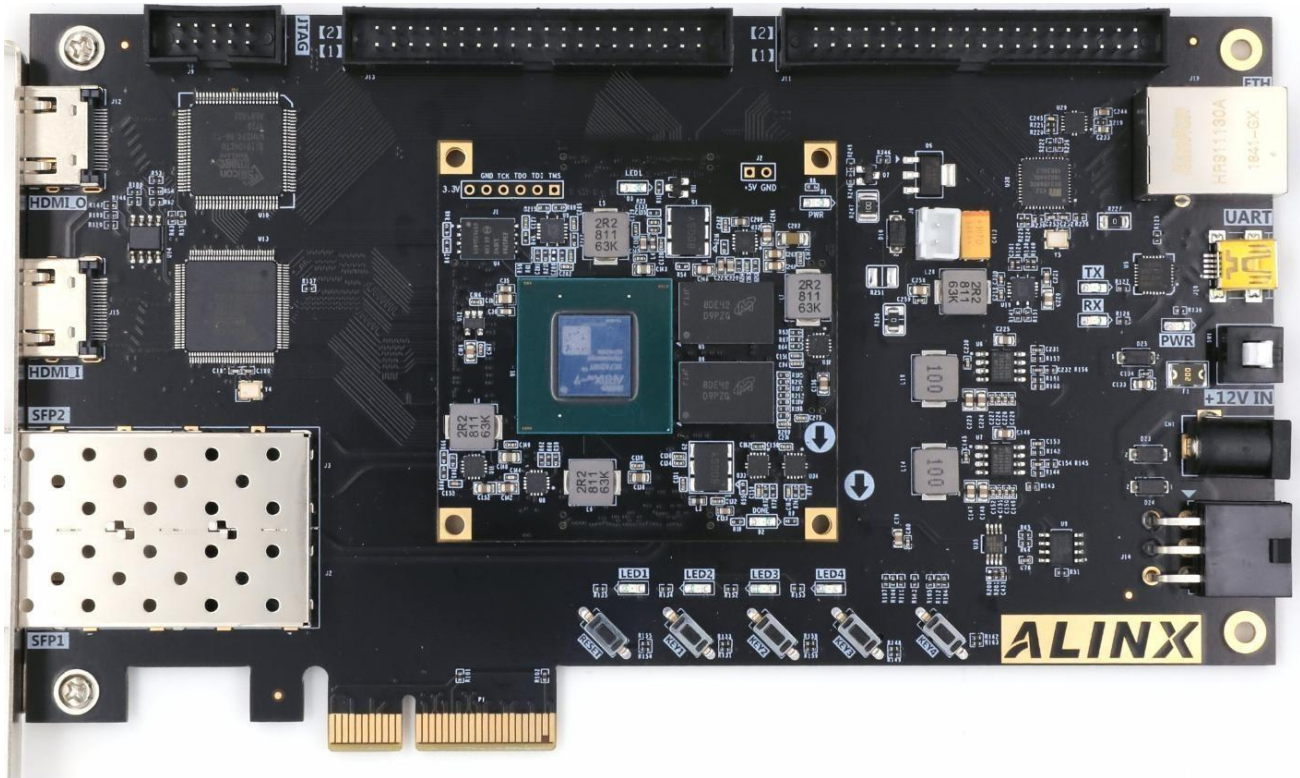


Figure 2-11-2: AC7A200 FPGA Core board (Bottom view)

## Part 3: Carrier Board



### Part 3.1: Carrier Board Introduction

Through the previous function introduction, you can understand the function of the carrier board part

- 1-channel PCIe x2 high speed data transmission interface
- 2-Port SPF cage
- 1-channel HDMI video input interface
- 1-channel HDMI video Output interface
- 1-channel 10/100M/1000M Ethernet RJ-45 interface
- 1-channel USB-to-Uart Bridge Communication interface
- 1 SD Card Slot
- EEPROM
- 2-channel 40-pin expansion ports
- JTAG debugging interface
- 5 independent buttons
- 4 user LED lights

## Part 3.2: Gigabit Ethernet Interface

The AX7A200 FPGA development board provides users with 1-channel Gigabit network communication service through the Micrel KSZ9031RNX Ethernet PHY chip. The Ethernet PHY chip is connected to the IO interface of the ARTIX7 FPGA. The KSZ9031RNX chip supports 10/100/1000 Mbps network transmission rate and communicates with the FPGA through the RGMII interface. KSZ9031RNX supports MDI/MDX adaptation, various speed adaptations, Master/Slave adaptation, and support for MDIO bus for PHY register management.

The KSZ9031RNX will detect the level status of some specific IOs to determine their working mode after powered on. Table 3-1-1 describes the default setup information after the GPHY chip is powered on.

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address 011
CLK125_EN	Enable 125Mhz clock output selection	Enable
LED_MODE	LED light mode configuration	Single LED light mode
MODE0~MODE3	Link adaptation and full duplex configuration	10/100/1000 adaptive, compatibleFull-duplex, half-duplex

Table 3-2-1: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of FPGA and PHY chip KSZ9031RNX is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising and falling edge of the clock.

When the network is connected to 100M Ethernet, the data transmission of FPGA and PHY chip KSZ9031RNX is communicated through the RMII bus, the transmission clock is 25Mhz, and the data is sampled on the rising and falling edge of the clock.



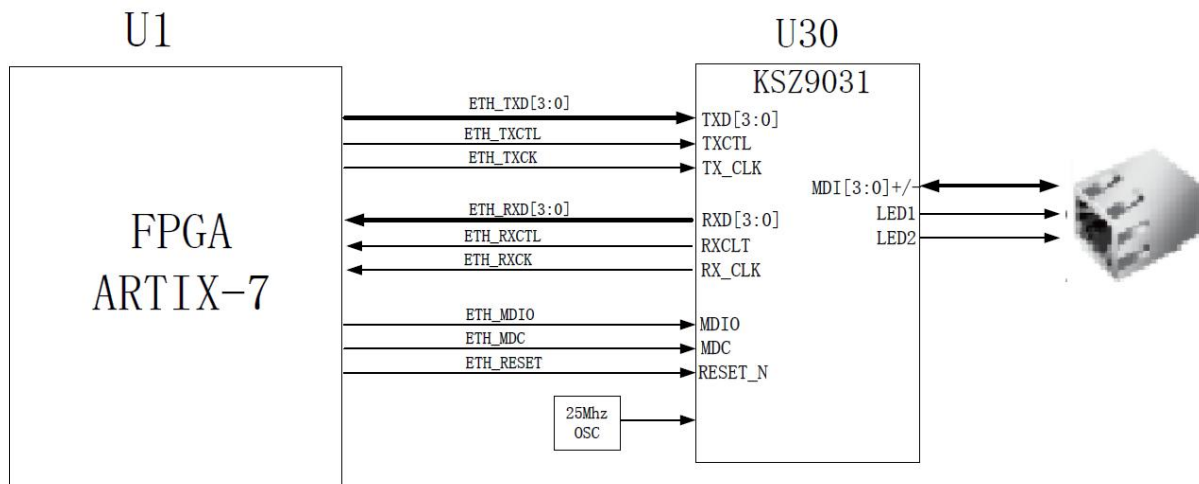


Figure 3-2-1: Gigabit Ethernet Interface Schematic

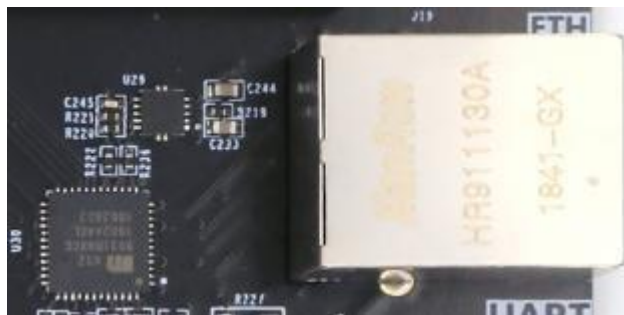


Figure 3-3-2: Gigabit Ethernet interface on the Carrier board

**Gigabit Ethernet Chip PHY pin assignments are as follows:**

Signal Name	FPGA Pin Number	Description
ETH_TXCK	P15	RGMIIT transmit clock
ETH_TXD0	N14	Transmit Data bit0
ETH_TXD1	P16	Transmit Data bit1
ETH_TXD2	R17	Transmit Data bit2
ETH_TXD3	R16	Transmit Data bit3
ETH_TXCTL	N17	Transmit Enable Signal
ETH_RXCK	V18	RGMIIT Receive Clock
ETH_RXD0	P19	Receive Data Bit0
ETH_RXD1	U18	Receive Data Bit1
ETH_RXD2	U17	Receive Data Bit2
ETH_RXD3	P17	Receive Data Bit3

ETH_RXCTL	R19	Receive data valid signal
ETH_MDC	N13	MDIO Management Clock
ETH_MDIO	P14	MDIO Management Data
ETH_RESET	R14	PHY Chip Reset Signal

### Part 3.3: SFP Interface

The AX7A200 FPGA development board has two optical interfaces. Users can purchase SFP optical modules (1.25G, 2.5G optical modules on the market) and insert them into these two optical interfaces for optical data communication. The two fiber interfaces are connected to the two RX/TX of the GNK transceiver of the FPGA. The TX signal and the RX signal are connected to the FPGA and the optical module through the DC blocking capacitor in differential signal mode. The TX and RX data rates are up to each 6.6Gb/s per channel. The reference clock for the GTX transceiver is provided by the 125Mhz differential clock of AC7A200 FPGA core board.

Figure 3-3-1 detailed the schematic diagram of FPGA and fiber design

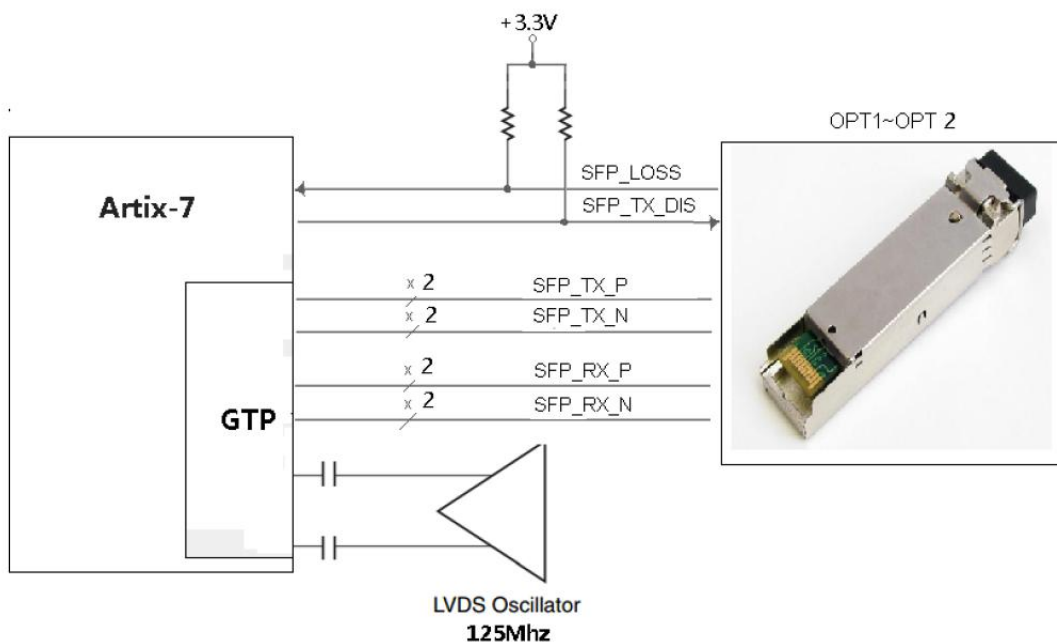


Figure 3-3-1: SFP Interface Schematic

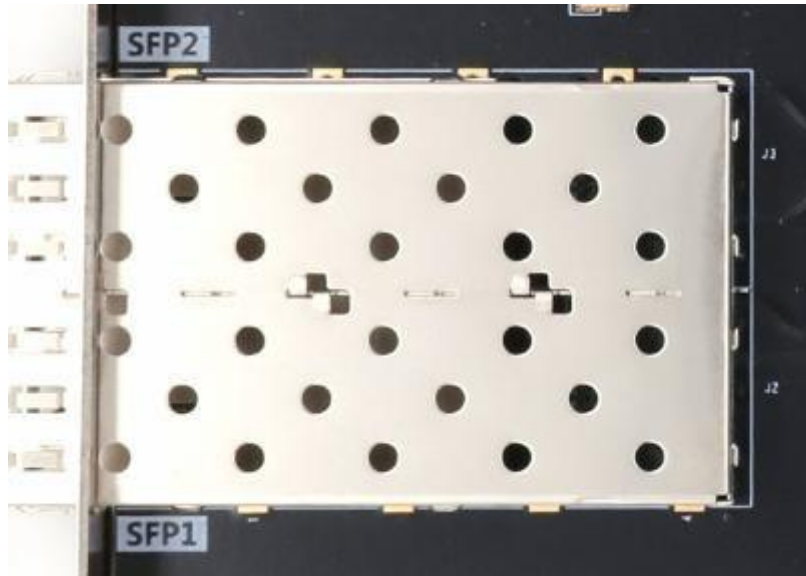


Figure 3-3-2: SFP interfaces on the Carrier Board

**The 1<sup>st</sup> fiber interface FPGA pin assignment is as follows:**

Signal Name	FPGA PIN	Description
SFP1_TX_P	B4	SFP1 Data Transfer (Positive)
SFP1_TX_N	A4	SFP1 Data Transfer (Negative)
SFP1_RX_P	B8	SFP1 Data Receiver (Positive)
SFP1_RX_N	A8	SFP1 Data Receiver (Negative)
SFP1_TX_DIS	J15	SFP1 Optical Transfer Disable, active high
SFP1_LOSS	H15	SFP1 Optical LOSS, High level means no light signal is received

**The 2<sup>nd</sup> fiber interface FPGA pin assignment is as follows:**

Signal Name	FPGA PIN	Description
SFP2_TX_P	D5	SFP2 Data Transfer (Positive)
SFP2_TX_N	C5	SFP2 Data Transfer (Negative)
SFP2_RX_P	D11	SFP2 Data Receiver (Positive)
SFP2_RX_N	C11	SFP2 Data Receiver (Negative)
SFP2_TX_DIS	H14	SFP2 Optical Transfer Disable, active high
SFP2_LOSS	J14	SFP2 Optical LOSS, High level means no light signal is received

## Part 3.4: PCIe x2 Interface

The AX7A200 FPGA development board provides an industrial-grade high-speed data transfer PCIe x2 interface (size dimension is PCIe x4). The PCIe card interface conforms to the standard PCIe card electrical specifications and can be used directly on the x4 PCIe slot of a normal PC.

The transmit and receive signals of the PCIe interface are directly connected to the GTP transceiver of the FPGA. The four channels of TX and RX signals are connected to the FPGA in differential signals, and the single channel communication rate can be up to 5G bit bandwidth. The PCIe reference clock is provided to the AX7A200 FPGA development board by the PCIe slot of the PC with a reference clock frequency of 100Mhz.

The design diagram of the PCIe interface of the AX7A200 FPGA development board is shown in Figure 3-4-1, where the TX transmit signal and the reference clock CLK signal are connected in AC coupled mode.

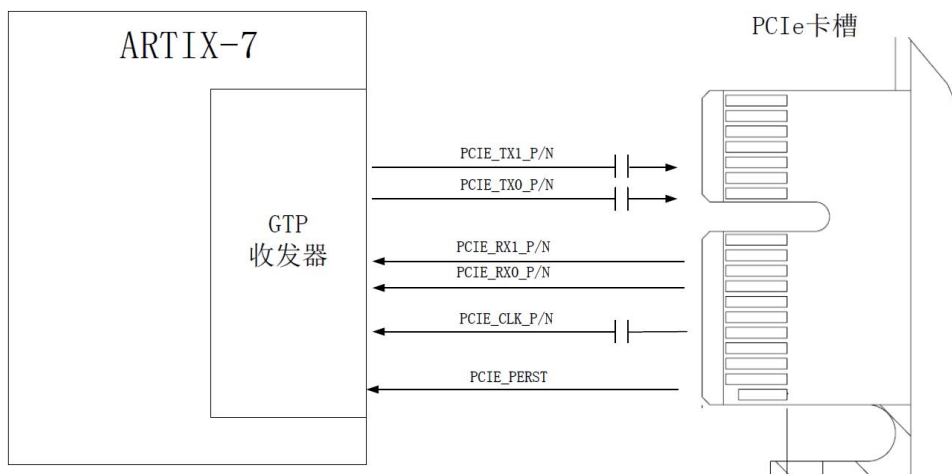


Figure 3-4-1: PCIe x2 schematic



Figure 3-4-2: PCIe x2 on the Carrier Board



**PCIex2 Interface Pin Assignment:**

Signal Name	FPGA Pin	Description
PCIE_RX0_P	D9	PCIE Channel 0 Data Receive Positive
PCIE_RX0_N	C9	PCIE Channel 0 Data Receive Negative
PCIE_RX1_P	B10	PCIE Channel 1 Data Receive Positive
PCIE_RX1_N	A10	PCIE Channel 1 Data Receive Negative
PCIE_TX0_P	D7	PCIE Channel 0 Data Transmit Positive
PCIE_TX0_N	C7	PCIE Channel 0 Data Transmit Negative
PCIE_TX1_P	B6	PCIE Channel 1 Data Transmit Positive
PCIE_TX1_N	A6	PCIE Channel 1 Data Transmit Negative
PCIE_CLK_P	F10	PCIE Reference Clock Positive
PCIE_CLK_N	E10	PCIE Reference Clock Negative

**Part 3.5: HDMI output interface**

HDMI output interface, select Sillion Image's SiI9134 HDMI (DVI) encoding chip, support up to 1080P@60Hz output, support 3D output.

The IIC configuration interface of SiI9134 is also connected to the IO of the FPGA. The SiI9134 is initialized and controlled by FPGA programming. The hardware connection of the HDMI output interface is shown in Figure 3-5-1.

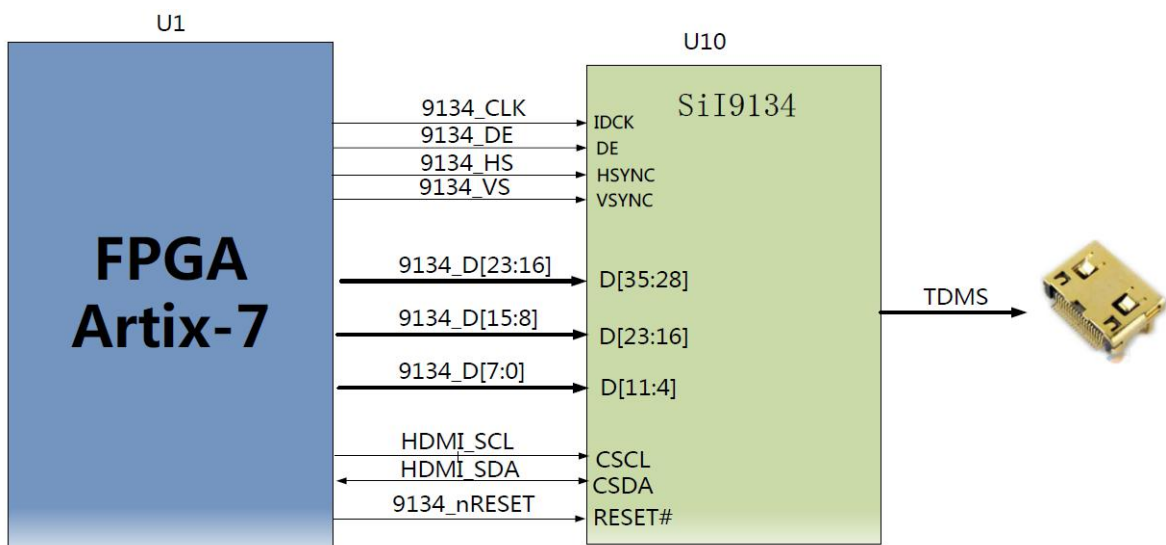


Figure 3-5-1: HDMI Output Schematic

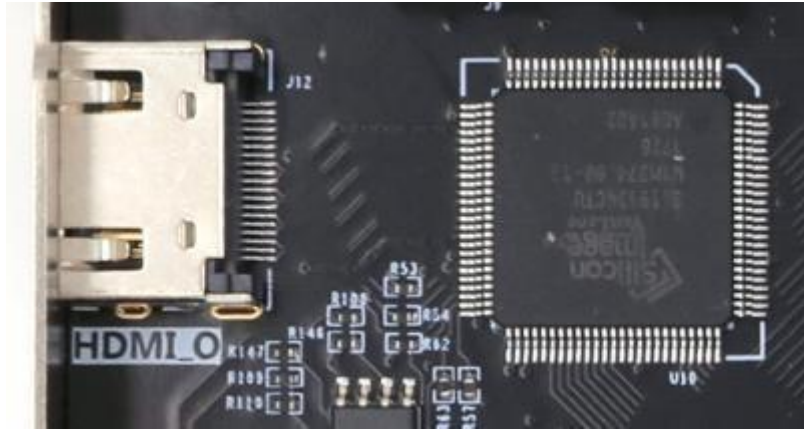


Figure 3-5-1: HDMI Output on the Carrire Board

**HDMI Input Pin Assignment:**

Signal Name	FPGA Pin
9134_NRESET	Y17
9134_CLK	Y22
9134_HS	T18
9134_VS	R18
9134_DE	U22
9134_D[0]	V22
9134_D[1]	Y18
9134_D[2]	Y19
9134_D[3]	W19
9134_D[4]	W20
9134_D[5]	Y21
9134_D[6]	U21
9134_D[7]	T21
9134_D[8]	W21
9134_D[9]	W22
9134_D[10]	T20
9134_D[11]	AB18
9134_D[12]	AA18
9134_D[13]	AA19
9134_D[14]	AB20
9134_D[15]	AA20
9134_D[16]	AA21

9134_D[17]	AB22
9134_D[18]	AB21
9134_D[19]	W17
9134_D[20]	V17
9134_D[21]	V20
9134_D[22]	U20
9134_D[23]	V19
HDMI_SCL	H13
HDMI_SDA	G13

### Part 3.6: HDMI Input interface

HDMI output interface, select Sillion Image's SiI9013/9011 HDMI decoder chip, support up to 1080P@60Hz input and support data output in different formats.

The IIC configuration interface of the SiI9013/9011 is connected to the IO of the FPGA. The SiI9013 is initialized and controlled through FPGA programming. The hardware connection of the HDMI input interface is shown in Figure 3-6-1.

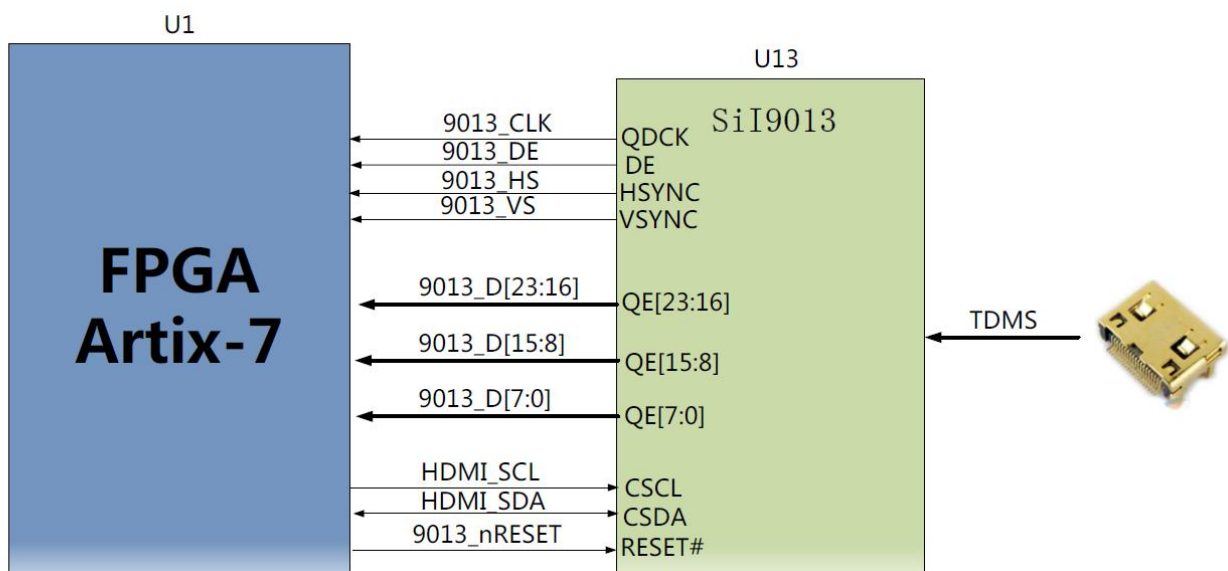


Figure 3-6-1: HDMI Input Schematic

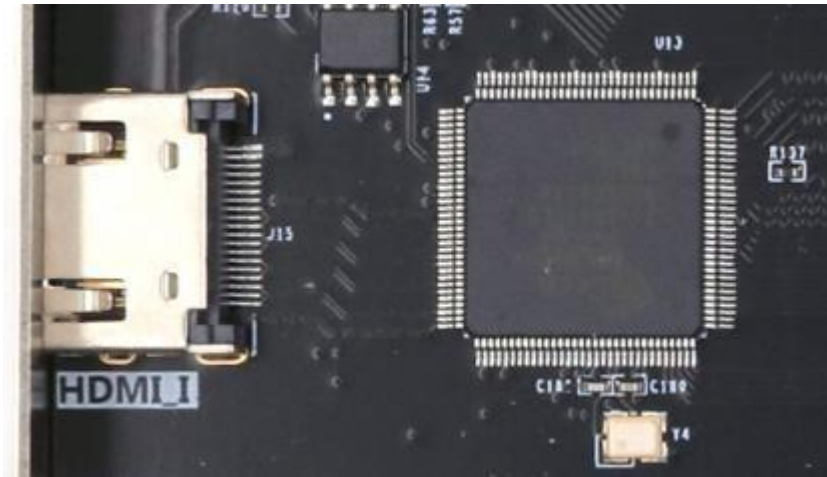


Figure 3-6-2: HDMI Input on the Carrier Board

**HDMI Input Pin Assignment:**

Signal Name	FPG Pin Number
9013_NRESET	J21
9013_CLK	K18
9013_HS	N18
9013_VS	M18
9013_DE	N19
9013_D[0]	M20
9013_D[1]	N20
9013_D[2]	L21
9013_D[3]	M21
9013_D[4]	K19
9013_D[5]	H17
9013_D[6]	H18
9013_D[7]	N22
9013_D[8]	M22
9013_D[9]	K22
9013_D[10]	K21
9013_D[11]	J22
9013_D[12]	H22
9013_D[13]	H20
9013_D[14]	G20
9013_D[15]	M17

9013_D[16]	J16
9013_D[17]	G17
9013_D[18]	G18
9013_D[19]	G15
9013_D[20]	G16
9013_D[21]	J19
9013_D[22]	H19
9013_D[23]	J20
HDMI_SCL	H13
HDMI_SDA	G13

## Part 3.7: SD Card Slot

The SD card (Secure Digital Memory Card) is a memory card based on the semiconductor flash memory process. It was completed in 1999 by the Japanese Panasonic-led concept, and the participants Toshiba and SanDisk of the United States conducted substantial research and development. In 2000, these companies launched the SD Association (Secure Digital Association), which has a strong lineup and attracted a large number of vendors. These include IBM, Microsoft, Motorola, NEC, Samsung, and others. Driven by these leading manufacturers, SD cards have become the most widely used memory card in consumer digital devices.

The SD card is a very common storage device. The extended SD card supports SPI mode and SD mode. The SD card used is a MicroSD card. The schematic diagram is shown in Figure 3-7-1.

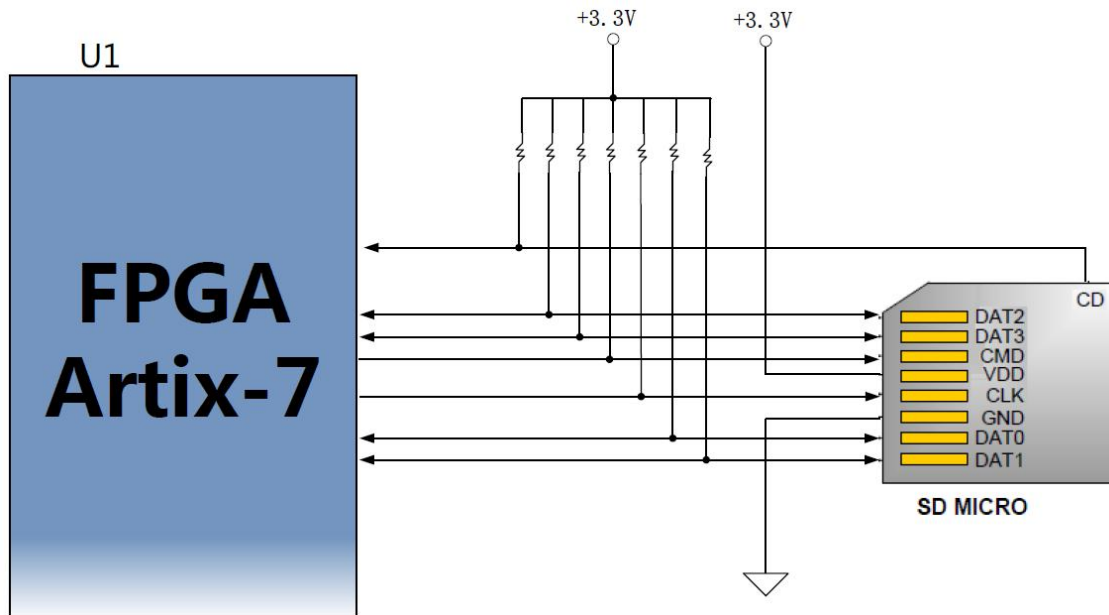


Figure 3-7-1: SD Card Schematic

**SD card slot pin assignment:**

SD Mode	
Signal Name	FPGA PIN
SD_CLK	E13
SD_CMD	E14
SD_CD_N	C13
SD_DAT0	D15
SD_DAT1	D14
SD_DAT2	F14
SD_DAT3	F13

**Part 3.8: USB-to-Uart Bridge Connector**

The AX7A200 FPGA development board includes the USB-UAR chip of Silicon Labs CP2102GM. The USB interface uses the MINI USB interface. It can be connected to the USB port of the upper PC for serial data communication with a USB cable. The schematic diagram of the USB Uart circuit design is shown in Figure 3-8-1:

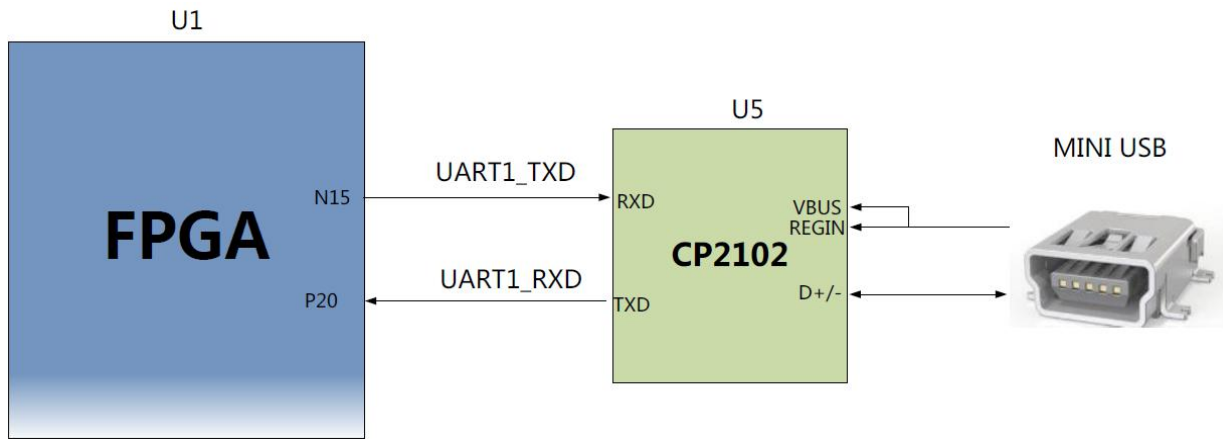


Figure 3-8-1: USB to serial port schematic



Figure 3-8-2: USB to serial port on the Carrier Board

Two LED indicators (LED3 and LED4) are set for the serial port signal, and the silkscreen on the PCB is TX and RX, indicating that the serial port has data transmission or reception, as shown in the following Figure 3-8-3

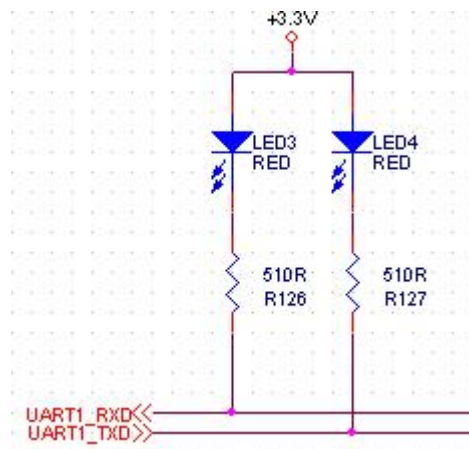


Figure 3-8-3: Serial Port communication LED Indicators Schematic



**USB-to-UART pin assignment:**

Signal Name	FPGA PIN
UART1_RXD	L14
UART1_TXD	L15

**Part 3.9: EEPROM 24LC04**

AX7A200 carrier board contains an EEPROM, model 24LC04, and has a capacity of 4Kbit (2\*256\*8bit). It consists of two 256-byte blocks and communicates via the IIC bus. The onboard EEPROM is to learn how to communicate with the IIC bus. The I2C signal of the EEPROM is connected to the BANK15 IO port on the FPGA side. Figure 3-9-1 below shows the design of the EEPROM

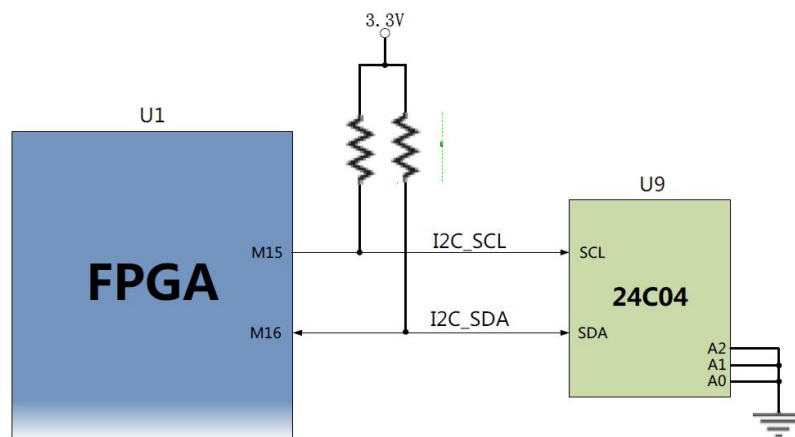


Figure 3-8-1: EEPROM Schematic

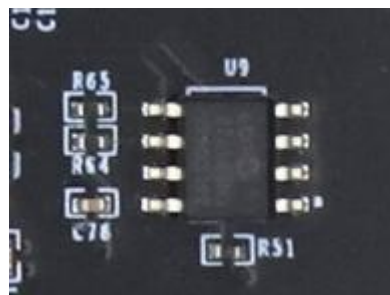


Figure 3-9-2: EEPROM on the Carrier Board

**EEPROM Pin Assignment**

Net Name	FPGA PIN
----------	----------

I2C_SCL	M15
I2C_SDA	M16

### Part 3.10: Temperature Sensor

A high-precision, low-power, digital temperature sensor chip is mounted on the AX7A200 FPGA development board, and the model is LM75 of ON Semiconductor. The temperature accuracy of the LM75 chip is 0.5 degrees, I2C bus is shared with EEPROM. The sensor and FPGA are directly connected to the I2C digital interface. The FPGA reads the temperature near the current FPGA development board through the I2C interface. Figure 3-10-1 below shows the design of the LM75 sensor chip.

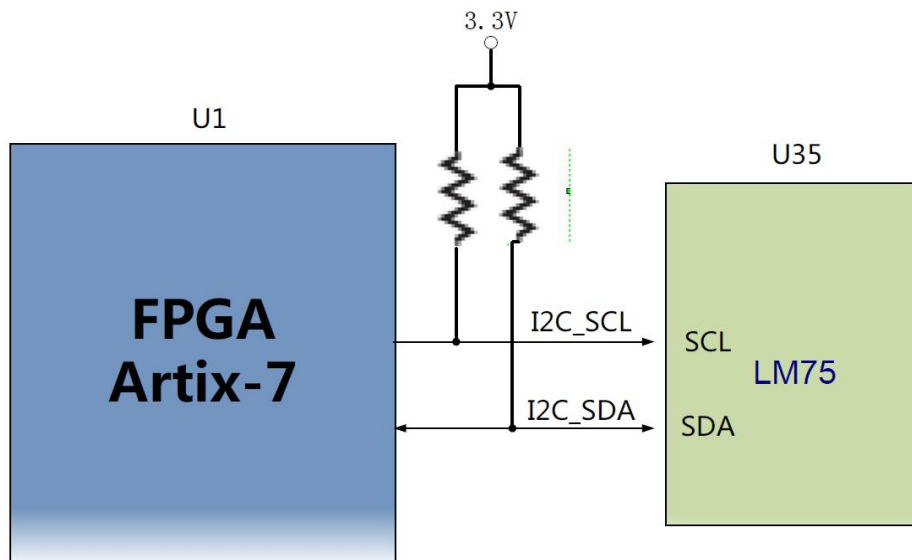


Figure 3-10-1: LM75 Sensor Schematic

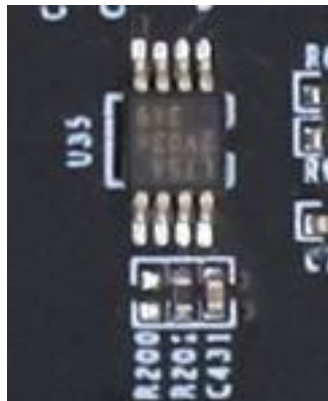


Figure 3-10-2: LM75 Sensor on the FPGA Board

### LM75 Sensor Pin Assignment

Pin Name	FPGA Pin
LM75_SCL	M15
LM75_SDA	M16

### Part 3.11: Expansion Header

The carrier board is reserved with two 0.1inch spacing standard 40-pin expansion ports J11 and J13, which are used to connect the ALINX modules or the external circuit designed by the user. The expansion port has 40 signals, of which 1-channel 5V power supply, 2-channel 3.3 V power supply, 3-channle ground and 34 IOs. **Do not directly connect the IO directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.**

A 33 ohm resistor is connected in series between the expansion port and the FPGA connection to protect the FPGA from external voltage or current. The circuit of the expansion port (J11) is shown in Figure 3-11-1.

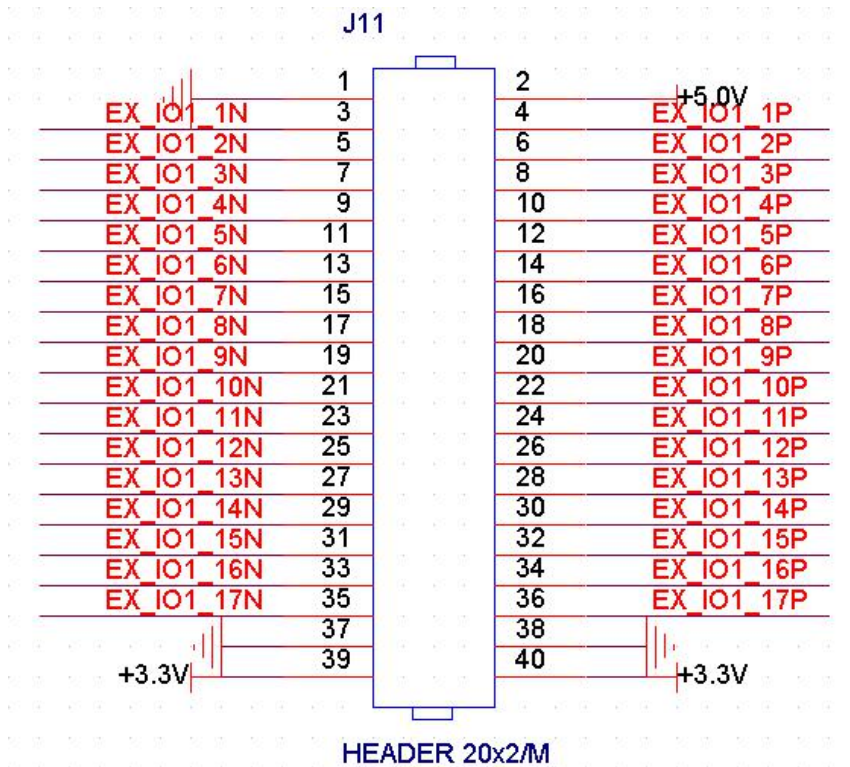


Figure 3-11-1: Expansion header J11 schematic

The figure 3-11-2 detailed the J11 expansion port on the carrier board. The Pin1 and Pin2 of the expansion port are already marked on the board.



Figure 3-11-2: Expansion header J11 on the Carrier Board

### J11 Expansion Header Pin Assignment

Pin Number	FPGA Pin	Pin Number	FPGA Pin
1	GND	2	+5V
3	G21	4	G22
5	C22	6	B22
7	F19	8	F20
9	D20	10	C20
11	A18	12	A19
13	B20	14	A20
15	F18	16	E18
17	E19	18	D19
19	C18	20	C19
21	B17	22	B18
23	D17	24	C17
25	A15	26	A16
27	B15	28	B16
29	A13	30	A14
31	E16	32	D16
33	C14	34	C15
35	F16	36	E17
37	GND	38	GND
39	+3.3V	40	+3.3V

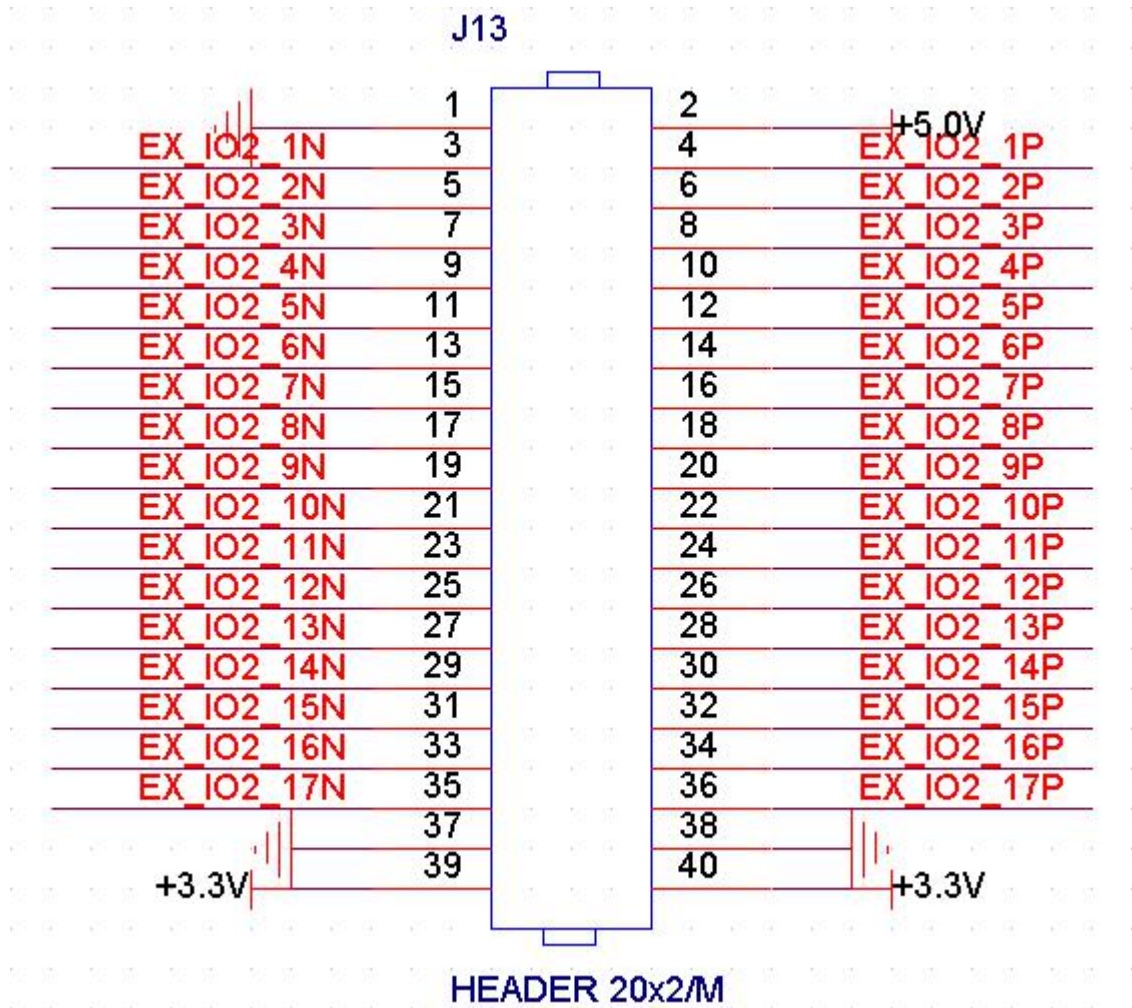


Figure 3-11-3: Expansion header J13 schematic

The figure 3-11-4 detailed the J13 expansion port on the carrier board. The Pin1 and Pin2 of the expansion port are already marked on the board.



Figure 3-11-4: Expansion header J13 on the carrier board

### J13 Expansion Header Pin Assignment

Pin Number	FPGA Pin	Pin Number	FPGA Pin
------------	----------	------------	----------

1	GND	2	+5V
3	W16	4	W15
5	T15	6	T14
7	GND	8	U15
9	V14	10	V13
11	W12	12	W11
13	Y12	14	Y11
15	W10	16	V10
17	AA10	18	AA11
19	AA9	20	AB10
21	U16	22	T16
23	AA13	24	AB13
25	AB11	26	AB12
27	Y13	28	AA14
29	W14	30	Y14
31	Y16	32	AA16
33	AB16	34	AB17
35	AA15	36	AB15
37	GND	38	GND
39	+3.3V	40	+3.3V

## Part 3.12: JTAG Interface

The development board reserves a JTAG interface for downloading FPGA programs or firmware to FLASH. In order to prevent damage to the FPGA chip caused by hot plugging, we added a protection diode to the JTAG signal to ensure that the signal voltage is within the range accepted by the FPGA to avoid damage to the FPGA.



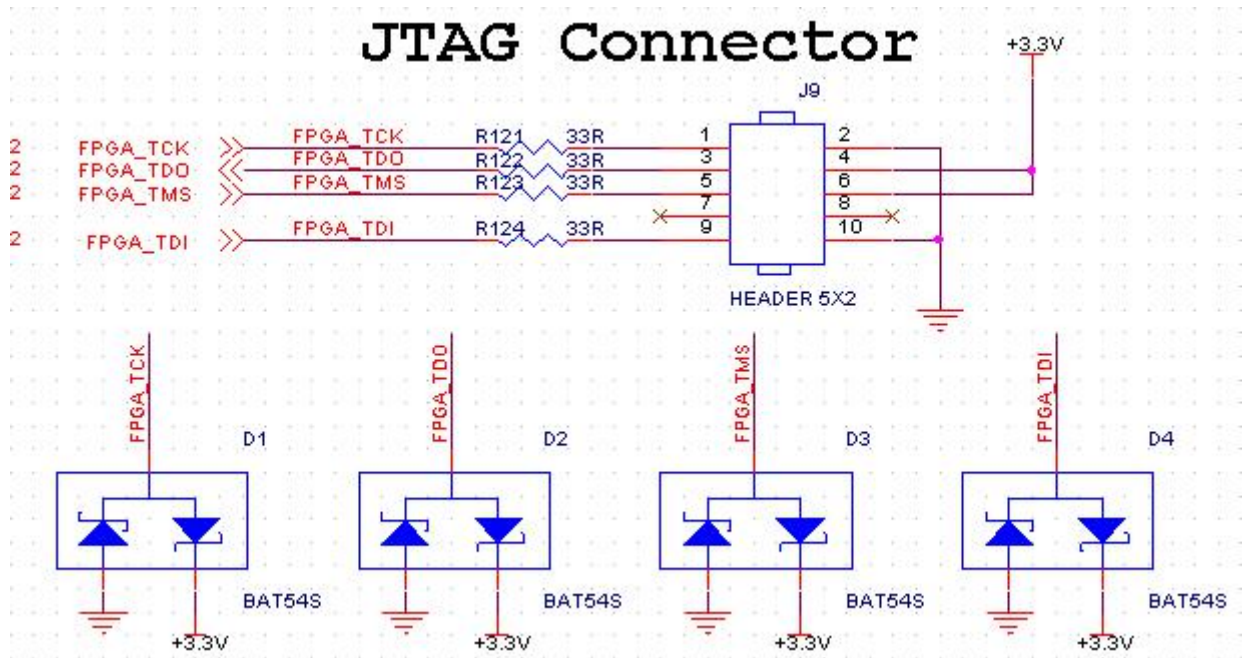


Figure 3-12-1: JTAG Interface Schematic

*Be careful not to hot plug the JTAG cable*



Figure 3-12-2: JTAG Interface on the Carrier Board

### Part 3.13: Buttons

The AX7A200 FPGA carrier board contains five user buttons RESET, KEY1~KEY4, and all the buttons are connected to the normal IO of the FPGA. The button is active low. When the button is pressed, the IO input voltage of the FPGA is low. When no button is pressed, The IO input voltage of the FPGA is high. The circuit of the button part is shown in Figure 3-13-1.

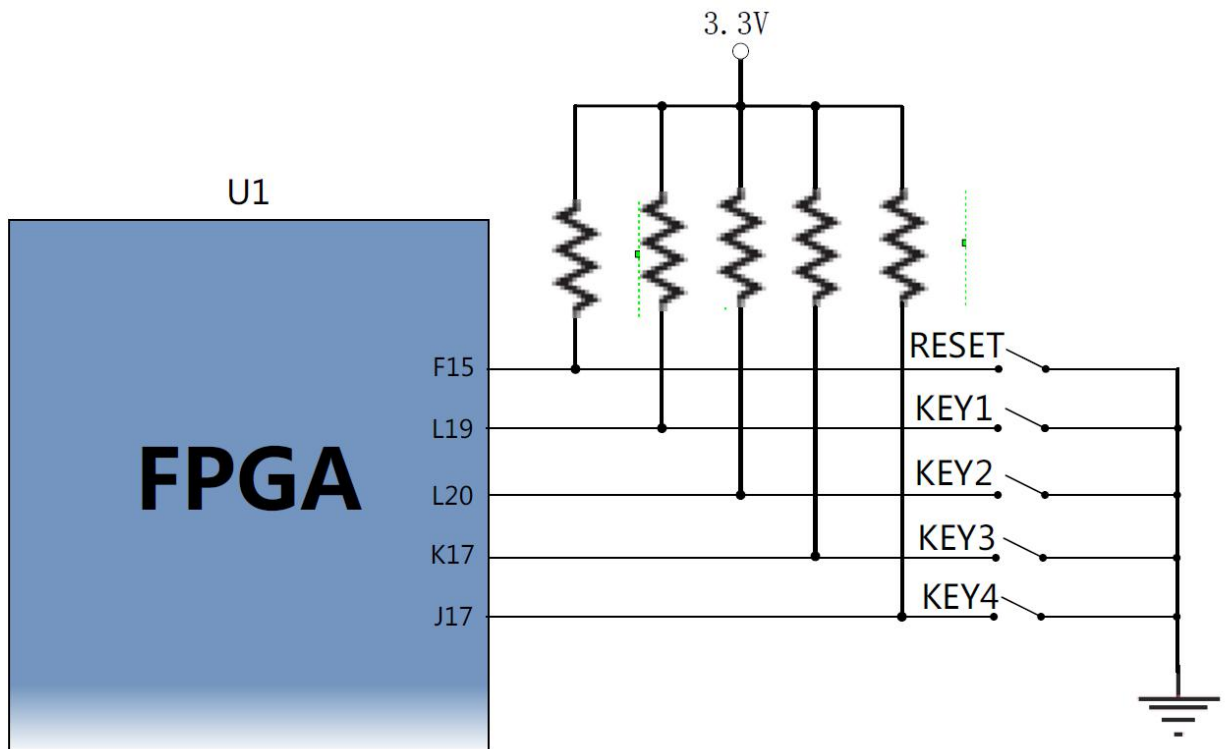


Figure 3-13-1: Button Schematic



Figure 3-13-2: Buttons on the Carrier Board

### Buttons Pin Assignment

Net Name	FPGA PIN
RESET	F15
KEY1	L19
KEY2	L20
KEY3	K17
KEY4	J17

### Part 3.14: LED Light

There are seven red LEDs on the AX7A200 FPGA carrier board, one of which is the power indicator (PWR), two are USB Uart data receiving and

transmitting indicators, and four are users LED lights (LED1~LED4). When the board is powered on, the power indicator will light up; User LED1~LED4 are connected to the normal IO of the FPGA. When the IO voltage connected to the user LED is configured low level, the user LED lights up. When the connected IO voltage is configured as high level, the user LED will be extinguished. The schematic diagram of the user LEDs hardware connection is shown in Figure 3-14-1.

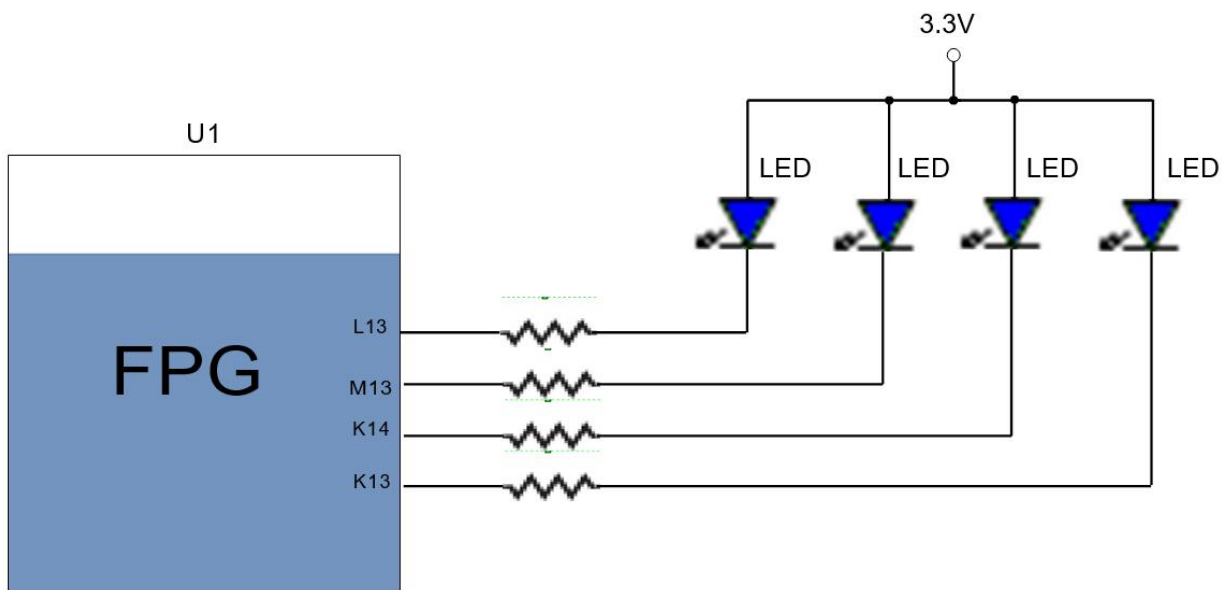


Figure 3-14-1: The User LEDs Schematic

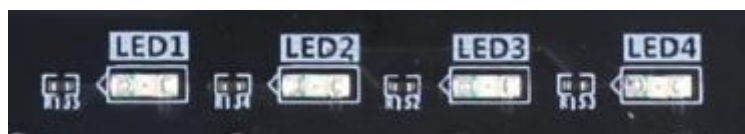


Figure 3-14-2: The User LEDs on the Carrier Board

### Pin assignment of user LED lights

Signal Name	FPGA PIN
LED1	L13
LED2	M13
LED3	K14
LED4	K13

## Part 3.15: Power Supply

The power input voltage of the AX7A200 FPGA development board is DC12V. The development board also supports power from the PCIe interface.

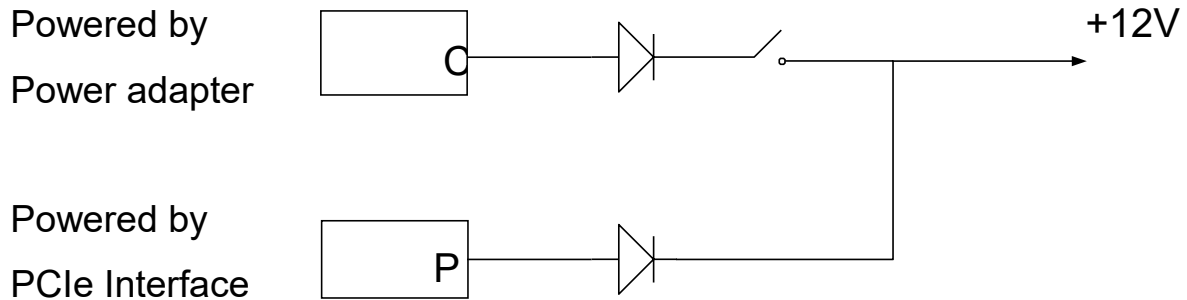


Figure 3-15-1: Power supply method for AX7A200 FPGA Board

The FPGA carrier board converts +12V voltage to +3.3V and +1.8V through two DC/DC power chip MP1482; one DC/DC power chip TPS54620 converts +12V voltage into +5V; one LDO power chip TPS74701 converts the +1.8V voltage to +1.2V. In addition, the +5V power supply on the carrier board supplies power to the core board through the inter-board connector. The power supply design on the carrier board is shown in Figure 3-15-2.

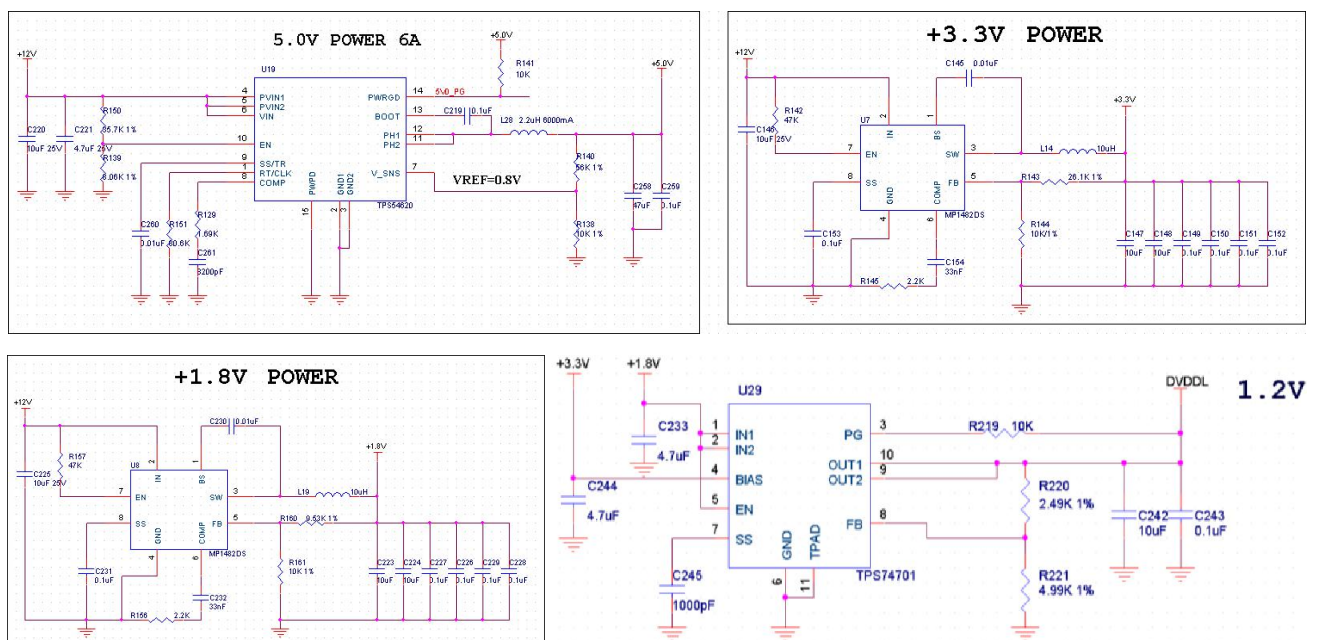


Figure 3-15-2: Power supply Schematic on the Carrier Board

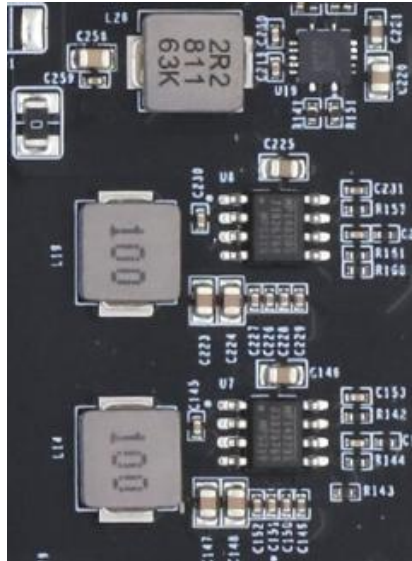


Figure 3-15-3: Power Supply Circuit on the Carrier Board

### Part 3.16: Fan

Because the FPGA chip generates a lot of heat when it works normally, we add a heat sink and fan to the chip to prevent the chip from overheating. The fan is controlled by the FPGA chip. The control pin is connected to the IO of the BANK16. If the IO level output is low, the MOSFET is turned on, the fan operates, and if the IO level output is high, the fan stops. The fan design on the board is shown in Figure 3-16-1:

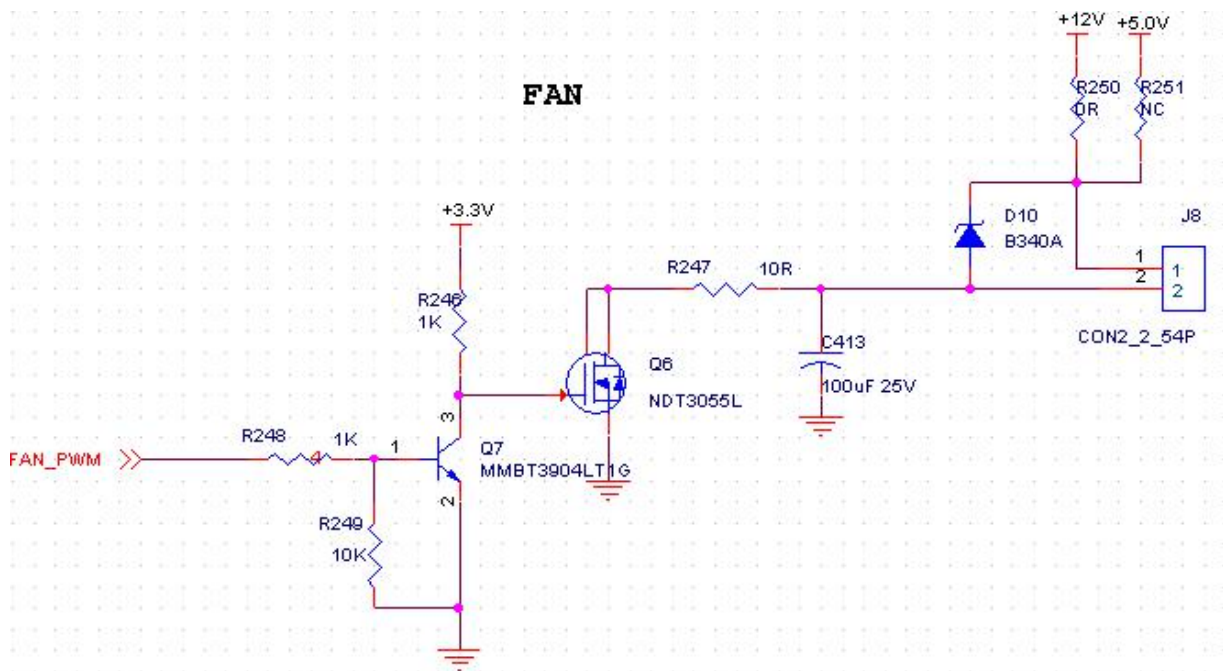


Figure 3-16-1: Fan design schematic



The fan has been screwed to the development board before leaving the factory. The power of the fan is connected to the J8 socket. The red is positive and the black is negative.

### Part 3.17: Carrier Board Size Dimension

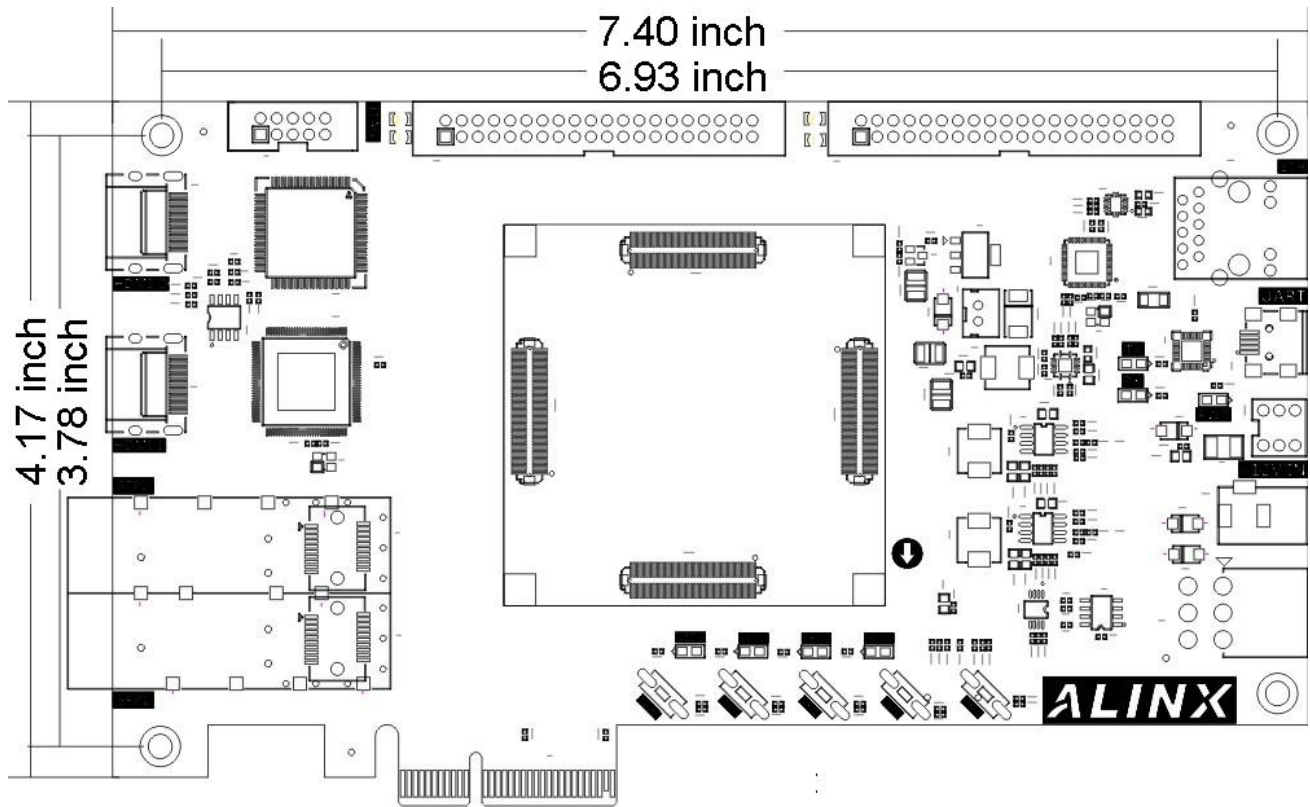


Figure 3-17-1: Carrier Board Size Dimension