TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 9 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2089C-35
TMM2089C-45
TMM2089C-55

PRELIMINARY

DESCRIPTION

The TMM2089C is a 73,728 bits high speed N-channel silicon gate MOS static random access memory organized as 8,192 words by 9 bits and operates from a single 5-volt supply. The TMM2089C is features an automatic stand-by mode when deselect by $\overline{CS1}$ signal. Thus the TMM2089C is suitable for use in cache memory and high speed storage. The TMM2089C has nine I/O terminals, therefore it is most suitable for MEMORY SYSTEM with Parity bit. The TMM2089C is offered is a 28 pin standard ceramic dual in-line package with 0.3 inch width for high density assembly.

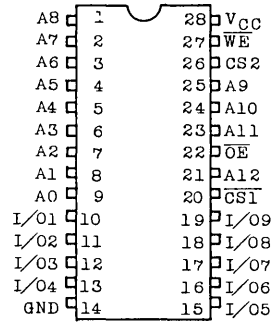
FEATURES

- Access Time and Current

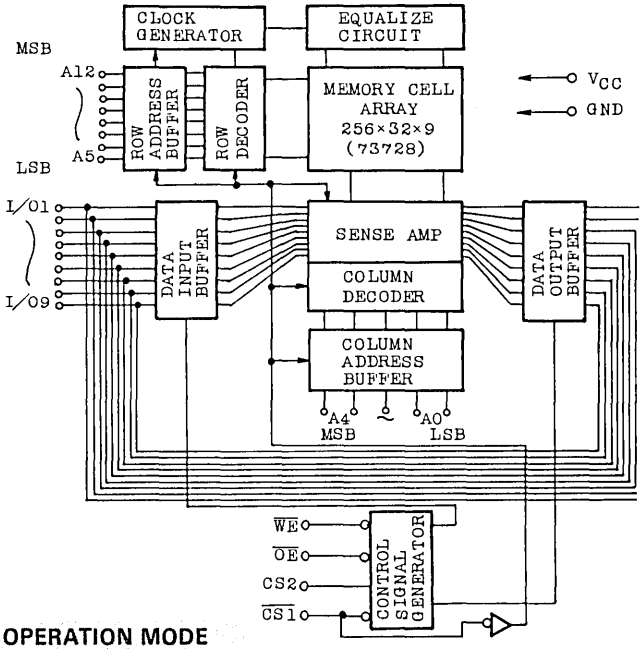
Part Number \ Parameter	Access Time (MAX.)	Operating Current (MAX.)	Standby Current (MAX.)
TMM2089C-35	35ns	135mA	15mA
TMM2089C-45	45ns	135mA	15mA
TMM2089C-55	55ns	135mA	15mA

- Single 5V Power Supply
- Fully static Operation
- Power Down Feature : ($\overline{CS1}$)
- Output Buffer Control : ($\overline{OE}$)
- Three State Outputs
- All Inputs and Outputs: (Directly TTL Corpatible)
- Inputs Protected : (All inputs have protection against static charge.)

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{12}$	Address Inputs
$\overline{CS1}$, CS2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
I/O1~I/O9	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground

OPERATION MODE

MODE	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	I/O1~9	Power
Write	L	H	*	L	In	Active
Read	L	H	L	H	Out	Active
Standby	H	*	*	*	High-Z	Standby
Standby	L	L	*	*	High-Z	Active
Output Buffer Disable	L	H	H	H	High-Z	Active

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−3.5~7.0	V
V_{IN}, V_{OUT}	Input Output Voltage	−3.5~7.0	V
$T_{opr.}$	Operating Temperature	0~70	°C
$T_{stg.}$	Storage Temperature	−55~150	°C
T_{nolder}	Soldering Temperature.·Time	260·10	°C·sec
P_D	Power Dissipation (Ta=70°C)	1.0	W

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−3.0	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.50	5.00	5.50	V

* Pulse width : 10ns, DC : −0.5V (Min.)

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	−1.0	1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V	−4.0	—	mA
I_{OL}	Output Low Current	V_{OL}=0.4V	8.0	—	mA
I_{LO}	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	−1.0	1.0	μA
I_{SBP}	Peak Power-on Current	$\overline{CS1}$=V_{CC}, CS2=0V, I_{OUT}=0mA	—	30	mA
I_{SB}	Standby Current	$\overline{CS1}$=V_{IH}, I_{OUT}=0mA	—	15	mA
I_{CC}	Operating Current	$\overline{CS1}$=V_{IL}, I_{OUT}=0mA	—	135	mA

CAPACITANCE * (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	pF

* Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TMM2089C-35		TMM2089C-45		TMM2089C-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	—	45	—	55	—	ns
t_{ACC}	Address Access Time	—	35	—	45	—	55	
t_{CO1}	$\overline{CS1}$ Access Time	—	35	—	45	—	45	
t_{CO2}	CS2 Access Time	—	25	—	25	—	30	
t_{OE}	$\overline{OE}$ Access Time	—	20	—	20	—	25	
t_{OH}	Output Data Hold Time from Address Change	5	—	5	—	5	—	
t_{CLZ}	Output Enable Time from $\overline{CS1}$ or CS2	0	—	5	—	5	—	
t_{CHZ}	Output Disable Time from $\overline{CS1}$ or CS2	—	20	—	20	—	20	
t_{OLZ}	Output Enable Time from $\overline{OE}$	0	—	0	—	0	—	
t_{OHZ}	Output Disable Time from $\overline{OE}$	—	10	—	10	—	15	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Dowen Time	—	30	—	30	—	30	

WRITE CYCLE

SYMBOL	PARAMETER	TMM2089C-35		TMM2089C-45		TMM2089C-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	—	45	—	55	—	ns
t_{CW}	Chip Selection to End of Write	30	—	40	—	50	—	
t_{AS}	Address Set Up Time	0	—	0	—	0	—	
t_{WP}	Write Pulse Width	25	—	35	—	45	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{DS}	Data Set UP Time	15	—	20	—	20	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	
t_{WLZ}	Output Enable Time from $\overline{WE}$	0	—	0	—	0	—	
t_{WHZ}	Output Disable Time from $\overline{WE}$	—	10	—	10	—	15	

A.C. TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Time	5ns
Input and Output Reference Levels	2.0V/0.8V
Output Load	Fig.1

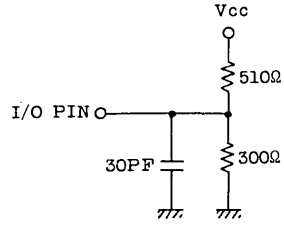
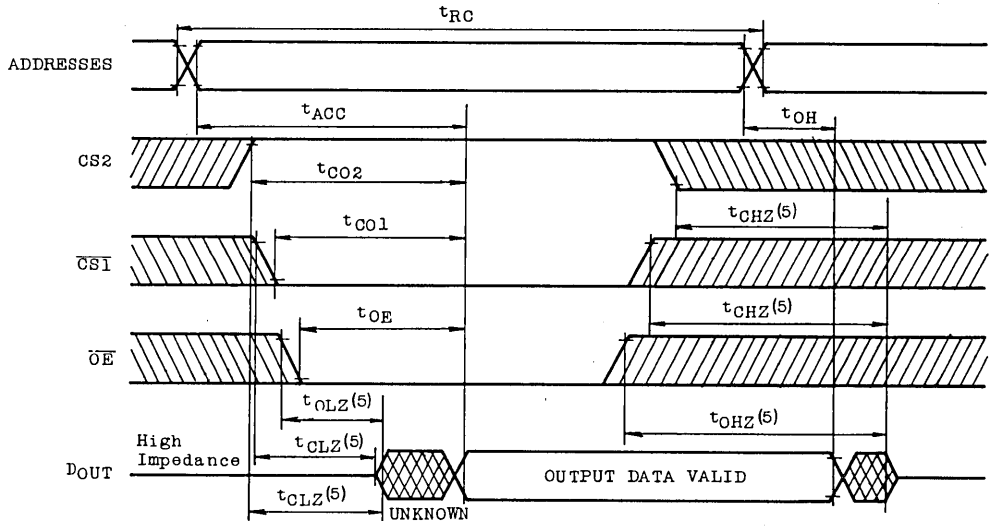


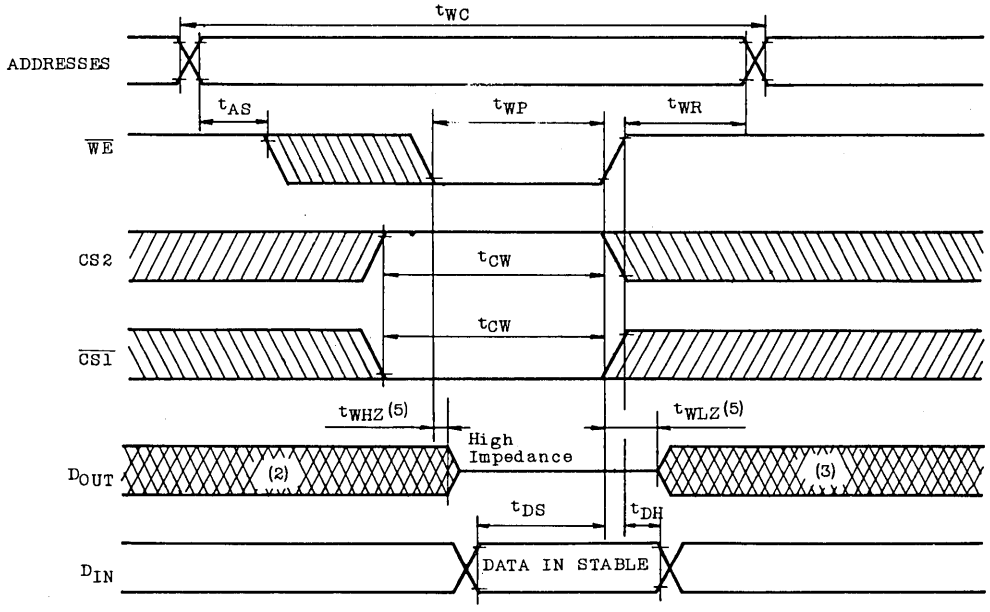
Fig.1 Output Load

TIMING WAVEFORMS

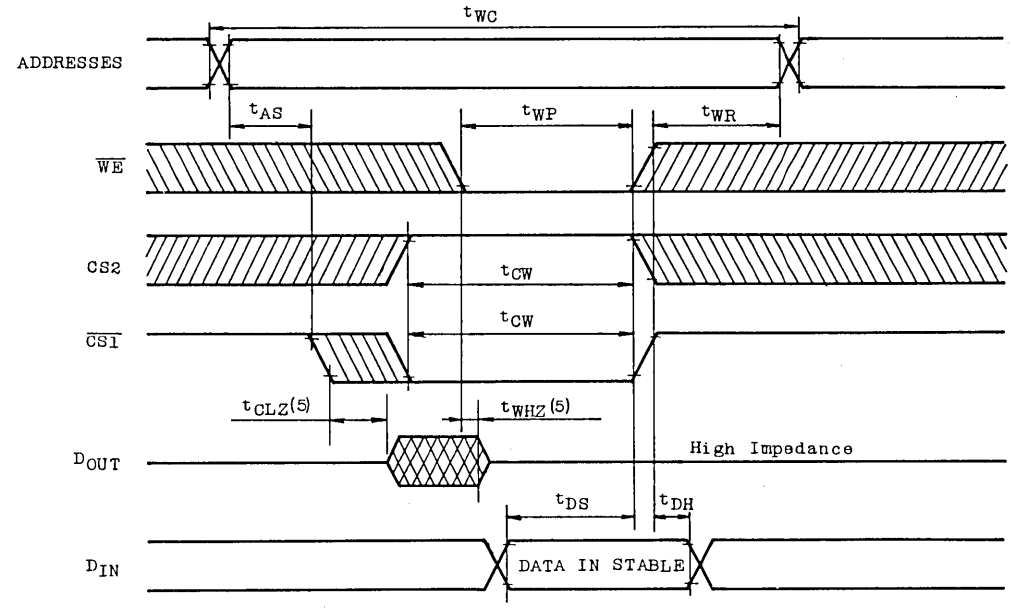
- READ CYCLE (1)



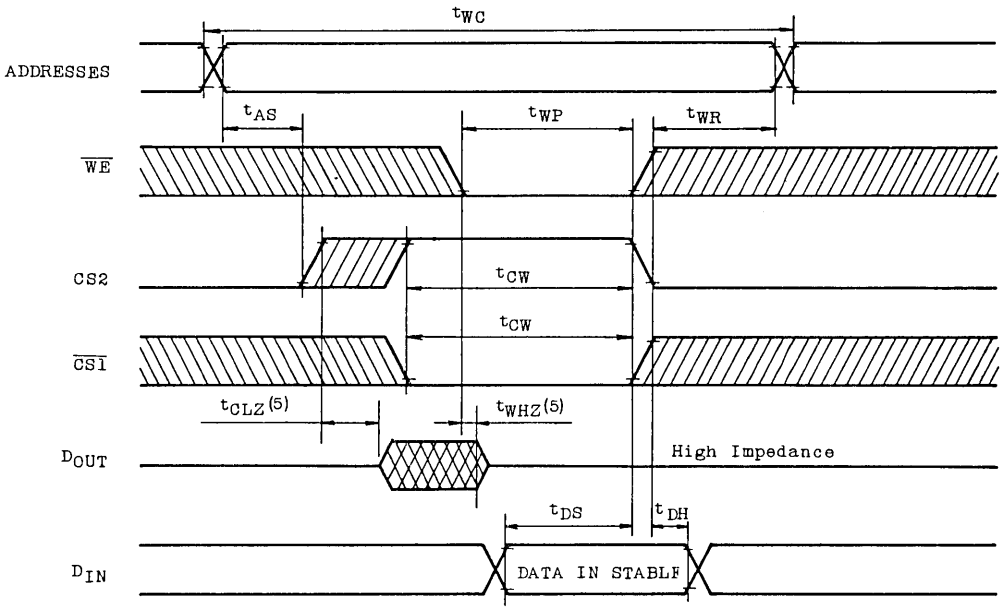
- WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



● WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



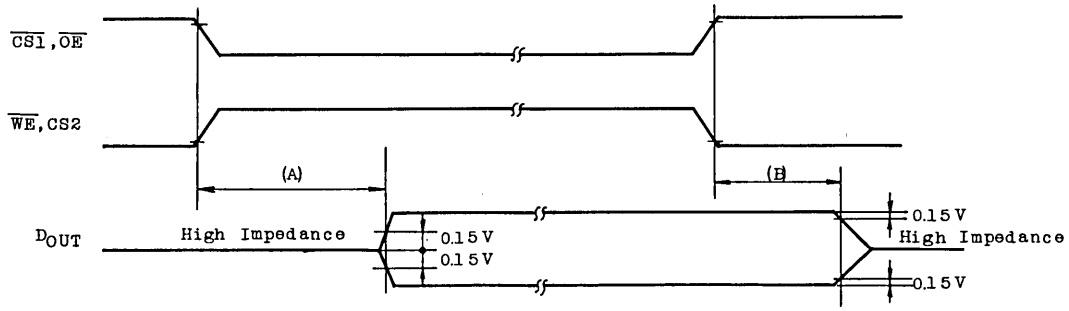
● WRITE CYCLE 3 (4) ($\overline{CS2}$ Controlled Write)



NOTE :

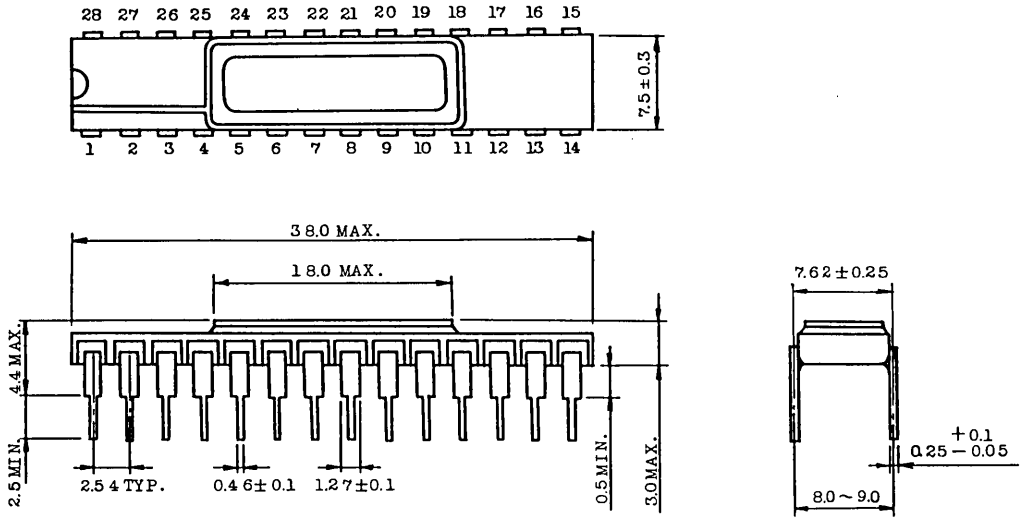
1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CS1}$ Low transition or CS2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CS1}$ Hight transition or CS2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain is a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load in Fig. 1.

(A) t_{CLZ}, t_{OLZ}, t_{WLZ}·····Output Enable Time
(B) t_{CHZ}, t_{OHZ}, t_{WHZ}·····Output Disable Time



OUTLINE DRAWINGS

Unit: mm



Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.28 leads.