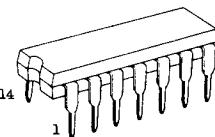


**TC5029BP QUAD 2-INPUT NAND GATE WITH N-CHANNEL OPEN DRAIN OUTPUT**

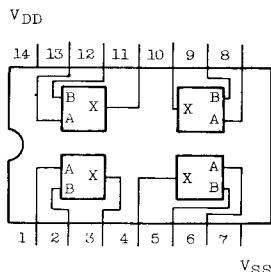
TC5029BP contains four circuits of 2 input NAND gates having its respective outputs of N-channel open drain structure.

Since the drain voltage of output transistors are guaranteed up to 26 volts, these can be used for wide range of applications such as level shifters and drivers, and the wired OR arrangement is also easily obtained. Please utilize these for level shifters for P-channel MOS, controlling analog switches of positive/negative power supplies, etc.



DIP 14 (3D 14A--P)

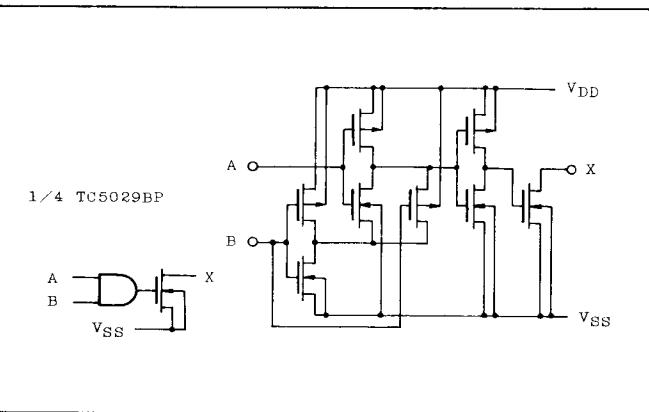
**PIN ASSIGNMENT**



\* **ABSOLUTE MAXIMUM RATINGS**

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V <sub>DD</sub>	V <sub>SS</sub> -0.5 ~ V <sub>SS</sub> +20	V
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.5 ~ V <sub>DD</sub> +0.5	V
Output Voltage	V <sub>OUT</sub>	V <sub>SS</sub> -0.5 ~ V <sub>SS</sub> +26	V
DC Input Current	I <sub>IN</sub>	±10	mA
Power Dissipation	P <sub>D</sub>	300	mW
Storage Temperature Range	T <sub>stg</sub>	-65 ~ 150	°C
Lead Temp./Time	T <sub>sol</sub>	260°C . 10sec	

**CIRCUIT DIAGRAM**



**TRUTH TABLE**

INPUTS		OUTPUT
B	A	X
L	L	HZ
L	H	HZ
H	L	HZ
H	H	L

HZ ; HIGH IMPEDANCE

RECOMMENDED OPERATION CONDITIONS (V<sub>SS</sub>-OV)

CHARACTERISTIC	SYMBOL				MIN.	TYP.	MAX.	UNIT
Supply Voltage	V <sub>DD</sub>				3	-	18	V
Input Voltage	V <sub>IN</sub>				0	-	V <sub>DD</sub>	V
Output Voltage	V <sub>OUT</sub>				0	-	24	V
Operating Temperature	T <sub>opr</sub>				-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V<sub>SS</sub>=OV)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V <sub>DD</sub> (V)	-40°C		25°C			85°C		UNIT	
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
Low Level Output Voltage	V <sub>OL</sub>	I <sub>OUT</sub> < 1μA V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5 10 15	- 0.05 0.05	0.05 - 0.05	- 0.00 0.00	0.00 0.05 0.05	0.05 - -	- 0.05 0.05	0.05 0.05 0.05	V	
Low Level Output Current	I <sub>OL</sub>	V <sub>OL</sub> =0.4V V <sub>OL</sub> =0.5V V <sub>OL</sub> =1.5V V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5 10 15	3.2 5.0 24.0	- 5.0 -	3.2 5.0 24.0	- - -	2.5 3.6 18.0	- - -	*	mA	
High Level Input Voltage **	V <sub>IH</sub>	V <sub>OUT</sub> =0.5V, 4.5V V <sub>OUT</sub> =1.0V, 9.0V V <sub>OUT</sub> =1.5V, 13.5V I <sub>OUT</sub> < 1μA	5 10 15	3.5 7.0 11.0	- - -	3.5 7.0 11.0	2.75 5.5 8.25	- - -	3.5 7.0 11.0	- - -	V	
Low Level Input Voltage **	V <sub>IL</sub>	V <sub>OUT</sub> =0.5V, 4.5V V <sub>OUT</sub> =1.0V, 9.0V V <sub>OUT</sub> =1.5V, 13.5V I <sub>OUT</sub> < 1μA	5 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.5 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0		
Output off Leakage Current	I <sub>DH</sub>	V <sub>OH</sub> =24V	-	-	0.5	-	10 <sup>-3</sup>	0.5	-	50	μA	
Input Current	High Level	I <sub>IH</sub>	V <sub>IH</sub> =18V	18	-	0.3	-	10 <sup>-5</sup>	0.3	-	1.0	μA
	Low Level	I <sub>IL</sub>	V <sub>IL</sub> =OV	18	-	-0.3	-	-10 <sup>-5</sup>	-0.3	-	-1.0	
Quiescent Current Consumption	I <sub>DD</sub>	V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub> *	5 10 15	- - -	1.0 2.0 4.0	- - -	0.001 0.001 0.002	1.0 2.0 4.0	- - -	7.5 15 30	μA	

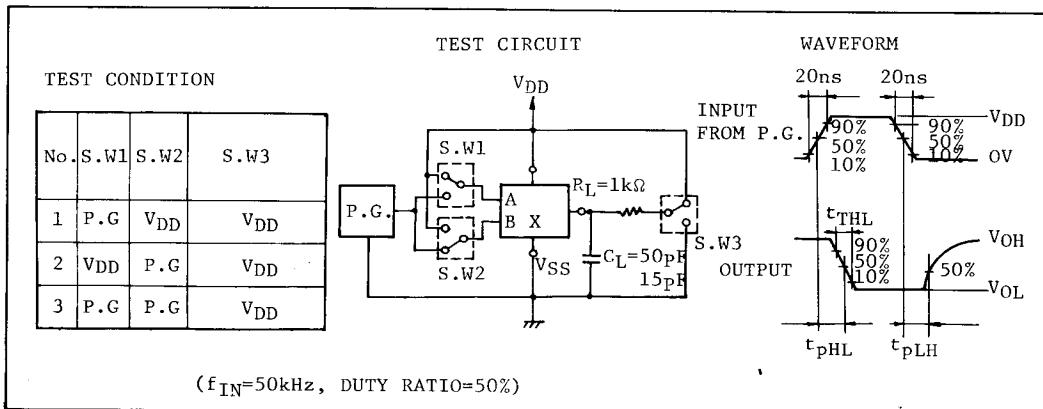
\* All valid input combinations. Outputs open.

\*\* R<sub>L</sub>=20KΩ

SWITCHING CHARACTERISTICS ( $T_a=25^\circ C$ ,  $V_{SS}=OV$ )

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	$V_{DD}$ (V)	MIN.	TYP.	MAX.	UNIT
Output Fall Time	$t_{THL}$	$C_L=50\text{pF}$	5 10 15	- - -	85 30 20	200 80 60	ns
(Low-High) Propagation Delay Time	$t_{PLH}$	$R_L=1\text{k}\Omega$ $C_L=15\text{pF}$	5 10 15	- - -	230 120 100	500 200 150	ns
(High-Low) Propagation Delay Time	$t_{PHL}$	$R_L=1\text{k}\Omega$ $C_L=15\text{pF}$	5 10 15	- - -	260 90 60	500 200 150	ns
(Low-High) Propagation Delay Time	$t_{PLH}$	$R_L=10\text{k}\Omega$ $C_L=15\text{pF}$	5 10 15	- - -	830 680 610	1200 1000 850	ns
(High-Low) Propagation Delay Time	$t_{PHL}$	$R_L=10\text{k}\Omega$ $C_L=50\text{pF}$	5 10 15	- - -	270 95 63	500 200 150	ns
Input Capacitance	$C_{IN}$			-	5	7.5	$\text{pF}$
Output Off Capacitance	$C_{OUT}$			-	25	-	$\text{pF}$

## SWITCHING TIME TEST CIRCUIT AND WAVEFORM



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