NIPPON PRECISION CIRCUITS LTD.

SM5130

PLL IC for Cordless Telephone

■ GENERAL DESCRIPTION

The SM5130 is a digital phase-locked loop (PLL) designed for cordless telephone system operating in the range of 46 - 49 MHz. This device is manufactured using MOLYGATE (モリゲート®) CMOS technology developed by NPC. The SM5130 contains two PLL circuits separately for the transmitter and the receiver, and therefore a single SM5130 can be used to build both handset and baseset in the cordless telephone system.

■ FEATURES

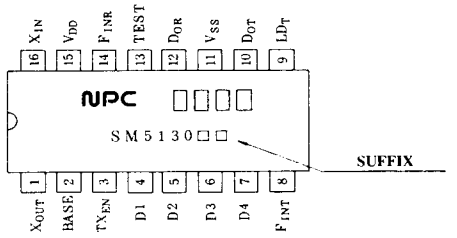
- Low supply voltage — Vdd=2.~5.5V
- Higher operating frequency — Fin=60MHz (MAX)
- High input sensitivity — Vin=300mVVp-p (MIN)
- Direct dividing for transmitter — 46~49MHz
- Baseset/Handset interchangeable
- Power saving function (non-transmitting section standby)
- On-chip digital unlock detector
- 16/18-pin plastic DIP/SOP
- Molybdenum gate CMOS

■ PRODUCT SELECTION LIST

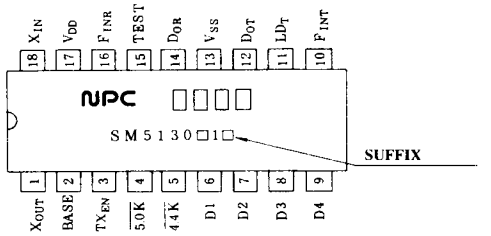
Suffix	Device No	Package	Lead	D1~D4 Terminal
AP	SM5130AP	DIP	16	On Chip pull-down resistor (For mechanical switch)
AS	SM5130AS	SOP		
AIP	SM5130A1P	DIP	18	
AIS	SM5130A1S	SOP		
DP	SM5130DP	DIP	16	without pull-down resistor (For µp control)
DS	SM5130DS	SOP		
DIP	SM5130DIP	DIP	18	
DIS	SM5130D1S	SOP		

■ PIN CONFIGURATION

- 16-Pin TOP VIEW



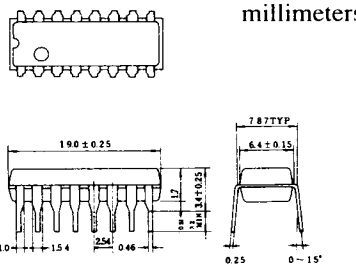
- 18-Pin



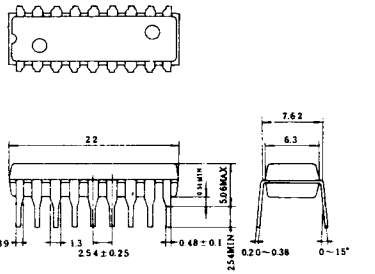
■ PACKAGE DIMENSIONS

- 16-Pin DIP

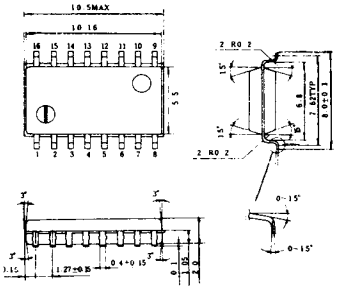
All dimensions in millimeters



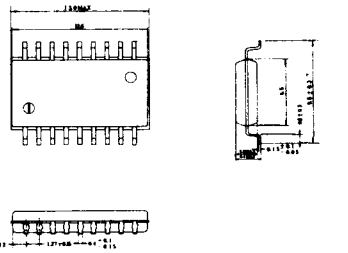
- 18-Pin DIP



- 16-Pin SOP



- 18-Pin SOP



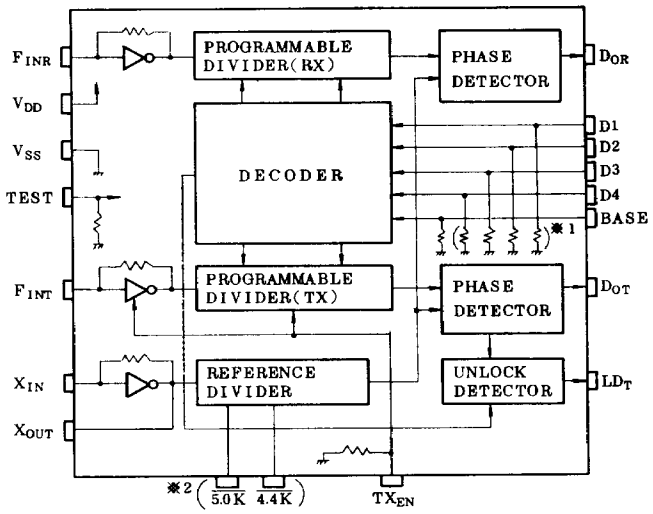
モリゲート® is a registered trademark of NPC Ltd.

■ PIN DESCRIPTION

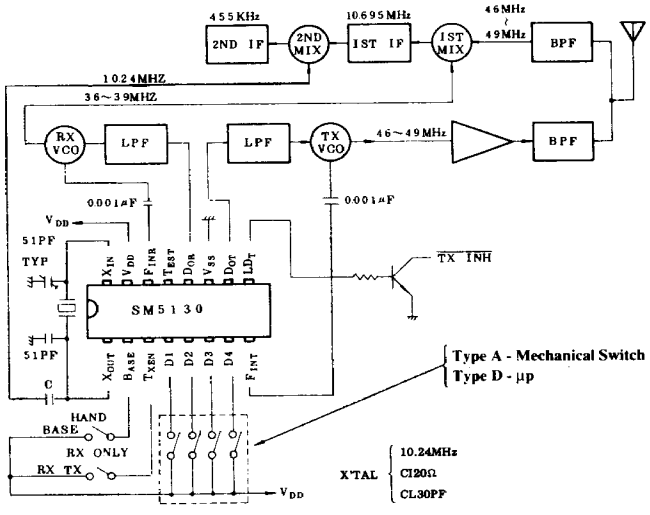
Pin No		Name	DESCRIPTION
16 Pins	18 Pins		
1	1	X_{OUT}	To connect crystal and capacitor. Output for 2nd mixer of receiver.
2	2	BASE	Baseset/Handset select V_{DD}: Baseset, Open: Handset
3	3	TX_{EN}	V_{DD}: Transmitter PLL operating mode Open; Standby mode (Low current consumption) On chip pull-down resistor
–	4	$\overline{5.0K}$	5kHz Output, Nch open drain
–	5	$\overline{4.4K}$	4.4kHz Output, Nch open drain
4	6	D1	Channel (1~10) set up terminal Type A; on chip pull-down resistor Type D; without pull-down resistor
5	7	D2	
6	8	D3	
7	9	D4	

Pin No.		Name	Description
16 Pins	18 Pins		
8	10	F_{INT}	Programable divider for transmitter input. On chip feed back resistor (AC coupling possible)
9	11	LD_T	Unlock detector output. On chip digital lock detector VDD level, Unlock (Transmitter only)
10	12	D_{OT}	To connect low pass filter of transmitter Tri-state output, for passive filter
11	13	V_{SS}	Ground
12	14	D_{OR}	To connect low pass filter of receiver. Tri-state output, for passive filter.
13	15	TEST	Test terminal. Normally open.
14	16	F_{INR}	Programmable divider for receiver input. On chip feed back resistor (AC coupling possible)
15	17	V_{DD}	Power-supply 2.4~5.5V
16	18	X_{IN}	To connect crystal (10.24MHz) and capacitor. On chip feed back resistor.

■ BLOCK DIAGRAM



■ APPLICATION (For 16-Pin device)



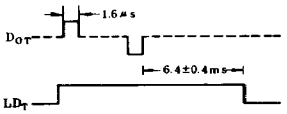


Figure 1 LDT and DOT waveforms

Notes:

1. LPF (passive low pass filter)
2. VCO increases the input voltage as the frequency becomes higher.
3. LDT becomes "H" (VDD level) when the channel has changed or the output time of DOT is over 1.6μs. LDT returns to "L" (ground level) 6.4 +/- 0.4 μs after such conditions (see Figure 1) are over.

■ FREQUENCY TABLE

Base	Channel Set-up				CH	TX (f_{REF} = 2.5KHz)		RX (f_{REF} = 2.5KHz)		
	D_4	D_3	D_2	D_1		f_{TX}, f_{VCO} (MHz)	N	f_{RX} (MHz)	f_{VCO} (MHz)	N
0	0	0	0	1	1	49.670	19868	46.610	35.915	14366
	0	0	1	0	2	49.845	19938	46.630	35.935	14374
	0	0	1	1	3	49.860	19944	46.670	35.975	14390
	0	1	0	0	4	49.770	19908	46.710	36.015	14406
	0	1	0	1	5	49.875	19950	46.730	36.035	14414
	0	1	1	0	6	49.830	19932	46.770	36.075	14430
	0	1	1	1	7	49.890	19956	46.830	36.135	14454
	1	0	0	0	8	49.930	19972	46.870	36.175	14470
	1	0	0	1	9	49.990	19996	46.930	36.235	14494
	1	0	1	0	10	49.970	19988	46.970	36.275	14510
1	0	0	0	1	1	46.610	18644	49.670	38.975	15590
	0	0	1	0	2	46.630	18652	49.845	39.150	15660
	0	0	1	1	3	46.670	18668	49.860	39.165	15666
	0	1	0	0	4	46.710	18684	49.770	39.075	15630
	0	1	0	1	5	46.730	18692	49.875	39.180	15672
	0	1	1	0	6	46.770	18708	49.830	39.135	15654
	0	1	1	1	7	46.830	18732	49.890	39.195	15678
	1	0	0	0	8	46.870	18748	49.930	39.235	15694
	1	0	0	1	9	46.930	18772	49.990	39.295	15718
	1	0	1	0	10	46.970	18788	49.970	39.275	15710

■ ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Power-supply voltage	V_{DD}-V_{SS}	-0.3~7.0	V
Input voltage	V_{IN}	V_{SS}~V_{DD}	V
Operating Temperature	T_{OPR}	-30~+80	°C
Storage Temperature	T_{STG}	-40~+125	°C
Soldering Temperature	T_{SLD}	260±5	°C
Soldering Time	T_{SLD}	10.5±0.5	sec.

■ ELECTRICAL CHARACTERISTICS

Ta=-30~80°C V_{SS}=OV V_{DD}=2.4~5.5V

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Operating Voltage	V_{DD}		2.4		5.5	V	
Current Consumption (1)	$I_{DD}1$	V_{DD}=2.4V TX_{EN}=H		2.5		mA	note 1 figure 2
	$I_{DD}2$	V_{DD}=3.0V TX_{EN}=H		4.0	7.0	mA	
	$I_{DD}3$	V_{DD}=4.5V TX_{EN}=H		9.0		mA	
	$I_{DD}4$	V_{DD}=5.5V TX_{EN}=H		13.0		mA	
Current Consumption (2)	$I_{DD}5$	V_{DD}=2.4V TX_{EN}=L		1.5		mA	note 2 figure 3
	$I_{DD}6$	V_{DD}=3.0V TX_{EN}=L		3.0	5.0	mA	
	$I_{DD}7$	V_{DD}=4.5V TX_{EN}=L		5.0		mA	
	$I_{DD}8$	V_{DD}=5.5V TX_{EN}=L		10.0		mA	
Operating Frequency	F_{TX}	F_{INT}=F_{INR}=300mV_{P-P}	60			MHz	
	F_{RX}	Sine wave	50			MHz	
Input Amplitude	V_{INT}	f_{TX}=50MHz f_{RX}=40MHz	0.3		V_{DD}-0.5	VP-P	
	V_{INR}	Sine wave	0.3		V_{DD}-0.5	VP-P	
Input Current	I_{IH}				300	μA	note 3
Output Current (LD)	I_{OH}	V_{OH}=V_{DD}-0.4V	0.4			mA	
	I_{OL}	V_{OL}=0.4V	0.4			mA	
Input Voltage	V_{IH}		V_{DD}-0.4			V	note 3
	V_{IL}				0.4	V	

note 1. V_{INT}=V_{INR}=300mV_{P-P} Sine wave. F_{TX}=46.930MHz, F_{RX}=39.295MHz
note 2. V_{INR}=300mV_{P-P} Sine wave. V_{RX}=39.295MHz
note 3. BASE, TX_{EN}, D1~D4 (A type)/BASE,TX_{EN} (D Type)

■ TYPICAL CHARACTERISTICS

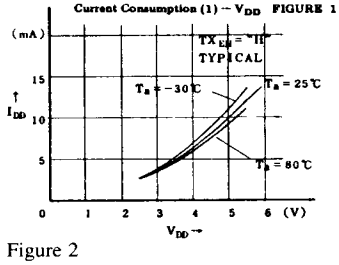


Figure 2

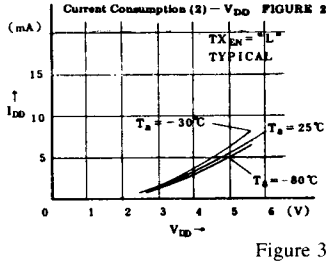


Figure 3

All specifications are subject to change without notice.

U.S. and Canada Distributor

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