CDP68HC68T1

CMOS Serial Real-Time Clock With RAM and Power Sense/Control

August 1997

Features

- **SPI (Serial Peripheral Interface)**
- **Full Clock Features**
  - **Seconds, Minutes, Hours (12/24, AM/PM), Day of Week, Date, Month, Year (0-99), Automatic Leap Year**
- **32 Word x 8-Bit RAM**
- **Seconds, Minutes, Hours Alarm**
- **Automatic Power Loss Detection**
- **Low Minimum Standby (Timekeeping) Voltage . . . 2.2V**
- **Selectable Crystal or 50/60Hz Line Input**
- **Buffered Clock Output**
- **Battery Input Pin that Powers Oscillator and also Connects to V_{DD} Pin When Power Fails**
- **Three Independent Interrupt Modes**
  - **Alarm**
  - **Periodic**
  - **Power-Down Sense**

Description

The CDP68HC68T1 Real-Time Clock provides a time/calendar function, a 32 byte static RAM, and a 3 wire Serial Peripheral Interface (SPI Bus). The primary function of the clock is to divide down a frequency input that can be supplied by the on-board oscillator in conjunction with an external crystal or by an external clock source. The internal oscillator can operate with a 32KHz, 1MHz, 2MHz, or 4MHz crystal. An external clock source with a 32KHz, 1MHz, 2MHz, 4MHz, 50Hz or 60Hz frequency can be used to drive the CDP68HC68T1. The time registers hold seconds, minutes, and hours, while the calendar registers hold day-of-week, date, month, and year information. The data is stored in BCD format. In addition, 12 or 24 hour operation can be selected. In 12 hour mode, an AM/PM indicator is provided. The T1 has a programmable output which can provide one of seven outputs for use elsewhere in the system.

Computer handshaking is controlled with a “wired-OR” interrupt output. The interrupt can be programmed to provide a signal as the result of: 1) an alarm programmed to occur at a predetermined combination of seconds, minutes, and hours; 2) one of 15 periodic interrupts ranging from sub-second to once per day frequency; 3) a power fail detect. The PSE output and the V_{SYS} input are used for external power control. The $\overline{CPUR}$ output is available to reset the processor under power-down conditions. $\overline{CPUR}$ is enabled under software control and can also be activated via the CDP68HC68T1’s watchdog. If enabled, the watchdog requires a periodic toggle of the CE pin without a serial transfer.

Pinouts

CDP68HC68T1 (PDIP, SBDIP, SOIC)
TOP VIEW

CDP68HC68T1 (SOIC)
TOP VIEW

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CDP68HC68T1E	-40 to 85	16 Ld PDIP	E16.3
CDP68HC68T1D	-40 to 85	16 Ld SBDIP	D16.3
CDP68HC68T1M	-40 to 85	20 Ld SOIC	M20.3
CDP68HC68T1M2	-40 to 85	16 Ld SOIC	M16.3
CDP68HC68T1W	-40 to 85	DIE	

NOTE: Pin number references throughout this specification refer to the 16 lead PDIP/SBDIP/SOIC. See pinouts for cross reference.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

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File Number **1547.3**

Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . -0.5V to +7V
Input Voltage, V_{IN} . . . . . V_{SS} -0.3V to V_{DD} +0.3V
Current Drain Per Input Pin Excluding V_{DD} and V_{SS}, I 10mA
Current Drain Per Output Pin, I. 40mA

Operating Conditions

Voltage Range . . . . . +3.0V to +6.0V
Standby (Timekeeping) Voltage . . . . . +2.2V to +6.0V
Temperature Range
CDP68HC68T1D (SBDIP Package) . . . . . -55°C to 125°C
CDP68HC68T1E (PDIP Package) . . . . . -40°C to 85°C
CDP68HC68T1M/M2 (SOIC Packages) . . . . . -40°C to 85°C
Input High Voltage . . . . . (0.7 x V_{DD}) to V_{DD}
Input Low Voltage . . . . . 0V to (0.3 x V_{DD})
Serial Clock Frequency (f_{SCK}) . . . . . +3.0V to +6.0V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld PDIP	90	N/A
16 Ld SOIC	100	N/A
20 Ld SOIC	100	N/A
16 Ld SBDIP	75	24

Maximum Junction Temperature (Hermetic) . . . . . 175°C
Maximum Junction Temperature (Plastic) . . . . . 150°C
Maximum Storage Temperature Range (T_{STG}) . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC, Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Static Electrical Specifications

At T_A = -40°C to +85°C, V_{DD} = V_{BATT} = 5V ±5%, except as noted.

PARAMETER		CONDITIONS		LIMITS CDP68HC68T1 MIN	(NOTE 2) TYP	MAX	UNITS
Quiescent Device Current	I_{DD}			-	1	10	µA
Output Voltage High Level	V_{OH}	I_{OH} = -1.6mA, V_{DD} = 4.5V		3.7	-	-	V
Output Voltage Low Level	V_{OL}	I_{OL} = 1.6mA, V_{DD} = 4.5V		-	-	0.4	V
Output Voltage High Level	V_{OH}	$I_{OH} \leq$ 10µA, V_{DD} = 4.5V		4.4	-	-	V
Output Voltage Low Level	V_{OL}	$I_{OL} \leq$ 10µA, V_{DD} = 4.5V		-	-	0.1	V
Input Leakage Current	I_{IN}			-	-	±1	µA
Three-State Output Leakage Current	I_{OUT}			-	-	±10	µA
Operating Current (Note 3) (I_D + I_B) V_{DD} = V_B = 5V Crystal Operation			32kHz	-	0.08	0.01	mA
			1MHz	-	0.5	0.6	mA
			2MHz	-	0.7	0.84	mA
			4MHz	-	1	1.2	mA
Pin 14 External Clock (Squarewave) (Note 3) (I_D + I_B) V_{DD} = V_S = 5V			32kHz	-	0.02	0.024	mA
			1MHz	-	0.1	0.12	mA
			2MHz	-	0.2	0.24	mA
			4MHz	-	0.4	0.5	mA
Standby Current (Note 3) V_S = 3V Crystal Operation	I_B		32kHz	-	20	25	µA
			1MHz	-	200	250	µA
			2MHz	-	300	360	µA
			4MHz	-	500	600	µA

Static Electrical Specifications At T_A = -40°C to +85°C, V_{DD} = V_{BATT} = 5V ±5%, except as noted. **(Continued)**

PARAMETER	CONDITIONS	LIMITS CDP68HC68T1 MIN	(NOTE 2) TYP		MAX		UNITS
Operating Current (Note 3) V_{DD} = 5V, V_B = 3V Crystal Operation			I_D	I_B	I_D	I_S	mA
	32kHz	-	25	15	30	20	
	1MHz	-	0.08	0.15	0.1	0.18	
	2MHz	-	0.15	0.25	0.18	0.3	
	4MHz	-	0.3	0.4	0.36	0.5	
Standby Current (Note 3) I_B V_B = 2.2V Crystal Operation	32kHz	-	10		12		µA
Input Capacitance C_{IN}	V_{IN} = 0, T_A = 25°C	-	-		2		pF
Maximum Rise and Fall Times t_r, t_f (Except XTAL Input and $\overline{POR}$ Pin 10)		-	-		2		µs
Input Voltage (Line Input Pin Only, Power Sense Mode)		0	10		12		V
V_{SYS} > V_B V_T (For V_B Not Internally Connected to V_{DD})		-	0.7		-		V
Power-On Reset ($\overline{POR}$) Pulse Width		100	75		-		ns

NOTES:

2. Typical values are for T_A = 25°C and nominal V_{DD}.
3. Clock out (Pin 1) disabled, outputs open circuited. No serial access cycles.

Functional Block Diagram

FIGURE 1. REAL TIME CLOCK FUNCTIONAL DIAGRAM

FIGURE 2. ADDRESS MAP

TABLE 1. CLOCK/CALENDAR AND ALARM DATA MODES

ADDRESS LOCATION (H)	FUNCTION	DECIMAL RANGE	BCD DATA RANGE	(NOTE 4) BCD DATE EXAMPLE
20	Seconds	0-59	00-59	18
21	Minutes	0-59	00-59	49
22	Hours 12 Hour Mode (Note 5)	1-12	81-92 (AM) A1-B2 (PM)	A3
	Hours 24 Hour Mode	0-23	00-23	15
23	Day of the Week (Sunday = 1)	1-7	01-07	03
24	Day of the Month (Date)	1-31	01-31	29
25	Month Jan = 1, Dec = 12	1-12	01-12	10
26	Years	0-99	00-99	85
28	Alarm Seconds	0-59	00-59	18
29	Alarm Minutes	0-59	00-59	49
2A	Alarm Hours (Note 6) 12 Hour Mode	1-12	01-12 (AM) 21-32 (PM)	23
	Alarm Hours 24 Hour Mode	0-23	00-23	15

NOTES:

4. Example: 3:49:18, Tuesday. Oct. 29,1985.
5. Most significant Bit, D7, is “0” for 24 hours, and “1” for 12 hour mode. Data Bit D5 is “1” for P.M. and ‘0” for A.M. in 12 hour mode.
6. Alarm hours. Data Bit D5 is “1” for P.M. and “0” for A.M. in 12 hour mode. Data Bits D7 and D6 are DON’T CARE.

Programmers Model - Clock Registers

HEX ADDRESS	WRITE/READ REGISTERS (DB7 … DB0)	NAME
20	TENS 0-5 / UNITS 0-9	SECONDS (00-59)
21	TENS 0-5 / UNITS 0-9	MINUTES (00-59)
22	12 HR 24 / X / PM/AM TENS 0-2 / UNITS 0-9	DB7, 1 = 12 HR., 0 = 24 HR. DB = 1 PM, 0 = AM HOURS (01-12 OR 00-23
23	X X X X / X UNITS 1-7	DAY OF WK (01-07) SUNDAY = 1
24	TENS 0-3 / UNITS 0-9	DATE DAY OF MONTH (01-28, 29, 30, 31)
25	TENS 0-1 / UNITS 0-9	MONTH (01-12) JAN = 1 DEC = 12
26	TENS 0-9 / UNITS 0-9	YEARS (00-99)
31	7 6 5 4 / 3 2 1 0	CONTROL
32	7 6 5 4 / 3 2 1 0	INTERRUPT
	WRITE ONLY REGISTERS	
28	TENS 0-5 / UNITS 0-9	ALARM SECONDS (00-59)
29	TENS 0-5 / UNITS 0-9	ALARM MINUTES (00-59)
2A	X / X / PM/AM TENS 0-2 / UNITS 0-9	ALARM HOURS (01-12 OR 00-23) PLUS AM/PM IN 12 HR. MODE PM = 1, AM = 0
	READ ONLY REGISTERS	
30	7 6 5 4 3 2 1 0	STATUS

RAM DATA BYTE

BIT 7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

HEX ADDRESS 00-1F

NOTE: X = Don't care writes, X = 0 when read.

Functional Description

The SPI real-time clock consists of a clock/calendar and a 32 x 8 RAM. Communications is established via the SPI (Serial Peripheral Interface) bus. In addition to the clock/calendar data from seconds to years, and system flexibility provided by the 32-byte RAM, the clock features computer handshaking with an interrupt output and a separate square-wave clock output that can be one of 7 different frequencies. An alarm circuit is available that compares the alarm latches with the seconds, minutes and hours time counters and activates the interrupt output when they are equal. The clock is specifically designed to aid in power-down/up applications and offers several pins to aid the designer of battery backup systems.

Mode Select

The voltage level that is present at the V_{SYS} input pin at the end of power-on-reset selects the device to be in the single supply or battery backup mode.

Single-Supply Mode

If V_{SYS} is a logic high when power-on-reset is completed, CLK OUT, PSE and $\overline{CPUR}$ will be enabled and the device will be completely operational. $\overline{CPUR}$ will be placed low if the logic level at the V_{SYS} pin goes low. If the output signals CLK OUT, PSE and $\overline{CPUR}$ are disabled due to a power-down instruction, V_{SYS} brought to a logic low and then to a logic high will re-enable these outputs. An example of the single-supply mode is where only one supply is available and V_{DD}, V_{BATT} and V_{SYS} are tied together to the supply.

Battery Backup Mode

If V_{SYS} is a logic low at the end of power-on-reset, CLK OUT, PSE and $\overline{CPUR}$ will be disabled (CLK OUT, PSE and $\overline{CPUR}$ low). This condition will be held until V_{SYS} rises to a threshold (about 0.7V) above V_{BATT}. The outputs CLK OUT, PSE and $\overline{CPUR}$ will then be enabled and the device will be operational. If V_{SYS} falls below a threshold above V_{BATT} the outputs CLK OUT, PSE and $\overline{CPUR}$ will be disabled. An example of battery backup operation occurs if V_{SYS} is tied to V_{DD} and V_{DD} is not connected to a supply when a battery is connected to the V_{BATT} pin. (See Pin Functions, V_{BATT} for Battery Backup Operation.)

Clock/Calendar (See Figure 1 and Figure 2)

The clock/calendar portion of this device consists of a long string of counters that is toggled by a 1Hz input. The 1Hz input is generated by a prescaler driven by an on-board oscillator that utilizes one of four possible external crystals or that can be driven by an external clock source. The 1Hz trigger to the counters can also be supplied by a 50Hz or 60Hz input source that is connected to the LINE input pin.

The time counters offer seconds, minutes and hours data in 12 hour or 24 hour format. An AM/PM indicator is available that once set, toggles every 12 hours. The calendar counters consist of day (day of week), date (day of month), month and years information. Data in the counters is in BCD format. The hours counter utilizes BCD for hour data plus bits for 12/24 hour and AM/PM. The 7 time counters are accessed serially at addresses 20H through 26H. (See Table 1).

RAM

The real-time clock also has a static 32 x 8 RAM that is located at addresses 00-1FH. Transmitting the address/control word with bit-5 low selects RAM access. Bits 0 through 4 select the RAM location.

Alarm

The alarm is set by accessing the three alarm latches and loading the required data. The alarm latches consist of seconds, minutes and hours registers. When their outputs equal the values in the seconds, minutes and hours time counters, an interrupt is generated. The interrupt output will go low if the alarm bit in the Interrupt Control Register is set high. The alarm interrupt bit in the Status Register is set when the interrupt occurs (see Pin Functions, $\overline{INT}$ Pin). To preclude a false interrupt when loading the time counters, the alarm interrupt bit should be set low in the Interrupt Control Register. This procedure is not required when the alarm time is set.

Watchdog Function (See Figure 6)

When bit 7 in the Interrupt Control Register is set high, the Clock's CE (chip enable) pin must be toggled at a regular interval without a serial data transfer. If the CE is not toggled, the clock will supply a CPU reset pulse and bit 6 in the Status Register will be set. Typical service and reset times are listed below.

	50Hz		60Hz		XTAL	
	MIN	MAX	MIN	MAX	MIN	MAX
Service Time	-	10ms	-	8.3ms	-	7.8ms
Reset Time	20	40ms	16.7	33.3ms	15.6	31.3ms

Clock Out

The value in the 3 least significant bits of the Clock Control Register selects one of seven possible output frequencies. (See Clock Control Register). This squarewave signal is available at the CLK OUT pin. When Power-Down operation is initiated, the output is set low.

Control Registers and Status Registers

The operation of the Real-Time Clock is controlled by the Clock Control and Interrupt Control Registers. Both registers are Read-Write Registers. Another register, the Status Register, is available to indicate the operating conditions. The Status Register is a Read only Register.

Power Control

Power control is composed of two operations, Power Sense and Power Down/Up. Two pins are involved in power sensing, the LINE input pin and the $\overline{INT}$ output pin. Two additional pins are utilized during power-down/up operation. They are the PSE (Power Supply Enable) output pin and V_{SYS} input pin.

FIGURE 3. POWER-SENSING FUNCTIONAL DIAGRAM

FIGURE 4. POWER-DOWN FUNCTIONAL DIAGRAM

FIGURE 5. POWER-UP FUNCTIONAL DIAGRAM (INITIATED BY INTERRUPT SIGNAL

Power Sensing (See Figure 3)

When Power Sensing is enabled (Bit 5 = 1 in Interrupt Control Register), AC transitions are sensed at the LINE input pin. Threshold detectors determine when transitions cease. After a delay of 2.68ms to 4.64ms, plus the external input circuit RC time constant, an interrupt is generated and a bit is set in the Status Register. This bit can then be sampled to see if system power has turned back on. See PIN FUNCTIONS, LINE PIN. The power-sense circuitry operates by sensing the level of the voltage presented at the line input pin. This voltage is centered around V_{DD} and as long as it is either plus or minus a threshold (about 1V) from V_{DD} a power-sense failure will not be indicated. With an AC signal present, remaining in this V_{DD} window longer than a minimum of 2.68ms will activate the power-sense circuit. The larger the amplitude of the AC signal, the less time it spends in the V_{DD} window, and the less likely a power failure will be detected. A 60Hz, $10V_{P-P}$ sine-wave voltage is an applicable signal to present at the LINE input pin to setup the power sense function.

Power Down (See Figure 4)

Power down is a processor-directed operation. A bit is set in the Interrupt Control Register to initiate operation. 3 pins are affected. The PSE (Power Supply Enable) output, normally high, is placed low. The CLK OUT is placed low. The $\overline{CPUR}$ output, connected to the processors reset input is also placed low. In addition, the Serial Interface is disabled.

Power Up (See Figure 5 and Figure 6)

Two conditions will terminate the Power-Down mode. The first condition (See Figure 5) requires an interrupt. The interrupt can be generated by the alarm circuit, the programmable periodic interrupt signal, or the power sense circuit.

The second condition that releases Power Down occurs when the level on the V_{SYS} pin rises about 0.7V above the level at the V_{BATT} input, after previously falling to the level of V_{BATT} (See Figure 6) in the Battery Backup Mode or V_{SYS} falls to logic low and returns high in the Single Supply Mode.

FIGURE 6. POWER-UP FUNCTIONAL DIAGRAM (INITIATED BY A RISE IN VOLTAGE ON THE "V_{SYS}" PIN)

CLK OUT

Clock output pin. One of seven frequencies can be selected (or this output can be set low) by the levels of the three LSB's in the Clock-Control Register. If a frequency is selected, it will toggle with a 50% duty cycle except 2Hz in the 50Hz time base mode. (Ex, if 1Hz is selected, the output will be high for 500ms and low for the same period). During power-down operation (bit 6 in Interrupt Control Register set to "1"), the clock-output pin will be set low.

$\overline{\text{CPUR}}$

CPU reset output pin. This pin functions as an N-Channel only, open-drain output and requires an external pull-up resistor.

$\overline{\text{INT}}$

Interrupt output pin. This output is driven from a single NFET pulldown transistor and must be tied to an external pull-up resistor. The output is activated to a low level when:

1. Power-sense operation is selected (B5 = 1 in Interrupt Control Register) and a power failure occurs.
2. A previously set alarm time occurs. The alarm bit in the Status Register and interrupt-out signal are delayed 30.5µs when 32kHz operation is selected and 15.3µs for 2MHz and 7.6µs for 4MHz.
3. A previously selected periodic interrupt signal activates.

The Status Register must be read to set the Interrupt output high after the selected periodic interval occurs. This is also true when conditions 1 and 2 activate the interrupt. If power down had been previously selected, the interrupt will also reset the power-down functions.

SCK, MOSI, MISO

See Serial Peripheral Interface (SPI) section in this data sheet.

CE

A positive chip-enable input. A low level at this input holds the serial interface logic in a reset state. This pin is also used for the watchdog function.

V_{SS}

The negative power-supply pin that is connected to ground.

PSE

Power-supply enable output pin. This pin is used to control power to the system. The pin is set high when:

1. V_{SYS} rises above the V_{BATT} voltage after V_{SYS} was placed low by a system failure.
2. An interrupt occurs.
3. A power-on reset (if V_{SYS} is a logic high).

The PSE pin is set low by writing a high into bit 6 (power-down bit) in the Interrupt Control Register.

$\overline{\text{POR}}$

Power-on reset. A Schmitt-trigger input that generates a power-on internal reset signal using an external R-C network. Both control registers and frequency dividers for the oscillator and line input are reset. The Status Register is reset except for the first time up bit (B4), which is set. Single supply or battery backup operation is selected at the end of POR.

LINE

This input is used for two functions. When not used it should be connected to V_{DD} via a 10kΩ resistor. The first function utilizes the input signal as the frequency source for the timekeeping counters. This function is selected by setting bit 6 in the Clock Control Register. The second function enables the line input to sense a power failure. Threshold detectors operating above and below V_{DD} sense an AC voltage loss. Bit 5 must be set to "1" in the Interrupt Control Register and crystal or external clock source operation is required. Bit 6 in the Clock Control Register must be low to select XTAL operation.

Oscillator Circuit

The CDP68HC68T1 has an on-board 150K resistor that is switched in series with its internal inverter when 32kHz is selected via the Clock Control Register. Note: When first powered up the series resistor is not part of the oscillator circuit. (The CDP68HC68T1 sets up for a 4MHz oscillator).

NOTES:

7. All frequencies recommended oscillator circuit. C1, C2 values crystal dependent.
8. R used for 32KHz operation only. 100K - 300K range as specified by crystal manufacturer.

FIGURE 7. OSCILLATOR CIRCUIT

V_{SYS}

This input is connected to the system voltage. After the CPU initiates power down by setting bit 6 in the Interrupt Control Register to “1”, the level on this pin will terminate power down if it rises about 0.7V above the level at the V_{BATT} input pin after previously falling below V_{BATT} +0.7V. When power down is terminated, the PSE pin will return high and the Clock Output will be enabled. The $\overline{CPUR}$ output pin will also return high. The logic level present at this pin at the end of $\overline{POR}$ determines the CDP68HC68T1’s operating mode.

V_{BATT}

The oscillator power source. The positive terminal of the battery should be connected to this pin. When the level on the V_{SYS} pin falls below V_{BATT} +0.7V, the V_{BATT} pin will be internally connected to the V_{DD} pin. When the voltage on V_{SYS} rises a threshold above (0.7V) the voltage on V_{BATT}, the connection from V_{BATT} to the V_{DD} pin is opened. When the “LINE” input is used as the frequency source, V_{BATT} may be tied to V_{DD} or V_{SS}. The “XTAL IN” pin must be at V_{SS} if V_{BATT} is at V_{SS}. If V_{BATT} is connected to V_{DD}, the “XTAL IN” pin can be tied to V_{SS} or V_{DD}.

XTAL IN, XTAL OUT

These pins are connected to a 32,768Hz. 1.048576MHz, 2.097152MHz or 4.194304MHz crystal. If an external clock is used, it should be connected to “XTAL IN” with ‘XTAL OUT” left open.

V_{DD}

The positive power-supply pin.

Clock Control Register

START-STOP

A high written into this bit will enable the counter stages of the clock circuitry. A low will hold all bits reset in the divider chain from 32Hz to 1Hz. A clock out selected by bits 0, 1 and 2 will not be affected by the stop function except the 1Hz and 2Hz outputs.

LINE-XTAL

When this bit is set high, clock operation will use the 50 or 60-cycle input present at the LINE input pin. When the bit is low, the crystal input will generate the 1Hz time update.

XTAL Select

One of 4 possible crystals is selected by value in these two bits:

0 = 4.194304MHz	2 = 1.048576MHz
1 = 2.097152MHz	3 = 32,768Hz

50-60Hz

50Hz is selected as the line input frequency when this bit is set high. A low will select 60Hz. The power-sense bit in the Interrupt Control Register must be set low for line frequency operation.

Clock Out

The three bits specify one of the 7 frequencies to be used as the squarewave clock output:

0 = XTAL	4 = Disable (low output)
1 = XTAL/2	5 = 1Hz
2 = XTAL/4	6 = 2Hz
3 = XTAL/8	7 = 50Hz or 60Hz
	XTAL Operation = 64Hz

All bits are reset by a power-on reset. Therefore, the XTAL is selected as the clock output at this time.

Interrupt Control Register

Watchdog

When this bit is set high, the watchdog operation will be enabled. This function requires the CPU to toggle the CE pin periodically without a serial-transfer requirement. In the event this does not occur, a CPU reset will be issued. Status Register must be read before re-enabling watchdog.

Power Down

A high in this location will initiate a power down. A CPU reset will occur, the CLK OUT and PSE output pins will be set low and the serial interface will be disabled.

CLOCK CONTROL REGISTER (Write/Read) - Address 31H

D7	D6	D5	D4	D3	D2	D1	D0
START	LINE	XTAL SEL	XTAL SEL	50Hz	CLK OUT	CLK OUT	CLK OUT
$\overline{STOP}$	$\overline{XTAL}$	1	0	$\overline{60}$Hz	2	1	0

Power Sense

This bit is used to enable the line input pin to sense a power failure. It is set high for this function. When power sense is selected, the input to the 50Hz to 60Hz prescaler is disconnected. Therefore, crystal operation is required when power sense is enabled. An interrupt is generated when a power failure is sensed and the power sense and Interrupt True bit in the Status Register are set. When power sense is activated, a “0” must be written to this location followed by a “1” to re-enable power sense.

Alarm

The output of the alarm comparator is enabled when this bit is set high. When a comparison occurs between the seconds, minutes and hours time and alarm counters, the interrupt output is activated. When loading the time counters, this bit should be set low to avoid a false interrupt. This is not required when loading the alarm counters. See Pin Functions, $\overline{\text{INT}}$ for explanation of alarm delay.

Periodic Select

The value in these 4 bits will select the frequency of the periodic output. (See Table 2).

INTERRUPT CONTROL REGISTER (Write/Read) - Address 32H

D7	D6	D5	D4	D3	D2	D1	D0
WATCHDOG	POWER DOWN	POWER SENSE	ALARM	PERIODIC SELECT			

NOTE: All bits are reset by power-on reset.

TABLE 2. PERIODIC INTERRUPT OUTPUT

D0 - D3 VALUE	PERIODIC INTERRUPT OUTPUT FREQUENCY	FREQUENCY TIME BASE	
		XTAL	LINE
0	Disable		
1	2048Hz	X	
2	1024Hz	X	
3	512Hz	X	
4	256Hz	X	
5	128Hz	X	
6	64Hz	X	
	50 or 60Hz		X
7	32Hz	X	
8	16Hz	X	
9	8Hz	X	
10	4Hz	X	
11	2Hz	X	X
12	1Hz	X	X
13	Minute	X	X
14	Hour	X	X
15	Day	X	X

STATUS REGISTER (Read Only) - Address 30H

D7	D6	D5	D4	D3	D2	D1	D0
0	WATCHDOG	TEST MODE	FIRST TIME UP	INTERRUPT TRUE	POWER SENSE INTERRUPT	ALARM INTERRUPT	CLOCK INTERRUPT

TRUTH TABLE

MODE	SIGNAL			
	CE	**SCK** (Note 9)	**MOSI**	**MISO**
DISABLE RESET	L	INPUT DISABLED	INPUT DISABLED	HIGH Z
WRITE	H	CPOL = 1 ↗ ↘ CPOL = 0	DATA BIT LATCH	HIGH Z
READ	H	CPOL = 1 ↘ ↗ CPOL = 0	X	NEXT DATA BIT SHIFTED OUT (Note 10)

NOTES:

9. When interfacing to CDP68HC05 microcontrollers, serial clock phase bit, CPHA, must be set = 1 in the microcomputer's Control Register.
10. MISO remains at a high Z until 8-bits of data are ready to be shifted out during a READ. It remains at a high Z during the entire WRITE cycle.

WATCHDOG

If this bit is set high, the watchdog circuit has detected a CPU failure.

TEST MODE

When this bit is set high, the device is in the TEST MODE.

FIRST-TIME UP

Power-on reset sets this bit high. This signifies that data in the RAM and Clock is not valid and should be initialized.

INTERRUPT TRUE

A high in this bit signifies that one of the three interrupts (Power Sense, Alarm, and Clock) is valid.

POWER-SENSE INTERRUPT

This bit set high signifies that the power-sense circuit has generated an interrupt.

ALARM INTERRUPT

When the seconds, minutes and hours time and alarm counter are equal, this bit will be set high. Status Register must be read before loading Interrupt Control Register for valid alarm indication after alarm activates.

CLOCK INTERRUPT

A periodic interrupt will set this bit high.

All bits are reset by a power-on reset except the "FIRST-TIME UP" which is set. All bits except the power-sense bit are reset after a read of this register.

Pin Signal Description

SCK (Serial Clock Input, Note 11)

This input causes serial data to be latched from the MOSI input and shifted out on the MISO output.

MOSI (Master Out/Slave In, Note 11)

Data bytes are shifted in at this pin, most significant bit (MSB) first.

MISO (Master In/Slave Out)

Data bytes are shifted out at this pin, most significant bit (MSB) first.

CE (Chip Enable, Note 12)

A positive chip-enable input. A low level at this input holds the serial interface logic in a reset state, and disables the output driver at the MISO pin.

NOTES:

11. These inputs will retain their previous state if the line driving them goes into a High-Z state.
12. The CE input has as internal pull down device, if the input is in a low state before going to High Z, the input can be left in a High Z.

Functional Description

The Serial Peripheral Interface (SPI) utilized by the CDP68HC68T1 is a serial synchronous bus for address and data transfers. The clock, which is generated by the micro-computer is active only during address and data transfers. In systems using the CDP68HC05C4 or CDP68HC05D2, the

inactive clock polarity is determined by the CPOL bit in the microcomputer's Control Register. A unique feature of the CDP68HC68T1 is that it automatically determines the level of the inactive clock by sampling SCK when CE becomes active (see Figure 8). Input data (MOSI) is latched internally on the internal strobe edge and output data (MISO) is shifted out on the shift edge, as defined by Figure 8. There is one clock for each data bit transferred (address, as well as data bits are transferred in groups of 8).

NOTE: "CPOL" is a bit that is set in the microcomputer's Control Register.

FIGURE 8. SERIAL RAM CLOCK (SCK) AS A FUNCTION OF MCU CLOCK POLARITY (CPOL)

Address And Data Format

There are three types of serial transfer:

1. Address Control - Figure 9.
2. READ or WRITE Data - Figure 10.
3. Watchdog Reset (actually a non-transfer) Figure 11.

The Address/Control and Data bytes are shifted MSB first, Into the serial data input (MOSI) and out of the serial data output (MISO).

Any transfer of data requires an Address/Control byte to specify a Write or Read operation and to select a Clock or RAM location, followed by one or more bytes of data.

Data is transferred out of MISO for a Read and into MOSI for a Write operation.

Address/Control Byte - Figure 9

It is always the first byte received after CE goes true. To transmit a new address, CE must first go false and then true again. Bit 5 is used to select between Clock and RAM locations.

BIT →	7	6	5	4	3	2	1	0
↓	W/$\overline{R}$	0	CLK $\overline{RAM}$	A4	A3	A2	A1	A0
04		A0-A4		Selects 5-Bit HEX Address of RAM or specifies Clock Register. Most Significant Address Bit. If equal to "1", A0 through A4 selects a Clock Register. If equal to "0", A0 through A4 selects one of 32 RAM locations. Must be set to "0" when not in Test Mode 7W/R W/R = "1" initiates one or more WRITE cycles.W/R = "0", initiates one or more READ cycles.				
5		CLK $\overline{RAM}$						
6		0						
7		W/R						

NOTE: SCK can be either polarity.

FIGURE 9. ADDRESS/CONTROL BYTE-TRANSFER WAVEFORMS

Read/Write Data (See Figure 10)

Read/Write data follows the Address/Control byte.

NOTE: SCK can be either polarity.

FIGURE 10. READ/WRITE DATA TRANSFER WAVEFORMS

Watchdog Reset - (See Figure 11)

When watchdog operation is selected, CE must be toggled periodically or a CPU reset will be outputted.

FIGURE 11. WATCHDOG OPERATION WAVEFORMS

Address And Data

Data transfers can occur one byte at a time (Figure 12) or in a multibyte burst mode (Figure 13). After the Real-Time Clock enabled, an Address/Control word is sent to set the CLOCK or RAM and select the type of operation (i.e., Read or Write). For a single-byte Read or Write, one byte is transferred to or from the Clock Register or RAM location specified in the Address/Control byte and the Real-Time Clock is then disabled. Write cycle causes the latched Clock Register or RAM address to automatically increment. Incrementing continues after each transfer until the device is disabled. After incrementing to 1FH the address will “wrap” to 00H and continue. Therefore, when the RAM is selected the address will “wrap” to 00H and when the clock is selected the address will “wrap” 20H.

FIGURE 12. SINGLE-BYTE TRANSFER WAVEFORMS

FIGURE 13. MULTIPLE-BYTE TRANSFER WAVEFORMS

Dynamic Electrical Specifications Bus Timing V_{DD} ±10%, V_{SS} = 0V_{DC}, T_A = 40^oC to 85^oC

IDENT. NO	PARAMETER		LIMITS (ALL TYPES)				UNITS
			V_{DD} = 3.3V		V_{DD} = 5V		
			MIN	MAX	MIN	MAX	
1	Chip Enable Setup Time	t_{EVCV}	200	-	100	-	ns
2	Chip Enable After Clock Hold Time	t_{CVEX}	250	-	125	-	ns
3	Clock Width High	t_{WH}	400	-	200	-	ns
4	Clock Width Low	t_{WL}	400	-	200	-	ns
5	Data In to Clock Setup Time	t_{DVCV}	200	-	100	-	ns
7	Clock to Data Propagation Delay	t_{CVDV}	-	200	-	100	ns
8	Chip Disable to Output High Z	t_{EXQZ}	-	200	-	100	ns
11	Output Rise Time	t_r	-	200	-	100	ns
12	Output Fall Time	t_f	-	200	-	100	ns
A	Data in After Clock Hold Time	t_{CVDX}	200	-	100	-	ns
B	Clock to Data Out Active	t_{CVQX}	-	200	-	100	ns
C	Clock Recovery Time	t_{REC}	200	-	200	-	ns

Timing Diagrams

FIGURE 14. WRITE-CYCLE TIMING WAVEFORMS

FIGURE 15. READ-CYCLE TIMING WAVEFORMS

System Diagrams

NOTE: Example of a system in which power is always on. Clock circuit driven by line input frequency.

FIGURE 16. POWER-ON ALWAYS SYSTEM DIAGRAM

System Diagrams (Continued)

NOTE: Example of a system in which the power is controlled by an external source. The LINE input pin can sense when the switch opens by use of the POWER-SENSE INTERRUPT. The CDP68HC68T1 crystal drives the clock input to the CPU using the CLK OUT pin. On power down when $V_{SYS} < V_{BATT} + 0.7V$. V_{BATT} will power the CDP68HC68T1. A threshold detect activates a P-Channel switch, connecting V_{BATT} to V_{DD}. V_{BATT} always supplies power to the oscillator, keeping voltage frequency variation to a minimum.

FIGURE 17. EXTERNALLY CONTROLLED POWER SYSTEM DIAGRAM

A Procedure for Power-Down Operation might consist of the following:

1. Set power sense operation by writing bit 5 high in the Interrupt Control Register.
2. When an interrupt occurs, the CPU reads the Status Register to determine the interrupt source.
3. Sensing a power failure, the CPU does the necessary housekeeping to prepare for shutdown.
4. The CPU reads the Status Register again after several milliseconds to determine validity of power failure.
5. The CPU sets power-down bit 6 and disables all interrupts in the Interrupt Control Register when power down is verified. This causes the CPU reset and clock out to be held low and disconnects the serial interface.
6. When power returns and V_{SYS} rises above V_{BATT}, power down is terminated. The CPU reset is released and serial communication is established.

System Diagrams (Continued)

FIGURE 18. EXAMPLE OF A SYSTEM WITH A BATTERY BACKUP

System Diagrams (Continued)

Example of an automotive system. The V_{SYS} and LINE inputs can be used to sense the ignition turning on and off. An external switch is included to activate the system without turning on the ignition. Also, the CMOS CPU is not powered down with the system V_{DD}, but is held in a low power reset mode during power down. When restoring power the CDP68HC68T1 will enable the CLK OUT pin and set the PSE and $\overline{CPUR}$ high.

Important Application Note: Those units with a code of 6PG have delayed alarm interrupts of 8.3ms regardless of CDP68HC68T1's operating frequency. (See Pin Functions, INT.) In addition, reading the Status Register before delayed alarm activates will disable alarm signal.

FIGURE 19. AUTOMOTIVE SYSTEM DIAGRAM

Dual-In-Line Plastic Packages (PDIP)

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 **(JEDEC MS-001-BB ISSUE D)**
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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Ceramic Dual-In-Line Metal Seal Packages (SBDIP)

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D16.3 **MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)**
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

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Small Outline Plastic Packages (SOIC)

M16.3 **(JEDEC MS-013-AA ISSUE C)**
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)

M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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