

PRELIMINARY

**THC63LVDM63A/THC63LVDF64A**

**85MHz LVDS 18 Bit COLOR  
HOST-LCD PANEL INTERFACE**

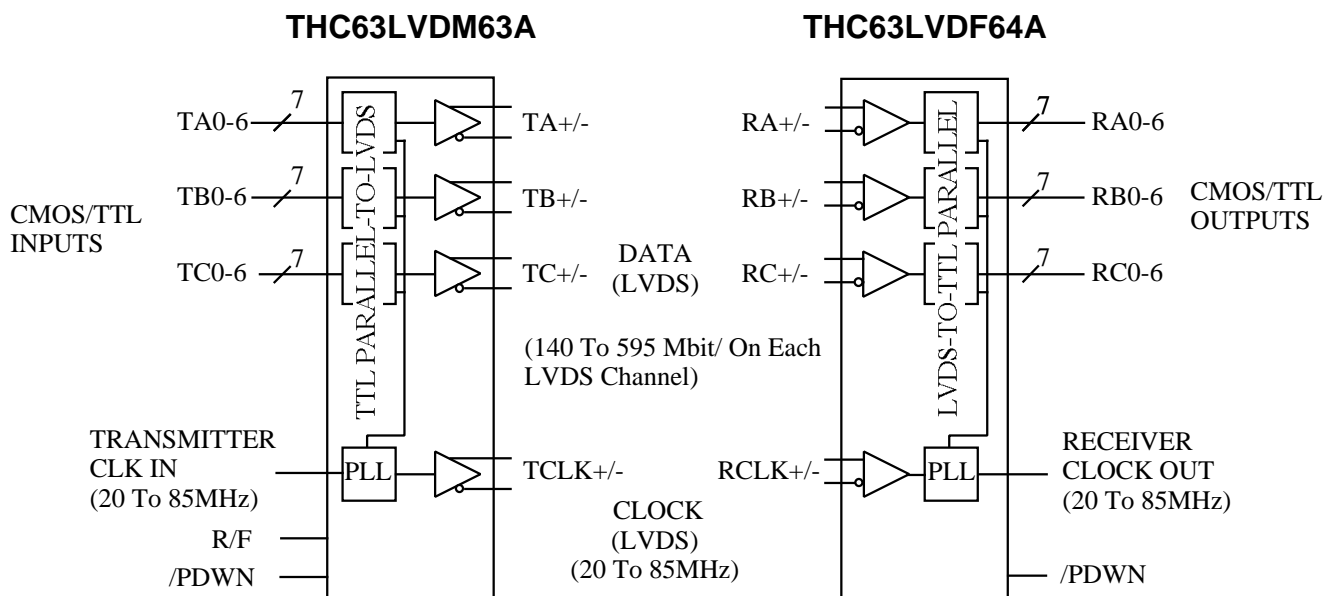
**General Description**

The THC63LVDM63A transmitter converts 21 bits of CMOS/TTL data into LVDS(Low Voltage Differential Signaling) data stream. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. The THC63LVDM63A can be programmed for rising edge or falling edge clocks through a dedicated pin.

The THC63LVDF64A receiver convert the LVDS data streams back into 21 bits of CMOS/TTL data with falling edge clock. At a transmit clock frequency of 85MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (HSYNC, VSYNC, CNTL1) are transmitted at a rate of 595 Mbps per LVDS data channel.

**Features**

- 21:3 Data channel compression at up to 223 Megabytes per sec throughput
- Wide Frequency Range: 20 - 85 MHz suited for VGA,SVGA,XGA and SXGA
- Narrow bus (8 lines) reduces cable size
- 345mV swing LVDS devices for Low EMI
- Supports Spread Spectrum Clock Generator
- On chip Input Jitter Filtering
- PLL requires No External Components
- Single 3.3V supply with 110mW(TYP)
- Low Power CMOS Design
- Power-Down Mode
- Low profile 48 Lead TSSOP Package
- Clock Edge Programmable for Transmitter
- Improved Replacement for the National DS90CF363/364



**OPTIONS**

CLOCK TRIGGERING	TRANSMITTER DEVICE	RECEIVER DEVICE
Falling Edge	<b>THC63LVDM63A(R/F pin=GND)</b>	<b>THC63LVDF64A</b>
Rising Edge	<b>THC63LVDM63A(R/F pin=Vcc)</b>	----

# PIN OUT

## TRANSMITTER DEVICE THC63LVDM63A

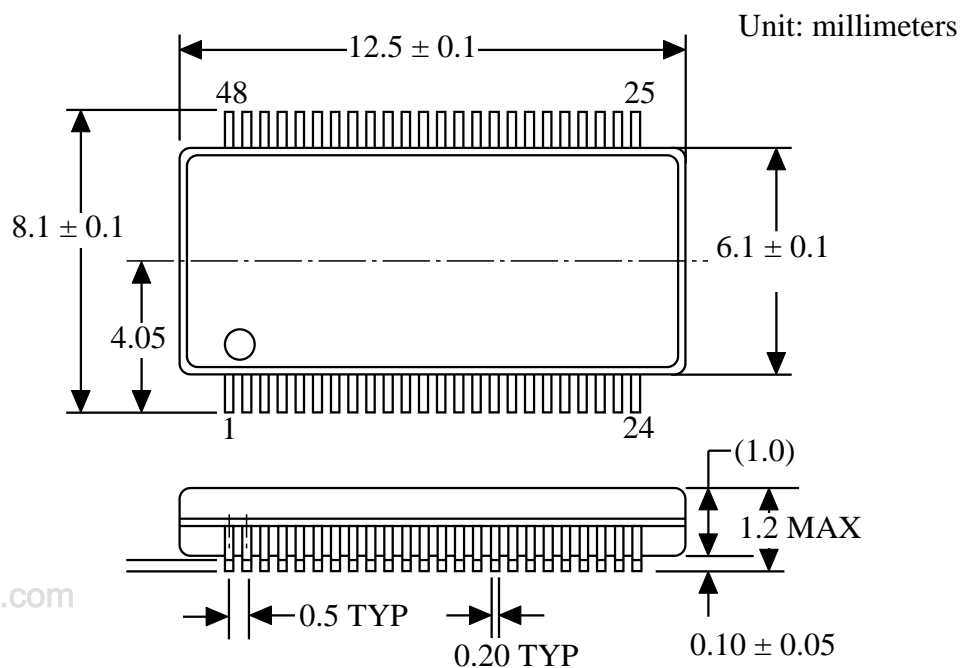
TA4	1	48	TA3
VCC	2	47	TA2
TA5	3	46	GND
TA6	4	45	TA1
GND	5	44	TA0
TB0	6	43	N/C
TB1	7	42	LVDS GND
VCC	8	41	TA-
TB2	9	40	TA+
TB3	10	39	TB-
GND	11	38	TB+
TB4	12	37	LVDS VCC
TB5	13	36	LVDS GND
R/F	14	35	TC-
TB6	15	34	TC+
TC0	16	33	TCLK-
GND	17	32	TCLK+
TC1	18	31	LVDS GND
TC2	19	30	PLL GND
TC3	20	29	PLL VCC
VCC	21	28	PLL GND
TC4	22	27	/PDWN
TC5	23	26	CLK IN
GND	24	25	TC6

## RECEIVER DEVICE THC63LVDF64A

RC3	1	48	VCC
RC4	2	47	RC2
GND	3	46	RC1
RC5	4	45	RC0
RC6	5	44	GND
N/C	6	43	RB6
LVDS GND	7	42	VCC
RA-	8	41	RB5
RA+	9	40	RB4
RB-	10	39	RB3
RB+	11	38	GND
LVDS VCC	12	37	RB2
LVDS GND	13	36	VCC
RC-	14	35	RB1
RC+	15	34	RB0
RCLK-	16	33	RA6
RCLK+	17	32	GND
LVDS GND	18	31	RA5
PLL GND	19	30	RA4
PLL VCC	20	29	RA3
PLL GND	21	28	VCC
/PDWN	22	27	RA2
CLKOUT	23	26	RA1
RA0	24	25	GND

# PACKAGE

48 Lead Molded Thin Shrink Small Outline Package, JEDEC



## Electrical Characteristics

$V_{CC} = 3.0 - 3.6V$ ,  $T_a = -10 - +70\text{ }^\circ\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
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### CMOS/TTL DC SPECIFICATIONS

$V_{IH}$	High Level Input Voltage		2.0		$V_{CC}$	V
$V_{IL}$	Low Level Input Voltage		GND		0.8	V
$V_{OH}$	High Level output Voltage	$I_{OH} = -4mA$	2.4			V
$V_{OL}$	Low Level Output Voltage	$I_{OL} = 4mA$			0.4	V
$I_{IN}$	Input Current	$0V \leq V_{IN} \leq V_{CC}$			$\pm 10$	$\mu A$
$I_{PD}$	Pull Down Current	R/F pin, $V_{IH} = V_{CC}$			100	$\mu A$
$I_{OS}$	Output Short Circuit Current	$V_{OUT} = 0V$			-50	$\mu A$

### LVDS DRIVER DC SPECIFICATIONS

$V_{OD}$	Differential Output Voltage	RL=100	250	350	450	mV
$V_{OD}$	Change in VOD between Complimentary Output States				35	mV
$V_{OC}$	Common Mode Voltage		1.125	1.25	1.375	V
$V_{OC}$	Change in VOC between Complimentary Output States				35	mV
$I_{OS}$	Output Short Circuit Current	$V_{OUT} = 0V, RL = 100$			-24	mA
$I_{OZ}$	Output TRI-STATE Current	/PDWN=0V, $V_{OUT} = 0V$ to $V_{CC}$			$\pm 10$	$\mu A$

### LVDS RECEIVER DC SPECIFICATIONS

$V_{TH}$	Differential Input High Threshold	$V_{OC} = +1.2V$			+100	mV
$V_{TL}$	Differential Input low Threshold		-100			mV
$I_{IN}$	Input Current	$V_{IN} = +2.4V / 0V$ $V_{CC} = 3.6V$			$\pm 10$	$\mu A$

### Absolute Maximum Ratings (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.3 to +4V
CMOS/TTL Input Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
CMOS/TTL Output Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Receiver Input Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Driver Output Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
Output Short Circuit Duration	continuous
Junction Temperature	+150 $^\circ\text{C}$
Storage Temperature Range	-65 $^\circ\text{C}$ to 150 $^\circ\text{C}$
Lead Temperature(Soldering, 4 sec.)	+260 $^\circ\text{C}$
Maximum Power Dissipation @25 $^\circ\text{C}$	1.4W

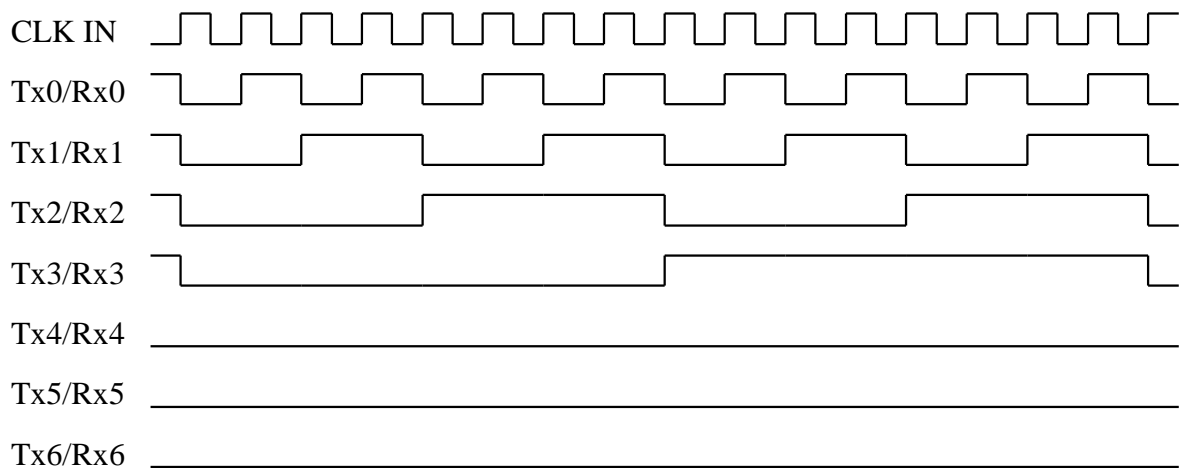
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not ment to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

**Supply Current**

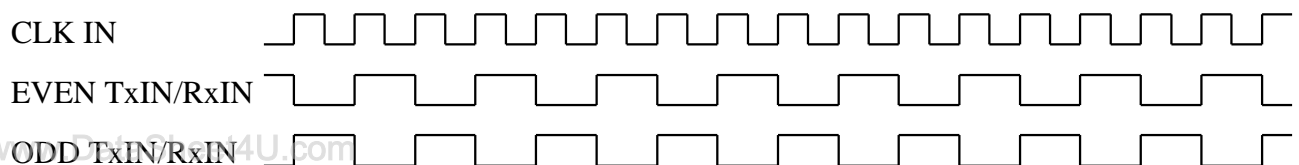
V<sub>cc</sub> = 3.0 - 3.6V, Ta = -10 - +70 °C

SYMBOL	PARAMETER	CONDITIONS	TYP	MAX	UNITS	
I <sub>TCCG</sub>	Transmitter Supply Current	RL=100 Ω, CL=5pF, V <sub>cc</sub> =3.3V, 16 Grayscale Pattern	f=65MHz	33	41	mA
			f=85MHz	37	45	mA
I <sub>TCCW</sub>	Transmitter Supply Current	RL=100 Ω, CL=5pF, V <sub>cc</sub> =3.3V, Worst Case Pattern	f=65MHz	35	43	mA
			f=85MHz	39	47	mA
I <sub>TCCS</sub>	Transmitter Power Down Supply Current	/PDWN =0 V		10	μA	
I <sub>RCCG</sub>	Receiver Supply Current	CL=8pF, V <sub>cc</sub> =3.3V, 16 Grayscale Pattern	f=65MHz	33	43	mA
			f=85MHz	44	54	mA
I <sub>RCCW</sub>	Receiver Supply Current	CL=8pF, V <sub>cc</sub> =3.3V, Worst Case Pattern	f=65MHz	58	75	mA
			f=85MHz	70	87	mA
I <sub>RCCS</sub>	Receiver Power Down Supply Current	/PDWN =0 V		10	μA	

**16 Grayscale Pattern**



**Worst Case Pattern**



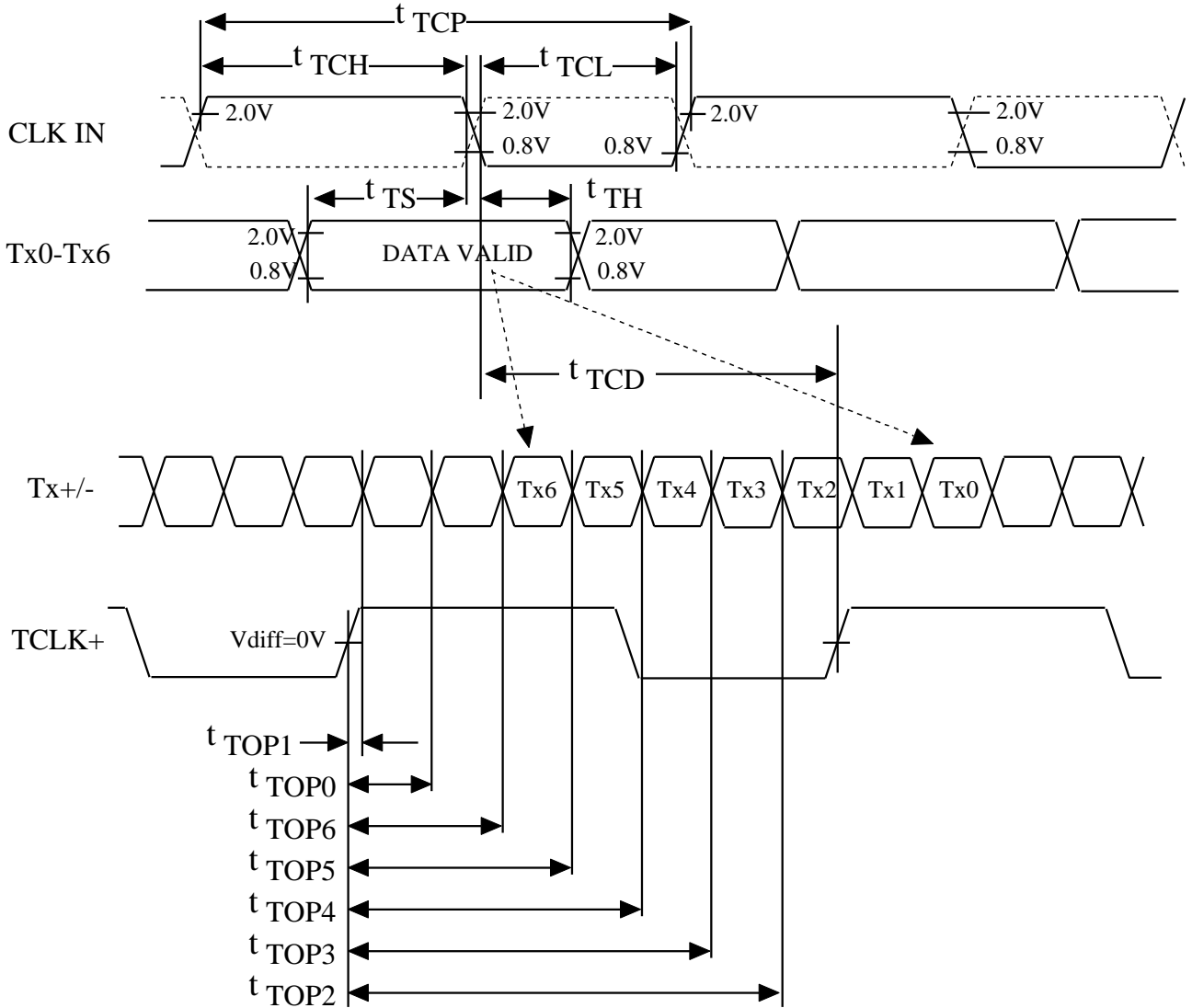
## Switching Characteristics

V<sub>CC</sub> = 3.0 - 3.6V, T<sub>a</sub> = -10 - +70 °C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
<b>TRANSMITTER</b>					
t <sub>TCIT</sub>	CLK IN Transition Time			5.0	ns
t <sub>TCP</sub>	CLK IN Period	11.76	T	50.0	ns
t <sub>TCH</sub>	CLK IN High Time	0.35T	0.5T	0.65T	ns
t <sub>TCL</sub>	CLK IN Low Time	0.35T	0.5T	0.65T	ns
t <sub>TCD</sub>	CLK IN to TCLK+/- Delay		2T/7		ns
t <sub>TS</sub>	TTL Data Setup to CLK IN	2.5			ns
t <sub>TH</sub>	TTL Data Hold from CLK IN	2.5			ns
t <sub>LVT</sub>	LVDS Transition Time		0.6	1.5	ns
t <sub>TOP1</sub>	Output Data Position 0 (T=11.76ns)	-0.2	0.0	0.2	ns
t <sub>TOP0</sub>	Output Data Position 1 (T=11.76ns)	T/7-0.2	T/7	T/7+0.2	ns
t <sub>TOP6</sub>	Output Data Position 2 (T=11.76ns)	2T/7-0.2	2T/7	2T/7+0.2	ns
t <sub>TOP5</sub>	Output Data Position 3 (T=11.76ns)	3T/7-0.2	3T/7	3T/7+0.2	ns
t <sub>TOP4</sub>	Output Data Position 4 (T=11.76ns)	4T/7-0.2	4T/7	4T/7+0.2	ns
t <sub>TOP3</sub>	Output Data Position 5 (T=11.76ns)	5T/7-0.2	5T/7	5T/7+0.2	ns
t <sub>TOP2</sub>	Output Data Position 6 (T=11.76ns)	6T/7-0.2	6T/7	6T/7+0.2	ns
t <sub>TPLL</sub>	Phase Lock Loop Set			10.0	ms
<b>RECEIVER</b>					
t <sub>RCP</sub>	CLK OUT Period	11.76	T	50.0	ns
t <sub>RCH</sub>	CLK OUT High Time		4T/7		ns
t <sub>RCL</sub>	CLK OUT Low Time		3T/7		ns
t <sub>RCD</sub>	RCLK+/- to CLK OUT Delay		5T/7		ns
t <sub>RS</sub>	TTL Data Setup to CLK OUT	3T/7-2.5			ns
t <sub>RH</sub>	TTL Data Hold from CLK OUT	4T/7-3.5			ns
t <sub>TLH</sub>	TTL Low to High Transition Time		3.0	5.0	ns
t <sub>THL</sub>	TTL High to Low Transition Time		3.0	5.0	ns
t <sub>RIP1</sub>	Input Data Position 0 (T=11.76ns)	-0.4	0.0	0.4	ns
t <sub>RIP0</sub>	Input Data Position 1 (T=11.76ns)	T/7-0.4	T/7	T/7+0.4	ns
t <sub>RIP6</sub>	Input Data Position 2 (T=11.76ns)	2T/7-0.4	2T/7	2T/7+0.4	ns
t <sub>RIP5</sub>	Input Data Position 3 (T=11.76ns)	3T/7-0.4	3T/7	3T/7+0.4	ns
t <sub>RIP4</sub>	Input Data Position 4 (T=11.76ns)	4T/7-0.4	4T/7	4T/7+0.4	ns
t <sub>RIP3</sub>	Input Data Position 5 (T=11.76ns)	5T/7-0.4	5T/7	5T/7+0.4	ns
t <sub>RIP2</sub>	Input Data Position 6 (T=11.76ns)	6T/7-0.4	6T/7	6T/7+0.4	ns
t <sub>RPLL</sub>	Phase Lock Loop Set			10	ms

# AC TIMING DIAGRAMS

## TRANSMITTER DEVICE

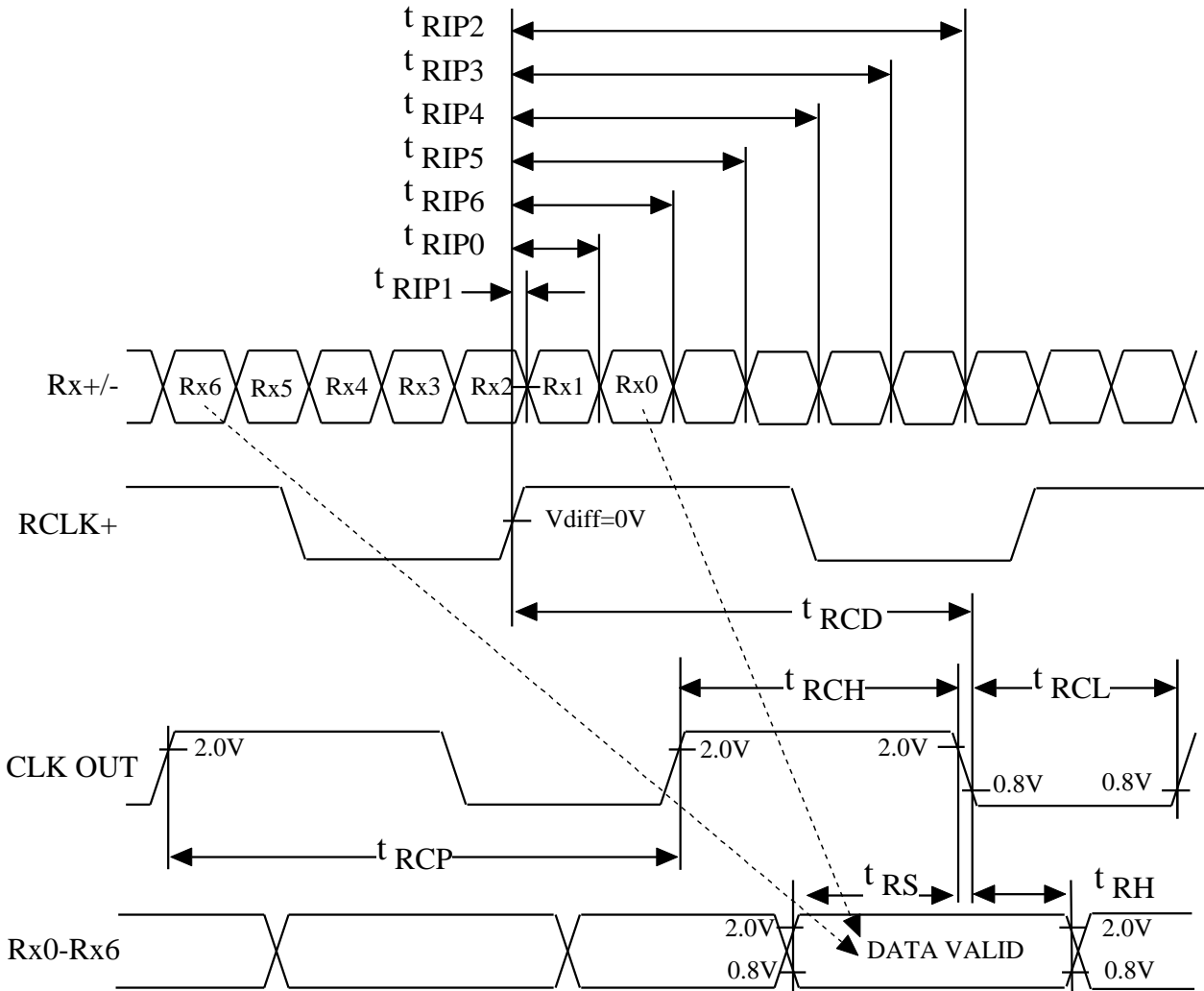


Note:

- 1) CLK IN: for THC63LVDM63A(R/F=GND), denoted as solid line,  
for THC63LVDM63A(R/F=Vcc), denoted as dashed line
- 2)  $V_{diff} = (TA+) - (TA-), \dots (TCLK+) - (TCLK-)$

# AC TIMING DIAGRAMS

## RECEIVER DEVICE



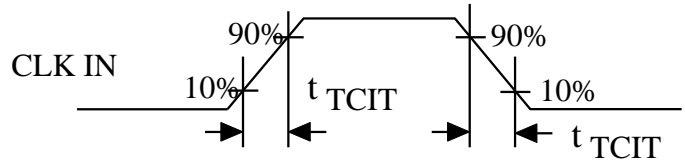
Note:

- 1)  $V_{diff} = (RA+) - (RA-), \dots (RCLK+) - (RCLK-)$

# AC TIMING DIAGRAMS

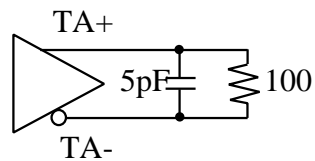
## TRANSMITTER DEVICE TRANSITION TIMES

### TTL Input

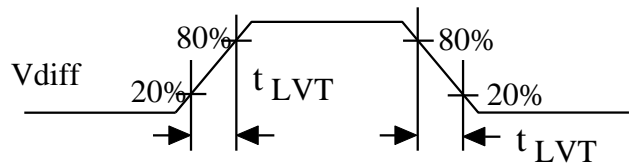


### LVDS Output

$$V_{diff} = (TA+) - (TA-)$$

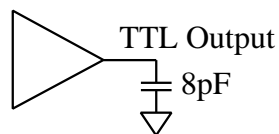


### LVDS output load

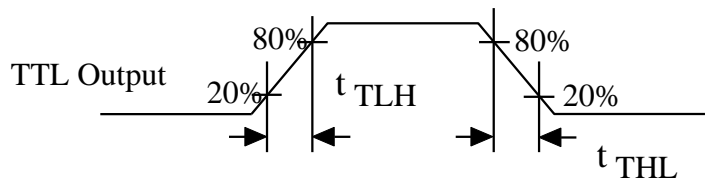


## RECEIVER DEVICE TRANSITION TIMES

### TTL Output

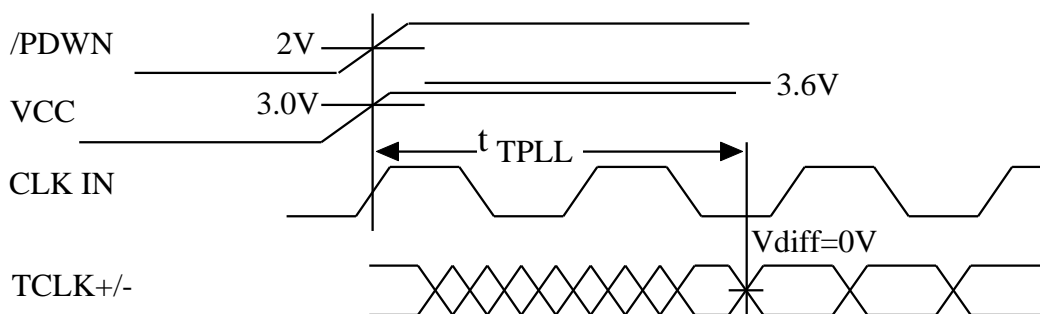


### TTL output load

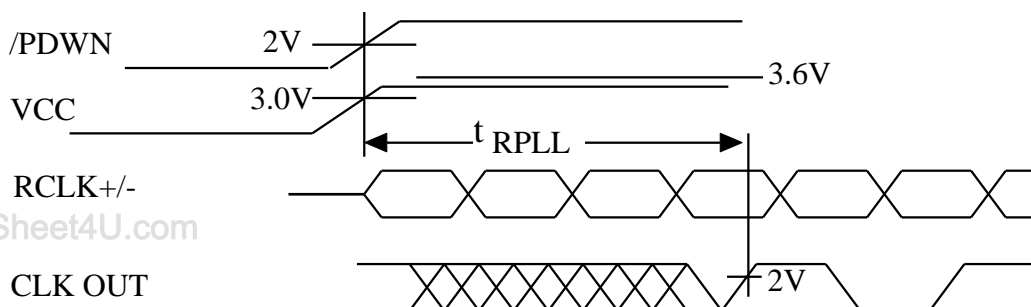


## PHASE LOCK LOOP SET TIME

### TRANSMITTER DEVICE



### RECEIVER DEVICE





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**THine**

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