Nios II

For other uses of "NIOS", see Nios (disambiguation).

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Nios II	
Designer	Altera
Bits	32-bit
Design	RISC
Endianness	Little-Endian
Open	No
Registers	
General purpose	32

Nios II is a 32-bit embedded-processor architecture designed specifically for the Altera family of field-programmable gate array (FPGA) integrated circuits. Nios II incorporates many enhancements over the original Nios architecture, making it more suitable for a wider range of embedded computing applications, from digital signal processing (DSP) to system-control.

Nios II is a successor to Altera's first configurable 16-bit embedded processor Nios.

Contents

Key features

Like the original Nios, the Nios II architecture is a RISC soft-core architecture which is implemented entirely in the programmable logic and memory blocks of Altera FPGAs. The soft-core nature of the Nios II processor lets the system designer specify and generate a custom Nios II core, tailored for his or her specific application requirements. System designers can extend the Nios II's basic functionality by adding a predefined memory management unit, or defining custom instructions and custom peripherals.

Custom instructions

Similar to native Nios II instructions, user-defined instructions accept values from up to two 32-bit source registers and optionally write back a result to a 32-bit destination register. By using custom instructions, the system designers can fine-tune the system hardware to meet performance goals and also the designer can easily handle the instruction as a macro in C.

Custom peripherals

For performance-critical systems that spend most CPU cycles executing a specific section of code, a user-defined peripheral can potentially offload part or all of the execution of a software-algorithm to user-defined hardware logic, improving power-efficiency or application throughput.

Memory Management Unit

Introduced with Quartus 8.0, the optional MMU enables Nios II to run operating systems which require hardware-based paging and protection, such as the Linux kernel. Without an MMU, Nios is restricted to operating systems which use a simplified protection and virtual memory-model: e.g., µClinux and FreeRTOS.

Memory Protection Unit

Introduced with Quartus 8.0, the optional MPU provides memory protection similar to that provided by an MMU but with a simpler programming model and without the performance overhead associated with an MMU.

Nios II CPU family

Nios II classic is offered in 3 different configurations: Nios II/f (fast), Nios II/s (standard), and Nios II/e (economy). Nios II gen2 is offered in 2 different configurations: Nios II/f (fast), and Nios II/e (economy).

Nios II/f

The Nios II/f core is designed for maximum performance at the expense of core size. Features of Nios II/f include:

- Separate instruction and data caches (512 B to 64 kB)
- Optional MMU or MPU
- Access to up to 2 GB of external address space
- Optional tightly coupled memory for instructions and data
- Six-stage pipeline to achieve maximum DMIPS/MHz
- Single-cycle hardware multiply and barrel shifter
- Optional hardware divide option
- Dynamic branch prediction
- Up to 256 custom instructions and unlimited hardware accelerators
- JTAG debug module
- Optional JTAG debug module enhancements, including hardware breakpoints, data triggers, and real-time trace

Nios II/s

Nios II/s core is designed to maintain a balance between performance and cost. Features of Nios II/s include:

- Instruction cache
- Up to 2 GB of external address space
- Optional tightly coupled memory for instructions
- Five-stage pipeline
- Static branch prediction
- Hardware multiply, divide, and shift options
- Up to 256 custom instructions
- JTAG debug module
- Optional JTAG debug module enhancements, including hardware breakpoints, data triggers, and real-time trace

Nios II/e

The Nios II/e core is designed for smallest possible logic utilization of FPGAs. This is especially efficient for low-cost Cyclone II FPGA applications. Features of Nios II/e include:

- Up to 2 GB of external address space

- JTAG debug module
- Complete systems in fewer than 700 LEs
- Optional debug enhancements
- Up to 256 custom instructions
- Free, no license required

Avalon switch fabric interface

Nios II uses the Avalon switch fabric as the interface to its embedded peripherals. Compared to a traditional bus in a processor-based system, which lets only one bus master access the bus at a time, the Avalon switch fabric, using a slave-side arbitration scheme, lets multiple masters operate simultaneously.

Development processes

Development for Nios II consists of two separate steps: hardware generation and software creation.

Development is hosted inside an Altera application called the Embedded Design Suite (EDS). The EDS contains a complete integrated development environment to manage both hardware and software in two separate steps:

Hardware generation process

Nios II hardware designers use the Qsys system integration tool, a component of the Quartus-II package, to configure and generate a Nios system. The configuration graphical user interface (GUI) allows users to choose the Nios-II's feature-set, and to add peripheral and I/O-blocks (timers, memory-controllers, serial interface, etc.) to the embedded system. When the hardware specification is complete, Quartus-II performs the synthesis, place & route to implement the entire system on the selected FPGA target.
Qsys is replacing the older SOPC (System-on-a-Programmable-Chip) Builder, which could also be used to build a Nios II system, and is being recommended for new projects.[1]

Software creation process

A separate package, called the Embedded Design Suite (EDS), manages the software development. Based on the Eclipse IDE, the EDS includes a C/C++ compiler (based on the GNU toolchain), debugger, and an instruction-set simulator. EDS allows programmers to test their application in simulation, or download and run their compiled application on the actual FPGA host.

Because the C/C++ development-chain is based on GCC, the vast majority of open source software for Linux compiles and runs with minimal or no modification. Third-party operating-systems have also been ported to Nios II. These include Micrium MicroC/OS-II, eCos, Segger Microcontroller embOS, ChibiOS/RT, µCLinux and FreeRTOS.

Licensing

Nios II is comparable to MicroBlaze, a competing softcore CPU for the Xilinx family of FPGA. Unlike MicroBlaze, Nios II is licensable for standard-cell ASICs through a third-party IP provider, Synopsys Designware. Through the Designware license, designers can port Nios-based designs from an FPGA-platform to a mass production ASIC-device.