EV8AQ160
QUAD ADC
Datasheet DS0846

MAIN FEATURES

- Quad ADC with 8-bit Resolution
  - 1.25 Gsps Sampling Rate in Four-channel Mode
  - 2.5 Gsps Sampling Rate in Two-channel Mode
  - 5 Gsps Sampling Rate in One-channel Mode
  - Built-in four-by-four Crosspoint Switch
- 2.5 GHz Differential Symmetrical Input Clock Required
- ADC Master Reset (LVDS)
- Double Data Rate Output Protocol
- LVDS Output Format
- Digital Interface (SPI) with Reset Signal
  - Selectable 1:1 or 1:2 Demultiplexed Outputs
  - Channel Mode Selection
  - 500 mVpp or 625 mVpp Analog Input (Differential AC or DC Coupled)
  - Selectable Bandwidth (Four Available Settings)
  - Gain Control (±18%)
  - Offset Control (±50 mV)
  - Phase Control (±14 ps Range)
  - Standby Mode (Full or Partial)
  - Binary or Gray Coding Selection
  - Test Mode
- Power Supplies: 3.3V and 1.8V (Outputs), 1.8V (Digital)
- Power Dissipation: 4.2W Total (1:1 DMUX Mode)
- EBGA380 Package (RoHS, 1.27 mm Pitch)

PERFORMANCE

- Selectable Full Power Input Bandwidth (–3 dB) up to 2 GHz (4-/2-/1-channel modes)
- Channel-to-channel Isolation: >60 dB
- Four-channel Mode (Fsampling = 1.25 Gsps, –1 dBFS)
  - Fin = 100 MHz: ENOB = 7.5 bit, SFDR = 58 dBc, SNR = 46.5 dBc, DNL = ±0.18 LSB, INL = ±0.4 LSB
  - Fin = 620 MHz: ENOB = 7.3 bit, SFDR = 56 dBc, SNR = 45 dBc
- Two-channel Mode (Fsampling = 2.5 Gsps, –1 dBFS)
  - Fin = 100 MHz: ENOB = 7.5 bit, SFDR = 58 dBc, SNR = 46 dBc, DNL = ±0.14 LSB, INL = ±0.35 LSB
  - Fin = 620 MHz: ENOB = 7.2 bit, SFDR = 56 dBc, SNR = 44.5 dBc
- One-Channel Mode (Fsampling = 5 Gsps, Fin = 100 MHz, –1 dBFS)
  - Fin = 100 MHz: ENOB = 7.4 bit, SFDR = 58 dBc, SNR = 46 dBc, DNL = ±0.12 LSB, INL = ±0.27 LSB
  - Fin = 620 MHz: ENOB = 7.1 bit, SFDR = 56 dBc, SNR = 44 dBc
- BER: 10^{-16} at Full Speed

SCREENING

- Temperature Range for Packaged Device
- Commercial *C* Grade: 0°C < T_{amb} < 70°C

Applications

- High-speed Oscilloscopes

e2v technologies (uk) limited, Waterhouse Lane, Chelmsford, Essex CM1 2QU United Kingdom Holding Company: e2v technologies plc

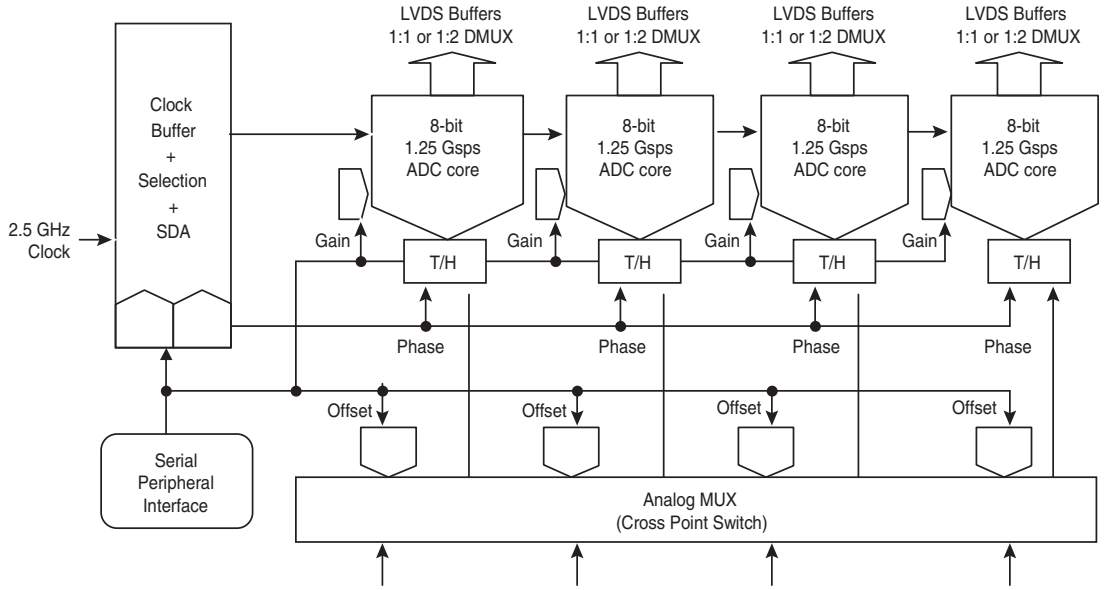
Telephone: +44 (0)1245 493493 Facsimile: +44 (0)1245 492492

Contact e2v by e-mail: enquiries@e2v.com or visit www.e2v.com for global sales and operations centres.

0846J–BDC–03/16

1. BLOCK DIAGRAM

Figure 1-1. Simplified Block Diagram



2. DESCRIPTION

The Quad ADC is constituted by four 8-bit ADC cores which can be considered independently (four-channel mode) or grouped by two cores (two-channel mode with the ADCs interleaved two by two or one-channel mode where all four ADCs are all interleaved).

All four ADCs are clocked by the same external input clock signal and controlled via an SPI (Serial Peripheral Interface). An analog multiplexer (cross-point switch) is used to select the analog input depending on the mode the Quad ADC is used.

The clock circuit is common to all four ADCs. This block receives an external 2.5 GHz clock (maximum frequency) and preferably a low jitter symmetrical signal. In this block, the external clock signal is then divided by two in order to generate the internal sampling clocks:

- In four-channel mode, the same 1.25 GHz clock is directed to all four ADC cores and T/H
- In two-channel mode, the in-phase 1.25 GHz clock is sent to ADC A or C and the inverted 1.25 GHz clock is sent to ADC B or D, while the analog input is sent to both ADCs, resulting in an interleaved mode with an equivalent sampling frequency of 2.5 Gsps
- In one-channel mode, the in-phase 1.25 GHz clock is sent to ADC A while the inverted 1.25 GHz clock is sent to ADC B, the in-phase 1.25 GHz clock is delayed by 90° to generate the clock for ADC C and the inverted 1.25 GHz clock is delayed by 90° to generate the clock for ADC D, resulting in an interleaved mode with an equivalent sampling frequency of 5 Gsps

Several adjustments for the sampling delay and the phase are included in this clock circuit to ensure a proper phase relation between the different clocks generated internally from the 2.5 GHz clock.

The *cross-point switch* (analog MUX) is common to all ADCs. It allows to select the analog input that has been chosen by the user:

- In four-channel mode, each analog input is sent to the corresponding ADC (AAI to ADC A, BAI to ADC B, CAI to ADC C and DAI to ADC D)
- In two-channel mode, one can consider that there are two independent ADCs composed of ADC A and B for the first one and of ADC C and D for the second one. The two analog inputs can be applied on AAI or on BAI for the first ADC (in which case, the signal is redirected internally to the second ADC of the pair that is, B or A respectively) and on CAI or DAI (in which case, the signal is redirected internally to the second ADC of the pair that is, D or C respectively)
- In one-channel mode, one analog input is chosen among AAI, BAI, CAI and DAI and then sent to all four ADCs

Figure 2-1. Four-channel Mode Configuration

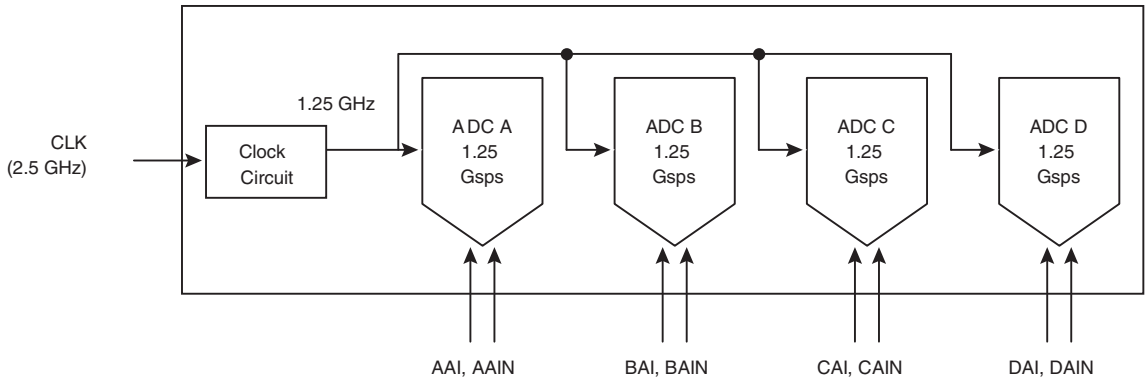


Figure 2-2. Two-channel Mode Configuration (Analog Input A and Analog Input C)

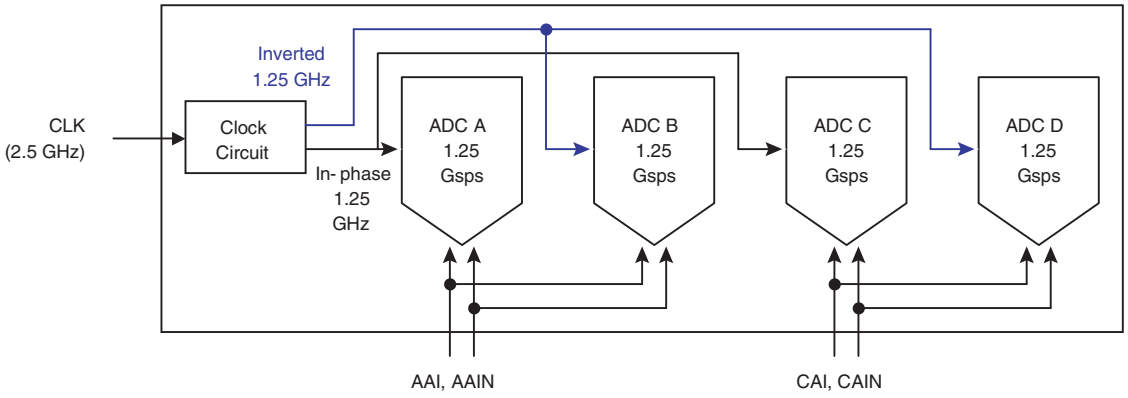


Figure 2-3. Two-channel Mode Configuration (Analog Input A and Analog Input D)

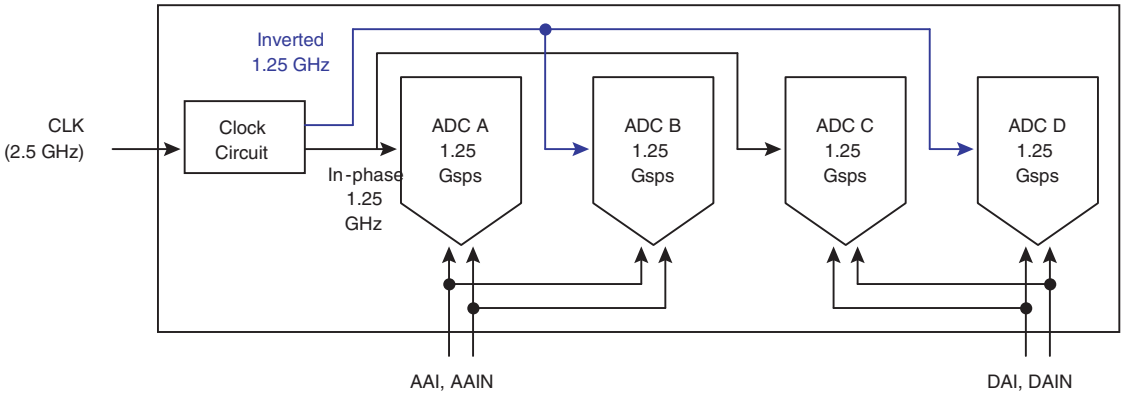


Figure 2-4. Two-channel Mode Configuration (Analog Input B and Analog Input C)

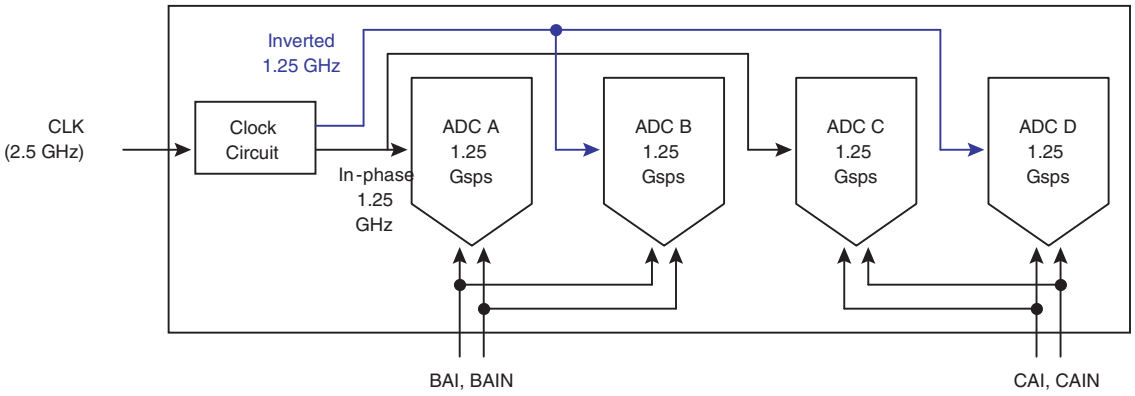


Figure 2-5. Two-channel Mode Configuration (Analog Input B and Analog Input D)

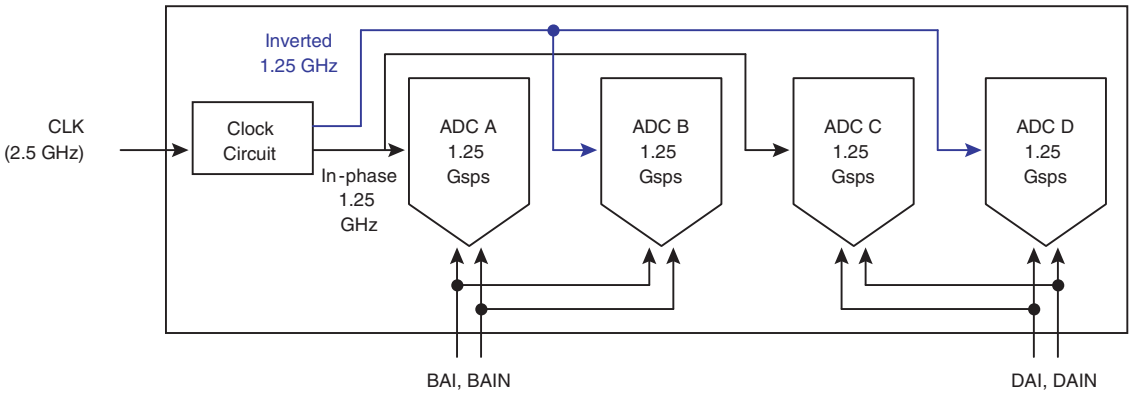
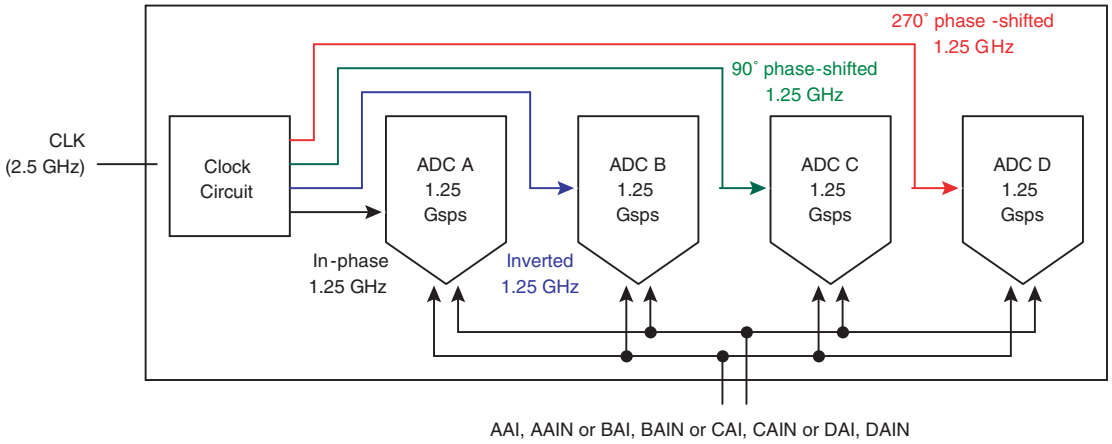


Figure 2-6. One-channel Mode Configuration



Note: For simplification purpose of the timer the temporal order of ports regarding sampling is A C B D, therefore samples order at output port is as follows:
A: N, N + 4, N + 8, N + 12…
C: N + 1, N + 5, N + 9…
B: N + 2, N + 6, N + 10…
D: N + 3, N + 7, N + 11…

The *T/H* (Track and Hold) is located after the cross-point switch and before the ADC cores. This block is used to track the data when the internal sampling clock is low and to hold the data when the internal sampling clock is high. This stage has a gain of two.

The *ADC cores* are all the same for the four ADCs. They include a quantifier block as well as a fast logic block composed of regenerating latches and the binary/Gray decoding block. They can handle a maximum sampling rate of 1.25 Gsps.

The *SPI* block provides the digital interface for the digital controls of the ADCs. All the functions of the ADC are contained in the SPI registers and controlled via this SPI (channel selection, standby mode, binary or Gray coding, 1:1 or 1:2 DMUX, Offset Gain and Phase adjust etc.).

The *demultiplexer block* allows the user to divide the output data rate by a factor of 2 (1:2 DMUX, selectable via the SPI, in the Control register), hence decreasing the output rate to a maximum of 625 Msps instead of 1.25 Gsps in double data rate.

The *output buffers* are LVDS compatible. They should be terminated using a 100Ω external termination resistor. When the 1:1 DMUX ratio is selected, half of the output data buffers (*L* port data bits) is switched off to optimize the power consumption. In this mode, the *L* port data bits can then be left floating (no termination required), since both outputs of the buffers will deliver High logical level.

The *ADC SYNC buffer* is also LVDS compatible. When active, the SYNC signal makes the output clock signals go low. The output data are undetermined during the reset and until the output clock restarts.

When the SYNC signal is released, the output clock signals restart after TDR + pipeline delay + a certain number of input clock cycles which is programmed via the SPI in the SYNC register (from minimum delay to minimum delay + 15 × 2 input clock cycles).

A diode for the die junction temperature monitoring is implemented using a diode-mounted transistor but not connected to the die: both cathode and anode are accessible externally.

Eight *DACs for the gain and the offset controls* are included in the design and are addressed through the SPI:

- Offset DACs act close to the cross-point switch
- Gain DACs act on the biasing of the reference ladders of each ADC core

These DACs have a resolution of 8-bit and will allow the control via the SPI of the offset and gain of the ADCs:

- Gain adjustment on 256 steps, ±18% range
- Offset adjustment on 256 steps, ±50 mV range

Four DACs for fine phase control are included in the design and are addressed through the SPI, they have an 8-bit resolution, and a tuning range of ±14 ps (1 step is about 110 fs).

3. SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Positive supply voltage	V_{CC}	4	V
Positive digital supply voltage	V_{CCD}	2.5	V
Positive output supply voltage	V_{CCO}	2.5	V
Analog input voltages	V_{IN} or V_{INN}	GND –0.3 (min) V_{CC} +0.3 (max)	V
Maximum difference between V_{IN} and V_{INN}	$V_{IN} – V_{INN}$	4	Vpp
Clock input voltage	V_{CLK} or V_{CLKN}	GND –0.3 (min) V_{CC} +0.3 (max)	V
Maximum difference between V_{CLK} and V_{CLKN}	$V_{CLK} – V_{CLKN}$	4	Vpp
Digital input voltage	V_D	V_{CC} + 0.3	V
Junction temperature	T_J	125	°C

Note: Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

4. RECOMMENDED CONDITIONS OF USE

Table 4-1. Recommended Conditions of Use

Parameter	Symbol	Comments	Recommended Value	Unit
Positive supply voltage	V_{CC}	Analog core and SPI pads	3.3	V
Positive digital supply voltage	V_{CCD}	SPI core	1.8	V
Positive output supply voltage	V_{CCO}	Output buffers	1.8	V
Differential analog input voltage (full scale)	V_{IN}, V_{INN} $V_{IN} – V_{INN}$		±250 500	mV mVpp
Digital CMOS input	V_D	V_{IL} V_{IH}	0 V_{CC}	V
Clock input power level	P_{CLK} P_{CLKN}		0	dBm
Clock frequency	F_{CLK}	For operation at 1.25 Gsps, 2.5 Gsps or 5 Gsps in four-channel, two-channel or one-channel mode respectively	≤ 2.5	GHz
Operating temperature range	T_{amb}	Commercial *C* grade	0°C < T_{amb} < 70°C	°C
Storage temperature	T_{stg}		–55 to 150	°C

No power sequence recommendation. The power supplies can be switched on and off in any order.

5. ELECTRICAL CHARACTERISTICS

Unless otherwise specified:

- V_{CC} = 3.3V, V_{CCD} = 1.8V, V_{CCO} = 1.8V
- –1 dBFS analog input (full scale input: $V_{IN} – V_{INN}$ = 500 mVpp)
- Clock input differentially driven, analog input differentially driven
- Default mode: four-channel mode ON, binary output data format, digital interface ON, 1:2 DMUX ON, standby mode OFF minimum bandwidth,

Table 5-1. Electrical Characteristics

Parameter	Symbol	Test Level	Min	Typ	Max	Unit	Notes
Resolution				8		Bit	
Power Requirements							
Power supply voltage							
Analog and SPI pads	V_{CC}		3.15	3.3	3.45	V	
Digital	V_{CCD}		1.7	1.8	1.9	V	
Output	V_{CCO}		1.7	1.8	1.9	V	
Power supply current (DMUX 1:1)							
Analog and SPI pads	I_{CC}	1,4		1.175	1.3	A	
Digital	I_{CCD}			4.9	5.5	mA	
Output	I_{CCO}			178	200	mA	

Table 5-1. Electrical Characteristics (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit	Notes
Power supply current (DMUX 1:2) Analog and SPI pads Digital Output	 I_{CC} I_{CCD} I_{CCO}	1,4		 1.25 4.9 300	 1.35 5.5 350	 A mA mA	
Power supply current (full standby mode, DMUX 1:1) Analog and SPI pads Digital Output and 3-Wire serial interface	 I_{CC} I_{CCD} I_{CCO}	1, 4		 136 4.9 29	 150 5.5 45	 mA mA mA	
Power supply current (full standby mode, DMUX 1:2) Analog and SPI pads Digital Output and 3-Wire serial interface	 I_{CC} I_{CCD} I_{CCO}	1, 4		 136 4.9 37	 150 5.5 45	 mA mA mA	
Power supply current (partial standby mode, DMUX 1:1) Analog and SPI pads Digital Output and 3-Wire serial interface	 I_{CC} I_{CCD} I_{CCO}	1, 4		 630 4.9 102	 700 5.5 200	 mA mA mA	
Power supply current (partial standby mode, DMUX 1:2) Analog and SPI pads Digital Output and 3-Wire serial interface	 I_{CC} I_{CCD} I_{CCO}	1, 4		 660 4.9 169	 750 5.5 200	 mA mA mA	
Power dissipation (max. power supplies) Full power (DMUX 1:1) Full power (DMUX 1:2) Partial standby (DMUX 1:1) Partial standby (DMUX 1:2) Full standby (DMUX 1:1) Full standby (DMUX 1:2)	 P_D	1, 4		 4.2 4.7 2.45 2.5 0.51 0.525	 4.5 4.9 2.55 2.8 0.59 0.59	 W W W W W W	
Analog Inputs							
Full-scale input voltage range (differential mode)	V_{IN} V_{INN}	1,4		250 250		mVpp mVpp	
Full-scale input voltage range (differential mode) Extended range	V_{IN} V_{INN}	1,4		312.5 312.5		mVpp	
Input common mode (provided by CMIRefAB and CMIRefCD)	V_{ICM}	1,4	1.7	1.8	1.95	V	(1)
Analog input capacitance (die + package)	C_{IN}	5		0.5		pF	
Input resistance (differential)	R_{IN}	4	90	100	110	Ω	(2)

Table 5-1. Electrical Characteristics (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit	Notes
Clock Inputs							
Source type	Differential Sinewave						
Clock input common mode voltage (note: the clock should be AC coupled) for information only	V_{CM}	5		1.8		V	
Clock input power level (low phase noise sinewave input)100Ω differential, AC coupled signal	P_{CLK}	4	–9	0	4	dBm	
Clock input swing (differential voltage) on each clock input	V_{CLK}, V_{CLKN}	4	159 159	447 447	709 709	mVpp mVpp	
Clock input capacitance (die + package)	C_{CLK}	5		0.5		pF	
Clock input resistance (differential)	R_{CLK}	4	85	113	115	Ω	
Clock jitter (max. allowed on clock source) For 1 GHz sinewave analog input	Jitter	4			500	fs	
Clock duty cycle requirement in one-channel mode for performance	Duty cycle	4	48	50	52	%	
Clock duty cycle requirement in two-channel mode for performance	Duty cycle	4	40	50	60	%	
Clock duty cycle requirement in four-channel mode for performance	Duty cycle	4	40	50	60	%	
SYNC, SYNCN Inputs							
Logic compatibility	LVDS						
Input voltages to be applied 50Ω transmission lines Logic Low Logic High Swing (each single-ended output) Common Mode	 V_{IL} V_{IH} V_{IH}-V_{IL} V_{ICM}	1,4	1.4	 330 1.2	 1.1	 V V mV V	
SYNC, SYNCN input capacitance	CSYNC	5		0.5		pF	
SYNC, SYNCN Input resistance	RSYNC	4	90	100	110	Ω	
SPI							
CMOS low level input voltage	V_{ilc}	1,4	0		0.25 × V_{CC}	V	(3)
CMOS high level input voltage	V_{ihc}	1,4	0.75 × V_{CC}		V_{CC}	V	(3)
CMOS low level of Schmitt trigger	Vtminusc	4			0.35 × V_{CC}	V	(3)(4)
CMOS high level of Schmitt trigger	Vtplusc	4	0.65 × V_{CC}			V	(3)(4)
CMOS Schmitt trigger hysteresis	Vhystc	4	0.15 × V_{CC}			V	(5)(6)
CMOS low level output voltage (Iolc = 2 or 3 mA)	Volc	4			0.4	V	(5)(6)
CMOS high level output voltage (Iohc = 2 or 3 mA)	Vohc	4	0.8 × V_{CC}			V	(7)

Table 5-1. Electrical Characteristics (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit	Notes
CMOS low level input current (Vinc = 0 V)	Iilc	1,4			30	nA	(8)
CMOS high level input current (Vinc = V_{CC})	Iihc	1,4			165	nA	(8)
RESETN low level input current	Iilc	1, 4		40	50	µA	(8)
RESETN high level input current	Iihc	1, 4			10	nA	(8)
Digital Data and Data Ready Outputs							
Logic compatibility		1,4		LVDS			(9)
Output levels 50Ω transmission lines, 100Ω (2 × 50Ω) differentially terminated							
Logic low	V_{OL}	1,4		1.1	1.25	V	(9)
Logic high	V_{OH}		1.25	1.42		V	
Swing (each single-ended output)	$V_{OH} – V_{OL}$		250	320	450	mV	
Common mode	V_{OCM}		1.125	1.28	1.575	V	
DC Accuracy							
Gain central value		1,4		1			(10)
Gain error drift		4			0.1	%/°C	
Input offset voltage		1,4		0		mV	(10)
Four-channel Mode (Fsampling = 1.25 Gsps, Fin = 95 KHz, –1 dBFS), for Each Channel *Without Calibration*							
DNLrms	DNLrms	1,4		0.07	0.15	LSB	(11)
Differential nonlinearity	DNL+	1,4		0.18	0.35	LSB	(11)
Differential nonlinearity	DNL-	1,4	–0.35	–0.18		LSB	(11)
INLrms	INLrms	1,4		0.18	0.4	LSB	(11)
Integral nonlinearity	INL+	1,4		0.4	0.9	LSB	(11)
Integral nonlinearity	INL-	1,4	–0.9	–0.4		LSB	(11)
Two-channel Mode (Fsampling = 2.5 Gsps, Fin = 95 KHz, –1 dBFS), for Each Channel *Without Calibration*							
DNLrms	DNLrms	1,4		0.05	0.15	LSB	(11)
Differential nonlinearity	DNL+	1,4		0.14	0.35	LSB	(11)
Differential nonlinearity	DNL-	1,4	–0.35	–0.14		LSB	(11)
INLrms	INLrms	1,4		0.14	0.4	LSB	(11)
Integral nonlinearity	INL+	1,4		0.35	0.9	LSB	(11)
Integral nonlinearity	INL-	1,4	–0.9	–0.35		LSB	(11)
One-channel Mode (Fsampling = 5 Gsps, Fin = 95 KHz, –1 dBFS) *Without Calibration*							
DNLrms	DNLrms	1,4		0.04	0.15	LSB	(11)
Differential nonlinearity	DNL+	1,4		0.12	0.35	LSB	(11)
Differential nonlinearity	DNL-	1,4	–0.35	–0.12		LSB	(11)

Table 5-1. Electrical Characteristics (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit	Notes
INLrms	INLrms	1,4		0.11	0.4	LSB	(11)
Integral nonlinearity	INL+	1,4		–0.27	0.9	LSB	(11)
Integral nonlinearity	INL-	1,4	–0.9	0.27		LSB	(11)

Notes:
1. The input common mode voltage is delivered via the CMIRefAB and CMIRefCD signals for channels A and B, and C and D respectively. The minimum load allowed on these signals is 2.5 kΩ (optimal load = 5 kΩ to 10 kΩ).
2. The input resistance can be trimmed via register at address 0x13 to reach the 100Ω value.
3. A minimum noise margin of 0.05 × V_{CC} is taken for Schmitt trigger input threshold switching levels compared to Vilc and Vihc.
4. Parameters specified for characterization purpose only, not valid at chip level specification.
5. Takes in account 200 mV voltage drop in both supply lines.
6. Iolc and Iohc values are source/sink currents in worst case conditions reflected in the name of the IO cell.
7. Leakage values related to ESD protection scheme and must be checked against leakage current observed with this process.
8. Internal 75 kΩ pull up.
9. Differential output buffers impedance = 100Ω differential.
10. Offset and Gain central values can be set to 0 mV and 1 respectively using the gain and offset adjustments provided in the SPI.
11. Values obtained without calibration. With calibration, |INL| values can be lowered to ±0.25 LSB typ (± 0.5 LSB max).

5.1 AC Electrical Characteristics

Unless otherwise specified:

- V_{CC} = 3.3V, V_{CCD} = 1.8V, V_{CCO} = 1.8V
- –1 dBFS analog input (full scale Input: $V_{IN} – V_{INN}$ = 500 mVpp)
- Clock input differentially driven; analog input differentially driven
- Default mode: four-channel mode ON, binary output data format, digital interface ON, 1:2 DMUX ON, standby mode OFF minimum bandwidth

Table 5-2. AC Electrical Characteristics

Parameter	Symbol	Test Level	Min	Typ	Max	Unit	Notes
AC Analog Inputs							
Full power input bandwidth Full setting (BW = *11* in register 0x01) Nominal setting (BW = *10* in register 0x01) Reduced setting (BW = *01* in register 0x01) Min setting (BW = *00* in register 0x01, default mode)	FPBW	4	 1.5 1.3 400 300	 2 1.5 600 500		 GHz GHz MHz MHz	(1)
Gain flatness (over any 500 MHz in full bandwidth setting, BW = *11* in register 0x01)	GF	4			1	dB	
Input voltage standing wave ratio	VSWR	4			1.6		(2)

Table 5-2. AC Electrical Characteristics (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit	Notes
Crosstalk (Fin = 620 MHz)		1,4	55	62		dB	
Dynamic Performance, Four-channel Mode (Fsampling = 1.25 Gsps, –1 dBFS) for Each Channel							
Effective number of bits Fs = 1.25 Gsps Fin = 10 MHz Fs = 1.25 Gsps Fin = 100 MHz Fs = 1.25 Gsps Fin = 620 MHz	ENOB	1,4	7.2 7.2 7	7.5 7.5 7.3		Bit	(3)
Signal-to-noise ratio Fs = 1.25 Gsps Fin = 10 MHz Fs = 1.25 Gsps Fin = 100 MHz Fs = 1.25 Gsps Fin = 620 MHz	SNR	1,4	45 45 43	46.5 46.5 45		dBc	(3)
Total harmonic distortion (25 Harmonics) Fs = 1.25 Gsps Fin = 10 MHz Fs = 1.25 Gsps Fin = 100 MHz Fs = 1.25 Gsps Fin = 620 MHz	|THD|	1,4	46 46 46	56 56 54		dBc	(3)
Spurious free dynamic range Fs = 1.25 Gsps Fin = 10 MHz Fs = 1.25 Gsps Fin = 100 MHz Fs = 1.25 Gsps Fin = 620 MHz	|SFDR|	1,4	48 48 48	59 58 56		dBc	(3)
Two-tone third order intermodulation distortion Fs = 1.25 Gsps Fin1 = 490 MHz Fin2 = 495 MHz [7dBFS]	|IMD3|	4		50		dBFS	(3)
Dynamic Performance Two-channel Mode (Fsampling = 2.5 Gsps, –1 dBFS) for Each Channel							
Effective number of bits Fs = 1.25 Gsps Fin = 10 MHz Fs = 1.25 Gsps Fin = 100 MHz Fs = 1.25 Gsps Fin = 620 MHz	ENOB	1,4	7.2 7.2 6.9	7.5 7.5 7.2		Bit	(3)
Signal-to-noise ratio Fs = 1.25 Gsps Fin = 10 MHz Fs = 1.25 Gsps Fin = 100 MHz Fs = 1.25 Gsps Fin = 620 MHz	SNR	1, 4	44 44 42	46 46 44.5		dBc	(3)
Total harmonic distortion (25 Harmonics) Fs = 1.25 Gsps Fin = 10 MHz Fs = 1.25 Gsps Fin = 100 MHz Fs = 1.25 Gsps Fin = 620 MHz	|THD|	1,4	48 48 48	59 58 55		dBc	(3)
Spurious-free dynamic range Fs = 1.25 Gsps Fin = 10 MHz Fs = 1.25 Gsps Fin =100 MHz Fs = 1.25 Gsps Fin = 620 MHz	|SFDR|	1,4	49 48 48	59 58 56		dBc	(3)
Two-tone third order intermodulation distortion Fs = 2.5 Gsps Fin1 = 490 MHz Fin2 = 495 MHz [7dBFS]	|IMD3|	4		50		dBFS	(3)
Dynamic Performance – One-channel Mode (Fsampling = 5 Gsps, –1 dBFS)							

Table 5-2. AC Electrical Characteristics (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit	Notes
Effective number of bits Fs = 5 Gsps Fin = 10 MHz Fs = 5 Gsps Fin = 100 MHz Fs = 5 Gsps Fin = 620 MHz	ENOB	1,4	 7 7 6.8	 7.4 7.4 7.1		Bit	(3)
Signal-to-noise ratio Fs = 5 Gsps Fin = 10 MHz Fs = 5 Gsps Fin = 100MHz Fs = 5 Gsps Fin = 620 MHz	SNR	1,4	 43 43 41	 46 46 44		dBc	(3)
Total harmonic distortion (25 harmonics) Fs = 5 Gsps Fin = 10 MHz Fs = 5 Gsps Fin = 100 MHz Fs = 5 Gsps Fin = 620 MHz	|THD|	1,4	 50 50 48	 62 60 56		dBc	(3)
Spurious free dynamic range Fs = 5 Gsps Fin = 10 MHz Fs = 5 Gsps Fin = 100 MHz Fs = 5 Gsps Fin = 620 MHz	|SFDR|	1,4	 48 48 48	 59 58 58		dBc	(3)
Two-tone third order Intermodulation distortion Fs = 5 Gsps Fin1 = 490 MHz Fin2 = 495 MHz [–7dBFS]	|IMD3|	4		48		dBFS	(3)

Notes:
1. It is recommended to use the ADC in reduced bandwidth mode in order to minimize the noise in the ADC when allowed by the application. Same bandwidth in interleaving mode and non interleaving mode (4-/2-/1-channel modes).
2. Specified from DC up to 2.5 GHz input signal. Input VSWR is measured on a soldered device. It assumes an external 50Ω ± 2Ω controlled impedance line, and a 50Ω driving source impedance (S_{11} < –30 dB).
3. All the figures provided at Fin = 10 and 100 MHz were obtained using the ADC in minimum band mode (bit 9 = *0* and bit 8 = *0* of register at address 0x01).The ones provided at Fin = 620 MHz were obtained using the ADC nominal band mode (bit 9 = *1* and bit 8 = *0* of register at address 0x01).

5.2 Transient and Switching Performances

Table 5-3. Transient and Switching Performances Fc = 2.5 GHz

Parameter	Symbol	Test Level	Min	Typ	Max	Unit	Notes
Transient Performance							
Bit Error Rate at 1.25 Gsps in Gray mode	BER	4		10^{-16}		Error/ sample	(1)
ADC settling time (V_{IN} – V_{INN} = 400 mVpp) in full BW mode	TS	4		2		ns	
Overvoltage recovery time	ORT	4		2		ns	
ADC step response rise/fall time (10% to 90%) at Fc = 2.5 GHz		4		200	220	ps	
Overshoot		4			2	%	

Table 5-3. Transient and Switching Performances Fc = 2.5 GHz (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit	Notes
Ringback		4			2	%	
Switching Performance and Characteristics							
Clock frequency	F_{CLK}	4	400		2500	MHz	(2)(3)
Sampling frequency (for each channel) Four-channel mode Two-channel mode One-channel mode	F_S		 200 400 800		 1250 2500 5000	 Msps Msps Msps	
Minimum clock pulse width (high)	TC1	4	160			ps	
Minimum clock pulse width (low)	TC2	4	160			ps	
Aperture delay	TA	4		40		ps	(2)
ADC aperture uncertainty (internal)	Jitter	4		300		fs rms	(2)
Output rise time for DATA (20% to 80%)	TR	4	150	200	250	ps	(4)
Output fall time for DATA (20% to 80%)	TF	4	150	200	250	ps	
Output rise time for DATA READY (20% to 80%)	TR	4	150	200	250	ps	(4)
Output fall time for DATA READY (20% to 80%)	TF	4	150	200	250	ps	
Data output delay	TOD	4		3		ns	(5)
Data ready output delay	TDR	4		3		ns	(5)
	|TOD – TDR|	4			50	ps	(5)
Data ready pipeline delay *Four-Channel Mode* 1:1 DMUX 1:2 DMUX *Two-Channel Mode* 1:1 DMUX 1:2 DMUX *One-Channel Mode* 1:1 DMUX 1:2 DMUX	TPD	4		 10 15 11 16 11 16		 Clock Cycles	(6)

Table 5-3. Transient and Switching Performances Fc = 2.5 GHz (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit	Notes
Output data pipeline delay *Four-Channel Mode* 1:1 DMUX port AH, BH, CH, DH 1:2 DMUX port AH, BH, CH, DH 1:2 DMUX port AL, BL, CL, DL *Two-Channel Mode* 1:1 DMUX port AH, CH 1:1 DMUX port BH, DH 1:2 DMUX port AH, CH 1:2 DMUX port AL, CL 1:2 DMUX port BH, DH 1:2 DMUX port BL, DL *One-Channel Mode* 1:1 DMUX port AH 1:1 DMUX port BH 1:1 DMUX port CH 1:1 DMUX port DH 1:2 DMUX port AL 1:2 DMUX port BL 1:2 DMUX port CL 1:2 DMUX port DL 1:2 DMUX port AH 1:2 DMUX port BH 1:2 DMUX port CH 1:2 DMUX port DH	TPD	4		 9 11 13 10 9 12 14 11 13 10 9 9.5 8.5 14 13 13.5 12.5 12 11 11.5 10.5		Clock cycles	
Output data to data ready propagation Delay 1:1 DMUX 1:2 DMUX	TD1	4	 400 650	 500 850	 600 1050	 ps ps	(7)
Data ready to output data propagation delay 1:1 DMUX 1:2 DMUX	TD2	4	 200 550	 300 750	 400 950	 ps ps	(7)
Data ready reset delay	TRDR			3.5 clock cycles + 1.5 ns		ns	
Minimum SYNC pulse width	TSYNC		2 x Tclock				(8)
SYNC setup time	Tsetup			40		ps	(8)
SYNC Hold time	Thold			0		ps	(8)

Notes: 1. Output error amplitude < ±6 lsb. Fs = 1.25 Gsps T_J = 110°C.

2. See "Definition of Terms" on page 69.

3. The clock frequency lower limit is due to the gain.

4. 50Ω // C_{LOAD} = 2 pF termination (for each single-ended output). Termination load parasitic capacitance derating value: 50 ps/pF (ECL).
5. TOD and TDR propagation times are defined at package input/outputs. They are given for reference only.
6. Data ready pipeline delay is given from data N clock rising edge to first change in XDR signal (with X = A, B, C, D).
7. Values for TD1 and TD2 are given for a 2.5 GHz external clock frequency (50% duty cycle). For different sampling rates, apply the following formula:
   TD1 = T/2 +(TOD-TDR)
   TD2 = T/2 +(TOD-TDR),
   where T= clock period. This places the rising edge (True-False) of the differential data ready signal in the middle of the output data valid window. The difference TD1-TD2 gives an information if Data Ready is centred on the output data If Data ready is in the middle to data TD1 = TD2 = Tdata/2
8. Tclock = external clock period.
   SYNC cannot change less than 40 ps before CLK has a rising edge
   SYNC can change 0 ps after CLK has a rising edge
   SYNC must be high for 2 CLK (external clock) rising edges

5.3 Test Level Explanation

Table 5-4. Explanation of Test Levels

1	100% production tested at +25°C (1) (for *C* temperature range(2)).
2	100% production tested at +25°C(1), and sample tested at specified temperatures (for *V* temperature ranges(2)).
3	Sample tested only at specified temperatures.
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter is a typical value only guaranteed by design only.
6	100% production tested over specified temperature range (for *B/Q* temperature range(2)).

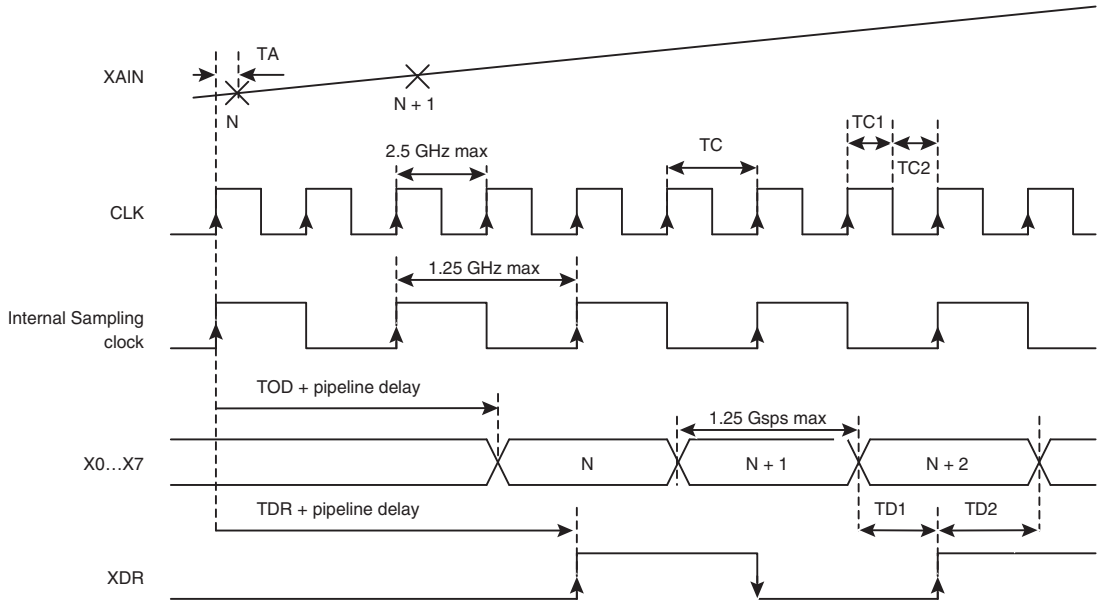
Only minimum and maximum values are guaranteed (typical values are resulting from characterization).

Notes: 1. Unless otherwise specified.
2. If applicable, please refer to “Ordering Information” on page 77”.

5.4 Timing Information

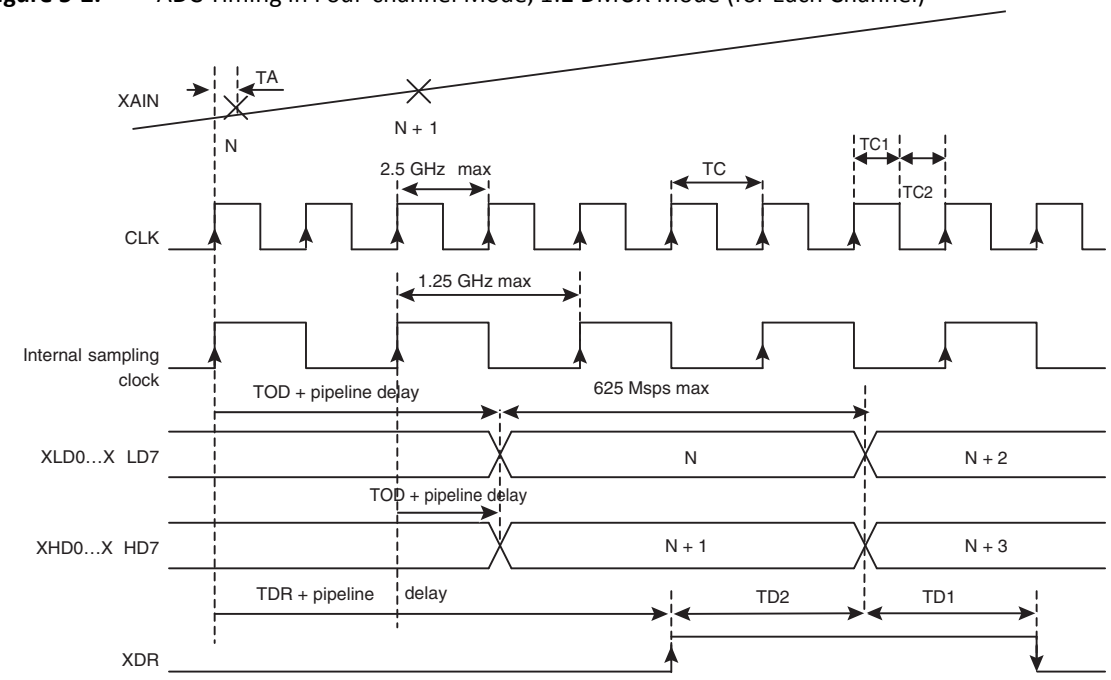
For the information on the reset sequence (using SYNC, SYNCN signals, please refer to Section 8.1 ”ADC Synchronization Signal (SYNC, SYNCN)” on page 43).

Figure 5-1. ADC Timing in Four-channel Mode, 1:1 DMUX Mode (for Each Channel)



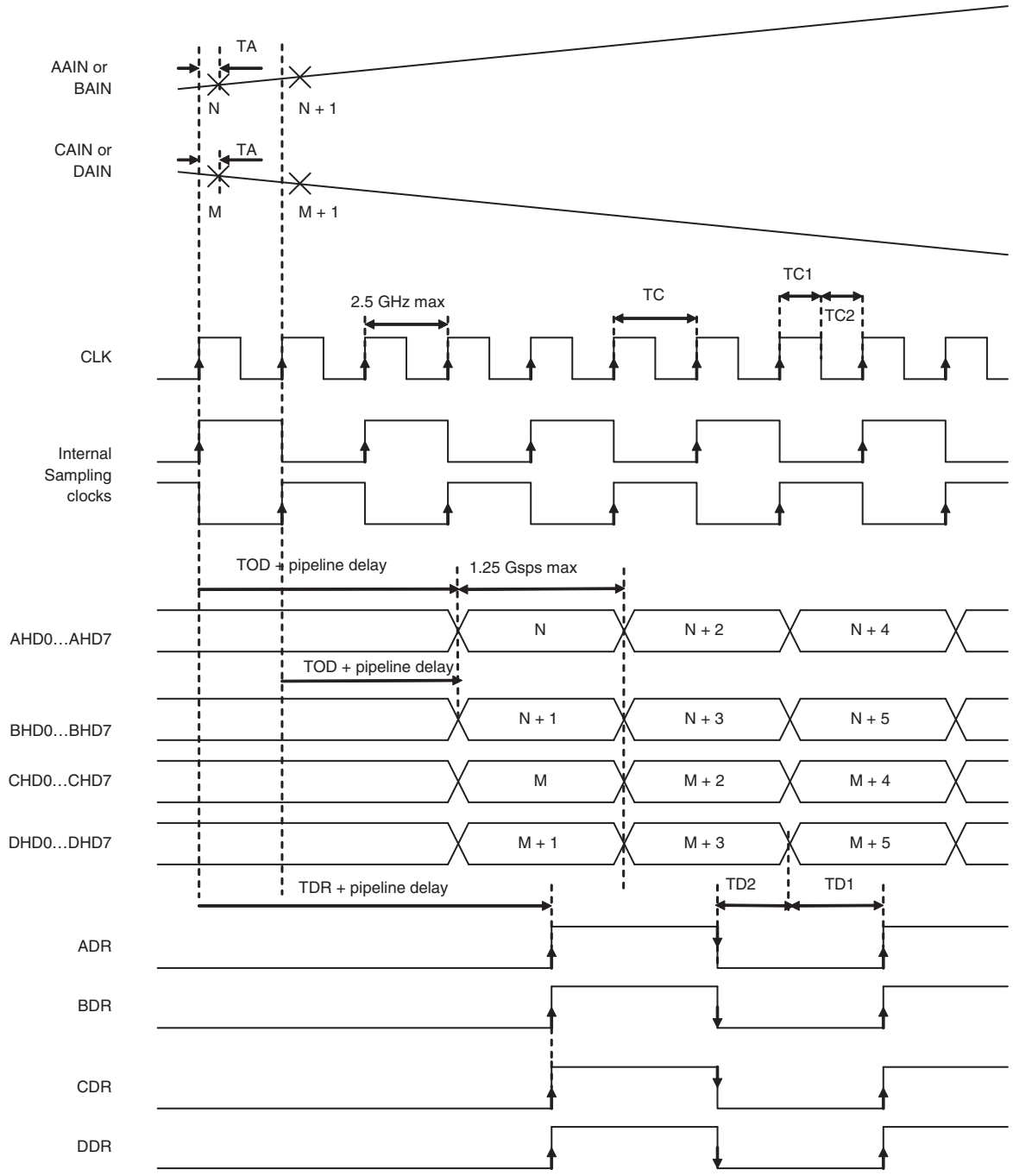
Notes: 1. X refers to A, B, C and D.
2. Not to scale.

Figure 5-2. ADC Timing in Four-channel Mode, 1:2 DMUX Mode (for Each Channel)



Notes: 1. X refers to A, B, C and D.
2. Not to scale.

Figure 5-3. ADC Timing in Two-channel Mode, 1:1 DMUX Mode



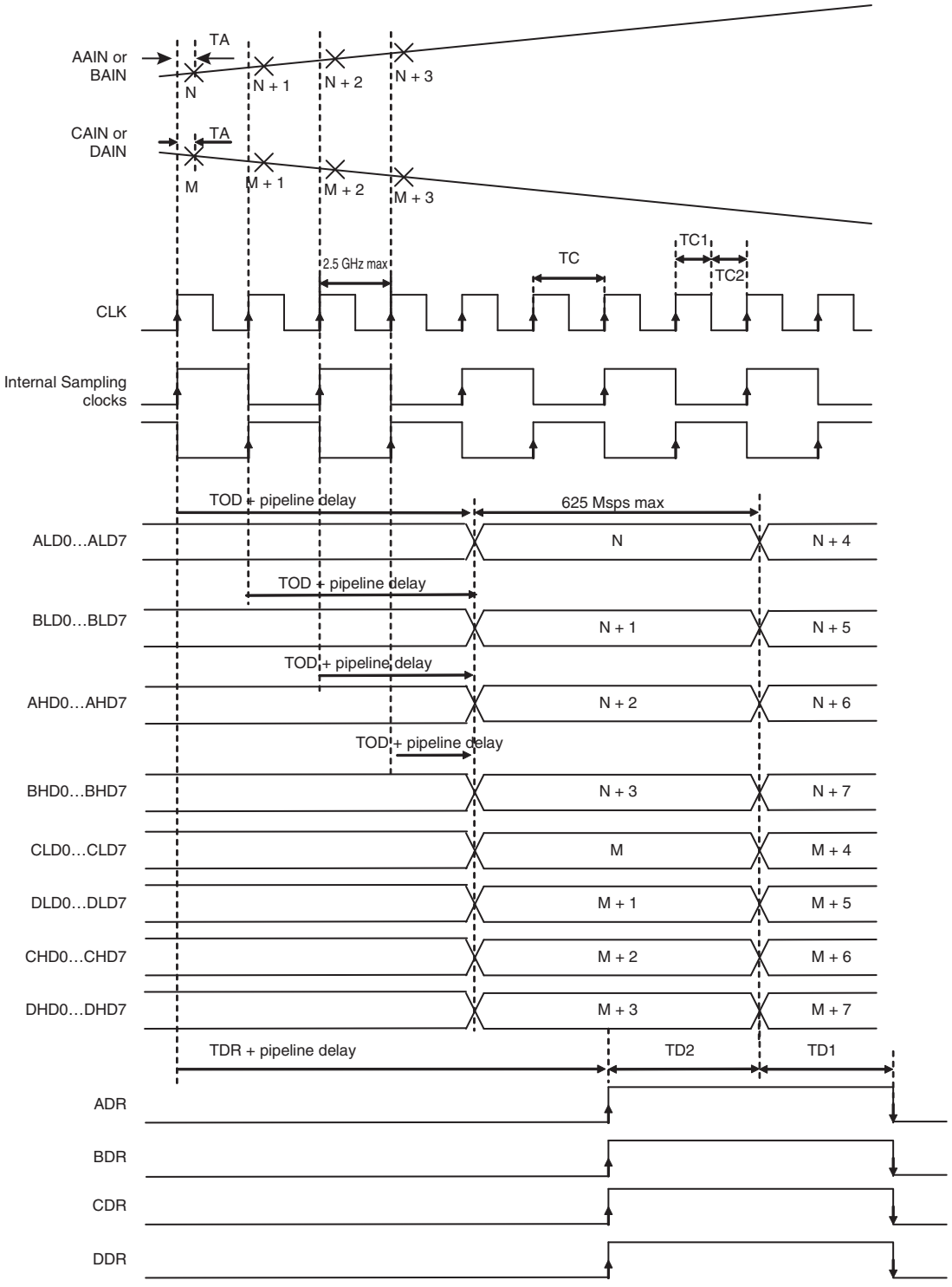
Notes: 1. In two-channel mode, the two analog inputs can be applied on:
(AAI, AAIN) and (CAI, CAIN), in which case, the outputs corresponding to (AAI, AAIN) will be on AHD0…AHD7 and BHD0…BHD7 and the ones corresponding to (CAI, CAIN) on CHD0…CHD7 and DHD0…DHD7

or (AAI, AAIN) and (DAI, DAIN), in which case, the outputs corresponding to (AAI, AAIN) will be on AHD0…AHD7 and BHD0…BHD7 and the ones corresponding to (DAI, DAIN) on CHD0…CHD7 and DHD0…DHD7
or (BAI, BAIN) and (CAI, CAIN), in which case, the outputs corresponding to (BAI, BAIN) will be on AHD0…AHD7 and BHD0…BHD7 and the ones corresponding to (CAI, CAIN) on CHD0…CHD7 and DHD0…DHD7

or (BAI, BAIN) and (DAIN, DAIN), in which case, the outputs corresponding to (BAI, BAIN) will be on AHD0…AHD7 and BHD0…BHD7 and the ones corresponding to (DAI, DAIN) on CHD0…CHD7 and DHD0…DHD7.

2. Not to scale.

Figure 5-4. ADC Timing in Two-Channel Mode, 1:2 DMUX Mode



Notes: 1. In two-channel mode, the two analog inputs can be applied on:

(AAI, AAIN) and (CAI, CAIN), in which case, the outputs corresponding to (AAI, AAIN) will be on ALD0…ALD7, AHD0…AHD7 and BLD0…BLD7, BHD0…BHD7 and the ones corresponding to (CAI, CAIN) on CLD0…CLD7, CHD0…CHD7 and DLD0…DLD7, DHD0…DHD7;

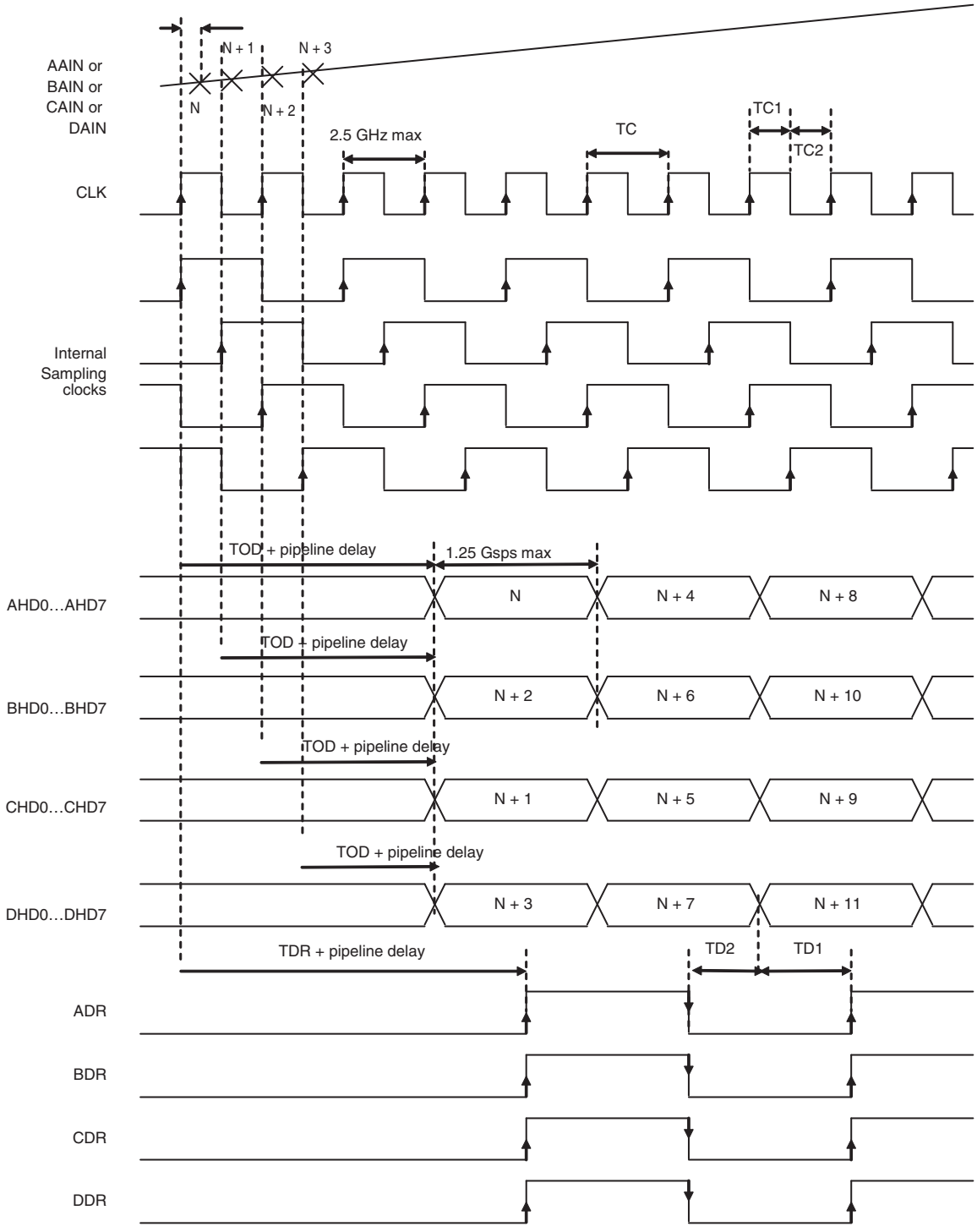
or (AAI, AAIN) and (DAI, DAIN), in which case, the outputs corresponding to (AAI, AAIN) will be on ALD0…ALD7, AHD0…AHD7 and BLD0…BLD7, BHD0…BHD7 and the ones corresponding to (DAI, DAIN) on CLD0…CLD7, CHD0…CHD7 and DLD0…DLD7, DHD0…DHD7;

or (BAI, BAIN) and (CAI, CAIN), in which case, the outputs corresponding to (BAI, BAIN) will be on ALD0…ALD7, AHD0…AHD7 and BLD0…BLD7, BHD0…BHD7 and the ones corresponding to (CAI, CAIN) on CLD0…CLD7, CHD0…CHD7 and DLD0…DLD7, DHD0…DHD7;

or (BAI, BAIN) and (DAIN, DAIN), in which case, the outputs corresponding to (BAI, BAIN) will be on ALD0…ALD7, AHD0…AHD7 and BLD0…BLD7, BHD0…BHD7 and the ones corresponding to (DAI, DAIN) on CLD0…CLD7, CHD0…CHD7 and DLD0…DLD7, DHD0…DHD7.

2. Not to scale.

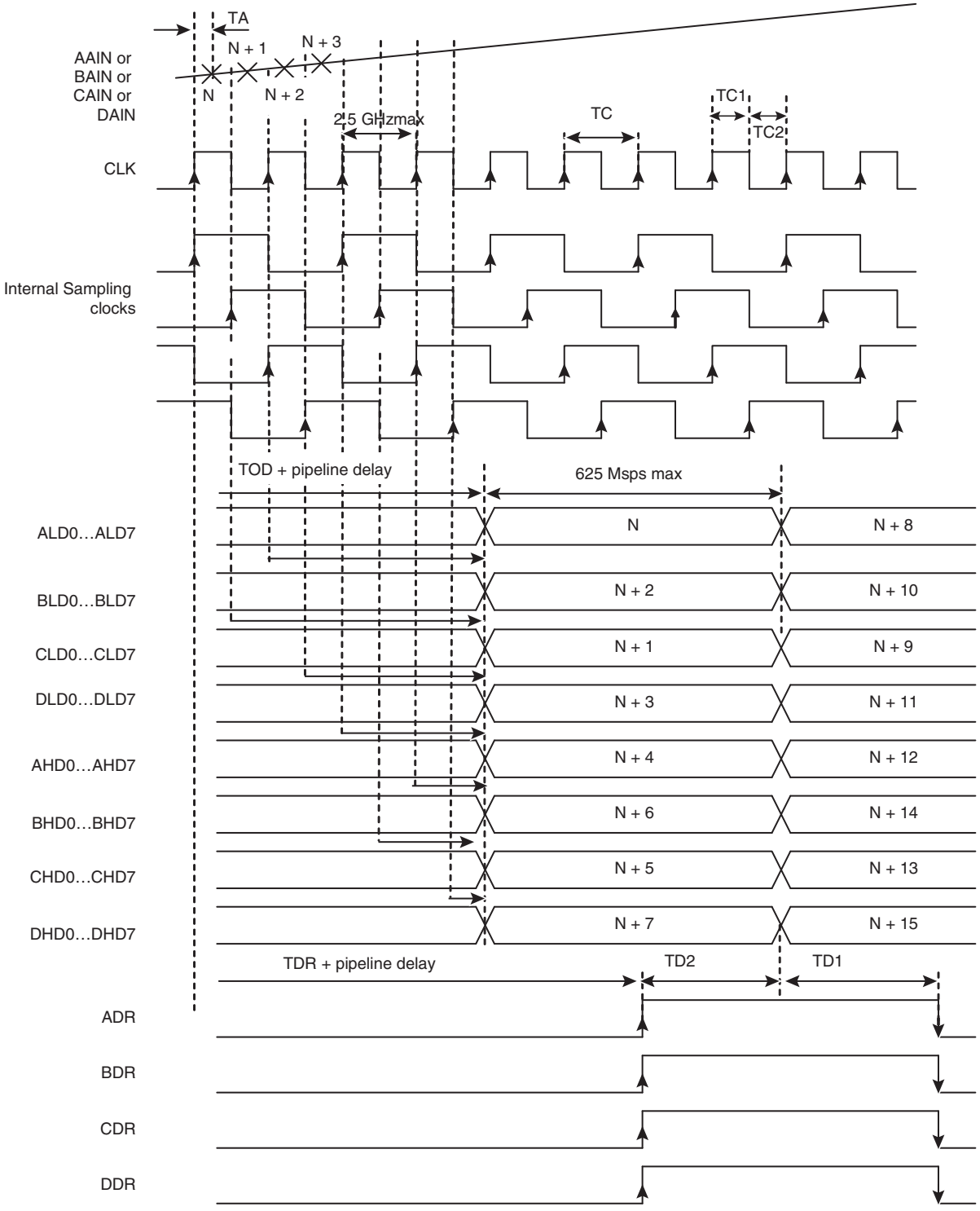
Figure 5-5. ADC Timing in One-channel Mode, 1:1 DMUX Mode



Notes: 1. In one-Channel mode, the analog input can be applied on (AAI,AAIN), (BAI, BAIN), (CAI, CAIN) or (DAI, DAIN). The choice is made via the SPI in the control register.

2. Not to scale.

Figure 5-6. ADC Timing in One-channel Mode, 1:2 DMUX Mode



Notes: 1. In one-channel mode, the analog input can be applied on (AAI,AAIN), (BAI, BAIN), (CAI, CAIN) or (DAI, DAIN). The choice is made via the SPI in the control register.

2. Not to scale.

5.5 Coding

Table 5-5. ADC Coding Table

Differential Analog Input	Voltage Level	Digital Output			
		Binary MSB……..LSB	Out-of-range	Gray MSB……..LSB	Out-of-range
+250 mV	>Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1	1	1 0 0 0 0 0 0 0	1
+250 mV	Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1	0	1 0 0 0 0 0 0 0	0
+248.05 mV	Top end of full scale – ½ LSB	1 1 1 1 1 1 1 0	0	1 0 0 0 0 0 0 1	0
+125 mV	3/4 full scale + ½ LSB	1 1 0 0 0 0 0 0	0	1 0 1 0 0 0 0 0	0
+123.05 mV	3/4 full scale – ½ LSB	1 0 1 1 1 1 1 1	0	1 1 1 0 0 0 0 0	0
+0.976 mV	Mid scale + ½ LSB	1 0 0 0 0 0 0 0	0	1 1 0 0 0 0 0 0	0
–0.976 mV	Mid scale – ½ LSB	0 1 1 1 1 1 1 1	0	0 1 0 0 0 0 0 0	0
–123.05 mV	1/4 full scale + ½ LSB	0 1 0 0 0 0 0 0	0	0 1 1 0 0 0 0 0	0
–125 mV	1/4 full scale – ½ LSB	0 0 1 1 1 1 1 1	0	0 0 1 0 0 0 0 0	0
–248.05 mV	Bottom end of full scale + ½ LSB	0 0 0 0 0 0 0 1	0	0 0 0 0 0 0 0 1	0
–250 mV	Bottom end of full scale – ½ LSB	0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0	0
< –250 mV	< Bottom end of full scale –½ LSB	0 0 0 0 0 0 0 0	1	0 0 0 0 0 0 0 0	1

6. PIN DESCRIPTION

6.1 Pinout View (Bottom View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
AD	GND	VCC	BLD6	BLD7	BLOR	GND	DiodA	tdreadyp	tdcop	trigp	SYNCP	CLK	CLKN	scan0	scan2	sclk	mosi	Res50	GND	CLOR	CLD7	CLD6	VCC	GND
AC	GND	VCC	BLD6N	BLD7N	BLORN	GND	DiodC	tdreadyn	tdcon	trign	SYNCN	GND	GND	scan1	rstn	csn	miso	Res62	GND	CLORN	CLD7N	CLD6N	VCC	GND
AB	BHOR	BHORN	VCC	GND	VCC	GND	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	GND	VCC	GND	VCC	CHORN	CHOR
AA	BHD7	BHD7N	VCC	GND	VCCO	VCC	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	VCC	VCCO	GND	VCC	CHD7N	CHD7
Y	BHD6	BHD6N	VCCO	GND	GND	VCCO	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	VCCO	GND	GND	VCCO	CHD6N	CHD6
W	BHD5	BHD5N	VCCO	GND	GND															GND	GND	VCCO	CHD5N	CHD5
V	BHD4	BHD4N	BLD5	BLD5N	GND															GND	CLD5N	CLD5	CHD4N	CHD4
U	BHD3	BHD3N	BLD4	BLD4N	VCCO															VCCO	CLD4N	CLD4	CHD3N	CHD3
T	BHD2	BHD2N	BLD3	BLD3N	GND															GND	CLD3N	CLD3	CHD2N	CHD2
R	BHD1	BHD1N	BLD2	BLD2N	VCC															VCC	CLD2N	CLD2	CHD1N	CHD1
P	BHD0	BHD0N	BLD1	BLD1N	GND															GND	CLD1N	CLD1	CHD0N	CHD0
N	BDR	BDRN	BLD0	BLD0N	VCC															VCC	CLD0N	CLD0	CDRN	CDR
M	ADR	ADRN	ALD0	ALD0N	VCC															VCC	DLD0N	DLD0	DDRN	DDR
L	AHD0	AHD0N	ALD1	ALD1N	GND															GND	DLD1N	DLD1	DHD0N	DHD0
K	AHD1	AHD1N	ALD2	ALD2N	VCC															VCC	DLD2N	DLD2	DHD1N	DHD1
J	AHD2	AHD2N	ALD3	ALD3N	GND															GND	DLD3N	DLD3	DHD2N	DHD2
H	AHD3	AHD3N	ALD4	ALD4N	VCCO															VCCO	DLD4N	DLD4	DHD3N	DHD3
G	AHD4	AHD4N	ALD5	ALD5N	GND															GND	DLD5N	DLD5	DHD4N	DHD4
F	AHD5	AHD5N	VCCO	GND	GND															GND	GND	VCCO	DHD5N	DHD5
E	AHD6	AHD6N	VCCO	GND	GND	VCCO	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCCO	GND	GND	VCCO	DHD6N	DHD6
D	AHD7	AHD7N	VCC	GND	VCCO	VCC	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCC	VCCO	GND	VCC	DHD7N	DHD7
C	AHOR	AHORN	VCC	GND	VCC	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCC	GND	VCC	DHORN	DHOR
B	GND	VCC	ALD6N	ALD7N	ALORN	GND	GND	GND	GND	GND	GND	CMIRef	CMIRef	GND	GND	GND	GND	GND	GND	DLORN	DLD7N	DLD6N	VCC	GND
A	GND	VCC	ALD6	ALD7	ALOR	GND	AAI	AAIN	GND	BAI	BAIN	GND	GND	CAI	CAIN	GND	DAI	DAIN	GND	DLOR	DLD7	DLD6	VCC	GND

VCC=3.3V VCCO = 1.8V VCCD = 1.8V

6.2 Pinout Table

Table 6-1. Pinout Table

Pin Label	Pin Number	Description
Power Supplies		
GND	A1, A6, A9, A12, A13, A16, A19 A24, B1, B6, B7, B8, B9, B10, B11, B14, B15, B16, B17, B18, B19, B24, C4, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C21, D4, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D21, E8, E9, E10, E11, E12, E13, E14, E15, E16, E17, J5, J20, L5, L20, P5, P20, T5, T20, Y8, Y9, Y12, Y13, Y16, Y17, AA4, AA8, AA9, AA12, AA13, AA16, AA17, AA21, AB4, AB6, AB8, AB9, AB12, AB13, AB16, AB17, AB19, AB21, AC1, AC6, AC12, AC13, AC19, AC24, AD1, AD6, AD19, AD24, E4, E5, E20, E21, F4, F5, F20, F21, G5, G20, V5, V20, W4, W5, W20, W21, Y4, Y5, Y20, Y21	Ground
V_{CC}	A2, A23, B2, B23, C3, C5, C6, C19, C20, C22, D3, D6, D7, D18, D19, D22, E7, E18, K5, K20, M5, M20, N5, N20, R5, R20, Y7, Y10, Y15, Y18, AA3, AA6, AA7, AA10, AA15, AA18, AA19, AA22, AB3, AB5, AB7, AB10, AB15, AB18, AB20, AB22, AC2, AC23, AD2, AD23, AA14, AB14, Y14	Analog + SPI pads power supply (3.3V)
V_{CCD}	Y11, AB11, AA11	Digital power supply (1.8V)
V_{CCO}	D5, D20, E3, E6, E19, E22, F3, F22, H5, H20, U5, U20, W3, W22, Y3, Y6, Y19, Y22, AA5, AA20	Output power supply (1.8V)
Clock Signal		
CLK	AD12	In-phase input clock signal
CLKN	AD13	Out-of-phase input clock signal
Analog Input Signals		
AAI	A7	In-phase analog input channel A
AAIN	A8	Out-of phase analog input channel A
BAI	A10	In-phase analog input channel B
BAIN	A11	Out-of phase analog input channel B
CAI	A14	In-phase analog input channel C
CAIN	A15	Out-of-phase analog input channel C
DAI	A17	In-phase analog input channel D
DAIN	A18	Out-of-phase analog input channel D

Table 6-1. Pinout Table (Continued)

Pin Label	Pin Number	Description
Digital Output Signals		
ALD0 ALD1 ALD2 ALD3 ALD4 ALD5 ALD6 ALD7	M3 L3 K3 J3 H3 G3 A3 A4	Channel A port L in-phase output data
ALD0N ALD1N ALD2N ALD3N ALD4N ALD5N ALD6N ALD7N	M4 L4 K4 J4 H4 G4 B3 B4	Channel A port L out-of-phase output data
ALOR ALORN	A5 B5	Channel A port L out-of-range bit
AHD0 AHD1 AHD2 AHD3 AHD4 AHD5 AHD6 AHD7	L1 K1 J1 H1 G1 F1 E1 D1	Channel A port H in-phase output data
AHD0N AHD1N AHD2N AHD3N AHD4N AHD5N AHD6N AHD7N	L2 K2 J2 H2 G2 F2 E2 D2	Channel A port H out-of-phase output data
AHOR AHORN	C1 C2	Channel A port H out-of-range bit
ADR ADRN	M1 M2	Channel A output clock
BLD0 BLD1 BLD2 BLD3 BLD4 BLD5 BLD6 BLD7	N3 P3 R3 T3 U3 V3 AD3 AD4	Channel B port L in phase output data

Table 6-1. Pinout Table (Continued)

Pin Label	Pin Number	Description
BLD0N BLD1N BLD2N BLD3N BLD4N BLD5N BLD6N BLD7N	N4 P4 R4 T4 U4 V4 AC3 AC4	Channel B port L out-of-phase output data
BLOR BLORN	AD5 AC5	Channel B port L out-of-range bit
BHD0 BHD1 BHD2 BHD3 BHD4 BHD5 BHD6 BHD7	P1 R1 T1 U1 V1 W1 Y1 AA1	Channel B port H in phase output data
BHD0N BHD1N BHD2N BHD3N BHD4N BHD5N BHD6N BHD7N	P2 R2 T2 U2 V2 W2 Y2 AA2	Channel B port H out-of-phase output data
BHOR BHORN	AB1 AB2	Channel B port H out-of-range bit
BDR BDRN	N1 N2	Channel B output clock
CLD0 CLD1 CLD2 CLD3 CLD4 CLD5 CLD6 CLD7	N22 P22 R22 T22 U22 V22 AD22 AD21	Channel C port L in phase output data
CLD0N CLD1N CLD2N CLD3N CLD4N CLD5N CLD6N CLD7N	N21 P21 R21 T21 U21 V21 AC22 AC21	Channel C port L out of phase output data

Table 6-1. Pinout Table (Continued)

Pin Label	Pin Number	Description
CLOR CLORN	AD20 AC20	Channel C port L out-of-range bit
CHD0 CHD1 CHD2 CHD3 CHD4 CHD5 CHD6 CHD7	P24 R24 T24 U24 V24 W24 Y24 AA24	Channel C port H in phase output data
CHD0N CHD1N CHD2N CHD3N CHD4N CHD5N CHD6N CHD7N	P23 R23 T23 U23 V23 W23 Y23 AA23	Channel C port H out of phase output data
CHOR CHORN	AB24 AB23	Channel C port H out-of-range bit
CDR CDRN	N24 N23	Channel C Output clock
DLD0 DLD1 DLD2 DLD3 DLD4 DLD5 DLD6 DLD7	M22 L22 K22 J22 H22 G22 A22 A21	Channel D port L in-phase output data
DLD0N DLD1N DLD2N DLD3N DLD4N DLD5N DLD6N DLD7N	M21 L21 K21 J21 H21 G21 B22 B21	Channel D port L out-of-phase output data
DLOR DLORN	A20 B20	Channel D port L out-of-range bit

Table 6-1. Pinout Table (Continued)

Pin Label	Pin Number	Description
DHD0 DHD1 DHD2 DHD3 DHD4 DHD5 DHD6 DHD7	L24 K24 J24 H24 G24 F24 E24 D24	Channel D port H in-phase output data
DHD0N DHD1N DHD2N DHD3N DHD4N DHD5N DHD6N DHD7N	L23 K23 J23 H23 G23 F23 E23 D23	Channel D port H out-of-phase output data
DHOR DHORN	C24 C23	Channel D port H out-of- range bit
DDR DDRN	M24 M23	Channel D Output clock
SPI Signals		
Csn	AC16	Chip select (Active low)
Sclk	AD16	SPI clock
MOSI	AD17	Master out, Slave In SPI input
MISO	AC17	Master In, Slave Out SPI output MISO should be pulled up to Vcc using 1K - 3K3 resistor MISO not tristated when inactive
Other Signals		
rstn	AC15	SPI asynchronous reset (active low)
scan0 scan1 scan2	AD14 AC14 AD15	Scan mode signals Pull up to V_{CC} with 4.7 KΩ
SYNCN SYNCP	AC11 AD11	Synchronization signal
Res50 Res62	AD18 AC18	50Ω and 62Ω reference resistor input
CMIRefAB CMIRefCD	B12 B13	Output reference for channel A-B and C-D Input common mode
DiodA DiodC	AD7 AC7	Temperature diode Anode and Cathode

Table 6-1. Pinout Table (Continued)

Pin Label	Pin Number	Description
trigp trign tdcop tdcon	AD10 AC10 AD9 AC9	Reserved pins See “Test Signals” on page 49. for more information
tdreadyn	AC8	Connect to ground
tdreadyp	AD8	Connect to ground

7. CHARACTERIZATION RESULTS

Nominal conditions (unless otherwise specified):

- V_{CC} = 3.3V, V_{CCD} = 1.8V, V_{CCO} = 1.8V
- –1 dBFS analog input (Full scale Input: $V_{IN} – V_{INN}$ = 500 mVpp)
- Clock input differentially driven; analog-input differentially driven
- Default mode: four-channel mode ON, binary output data format, Digital interface ON, 1:2 DMUX ON, Standby mode OFF, minimum bandwidth

Figure 7-1. Full Power Input Bandwidth (–1 dBFS Input in 500 mVpp Setting, Four-channel Mode, Fc = 2.5 GHz, Full Band Setting)

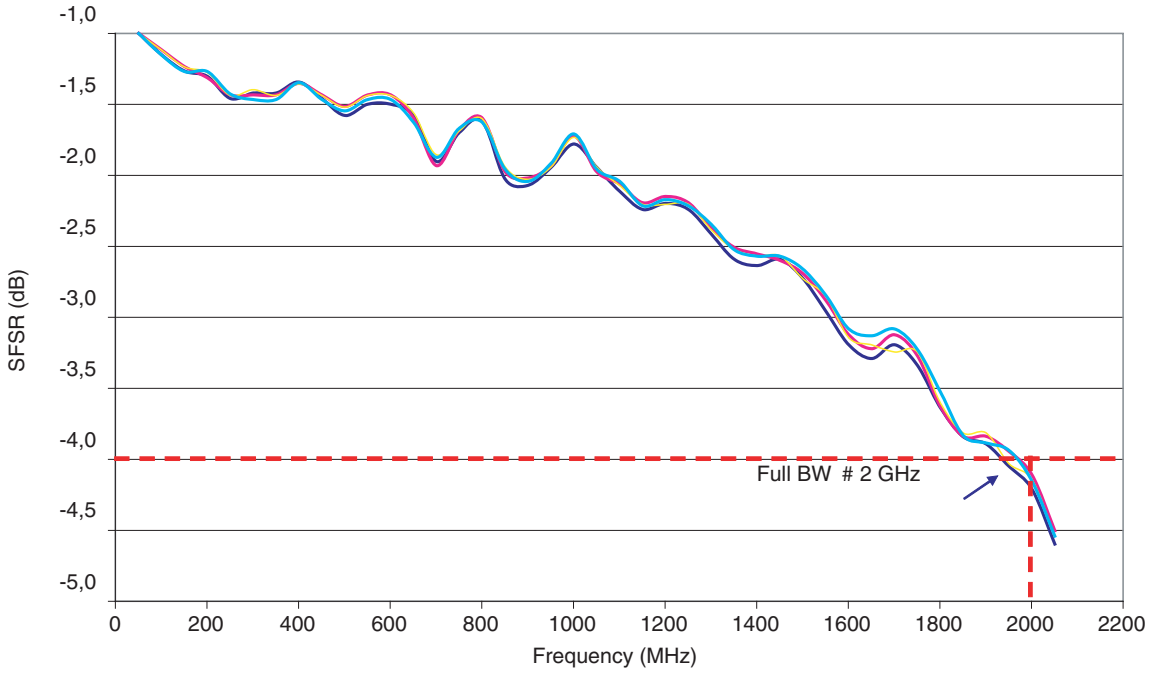


Figure 7-2. Crosstalk (Fc = 2.5 GHz, Channel A on Channel B)

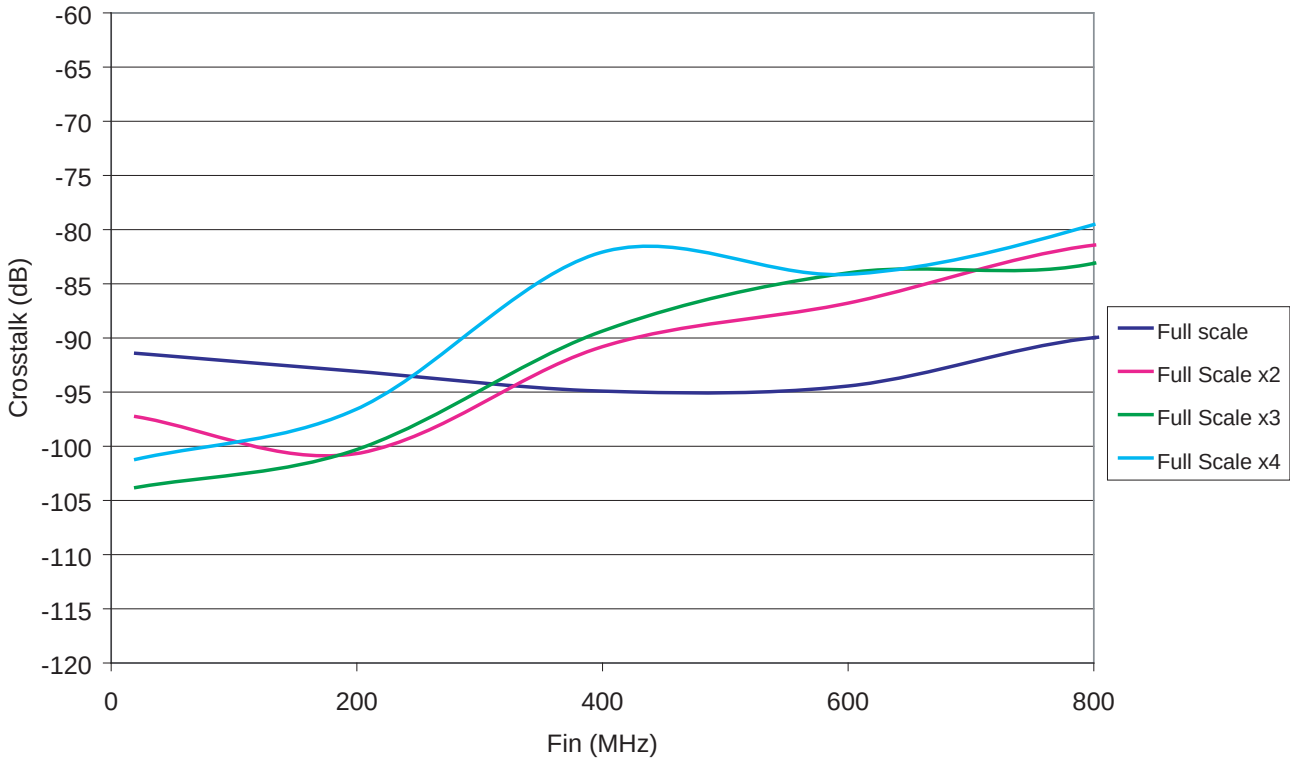


Figure 7-3. Crosstalk (Fc = 2.5 GHz, Channel B on Channel C)

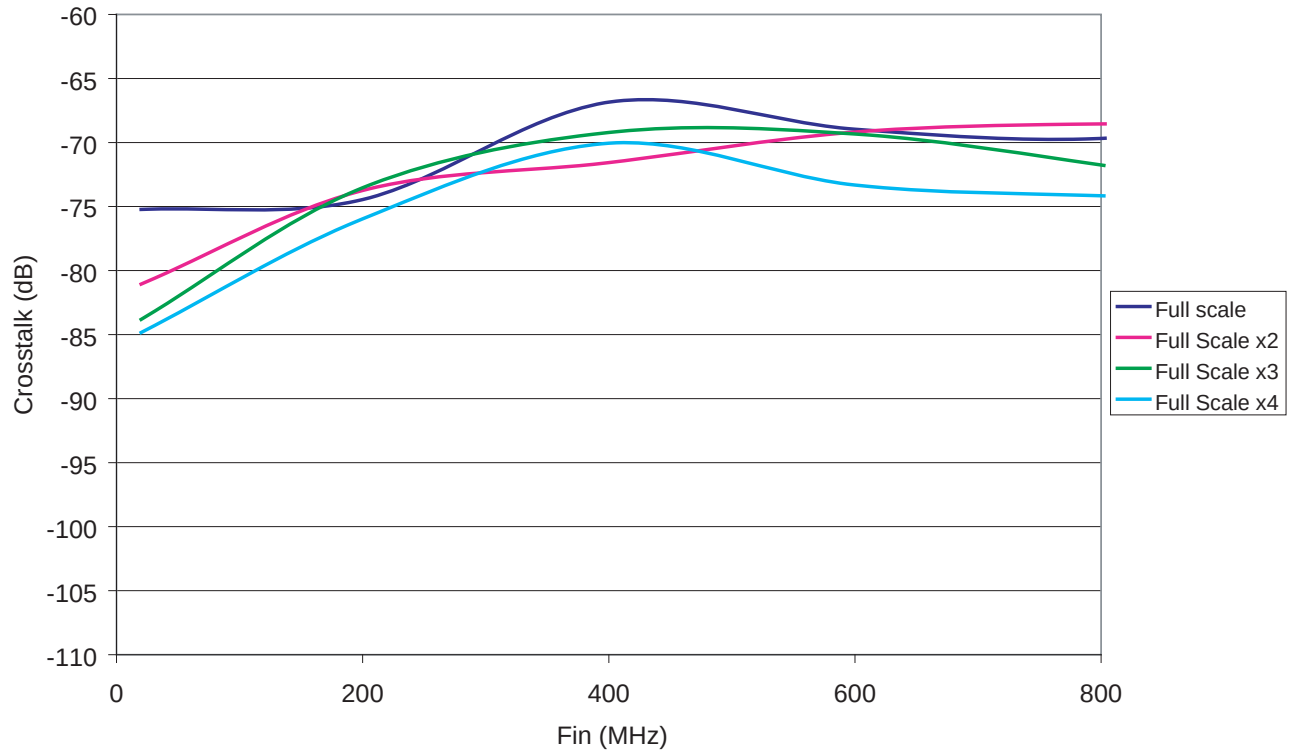


Figure 7-4. Step Response (Fc = 2.5 GHz, DMUX 1:2 Mode, Fin = 300 MHz)

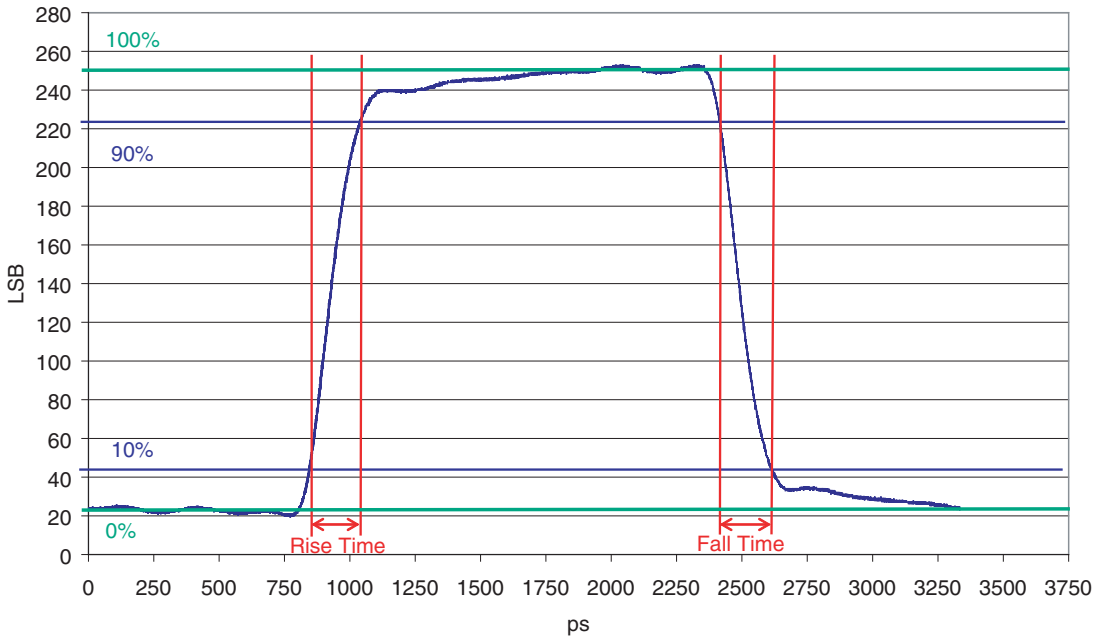
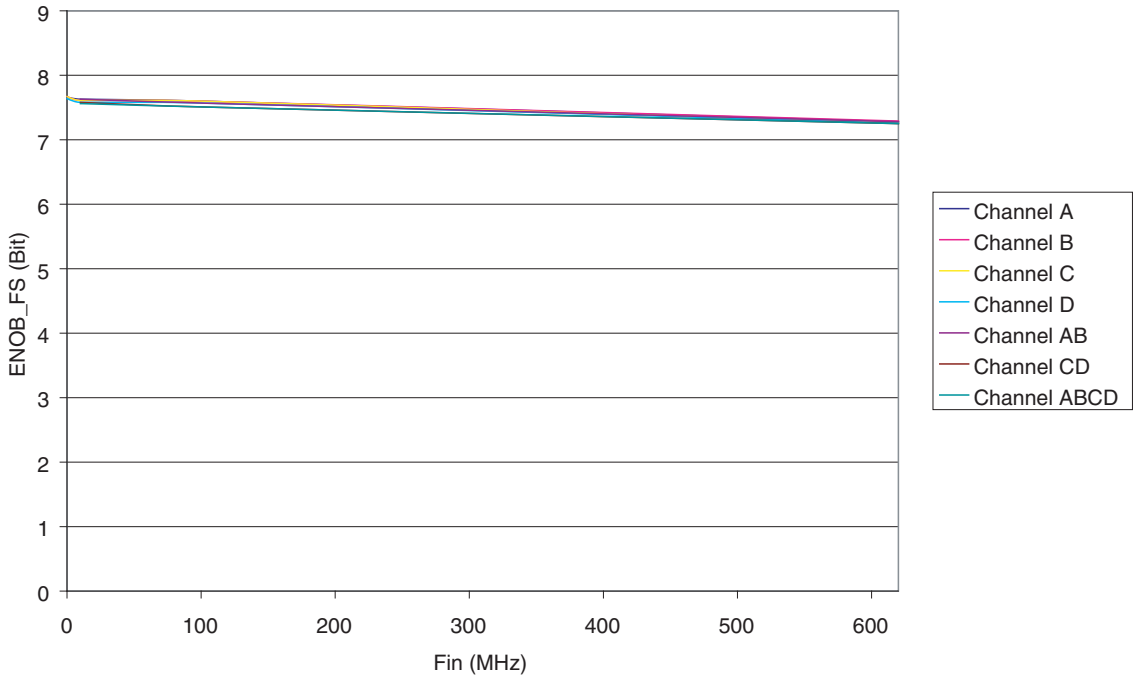


Figure 7-5. ENOB versus Input Frequency (Fc = 2.5 GHz)



0846J–BDC–03/16

Figure 7-6. SNR versus Input Frequency (Fc = 2.5 GHz)

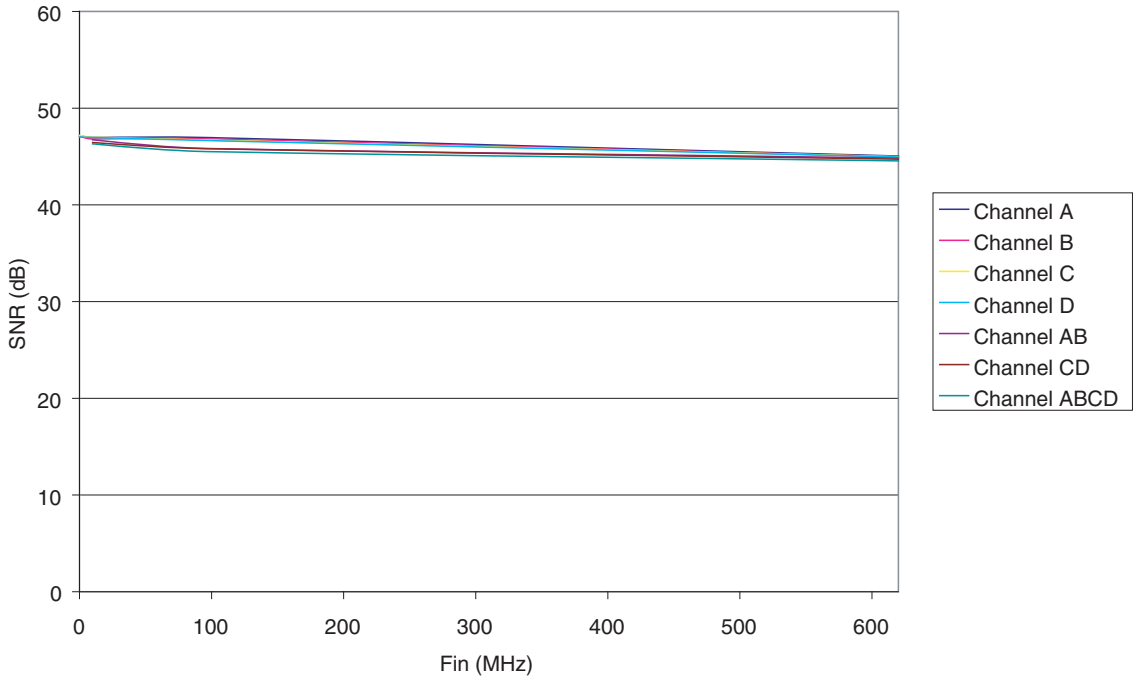


Figure 7-7. THD versus Input Frequency (Fc = 2.5 GHz)

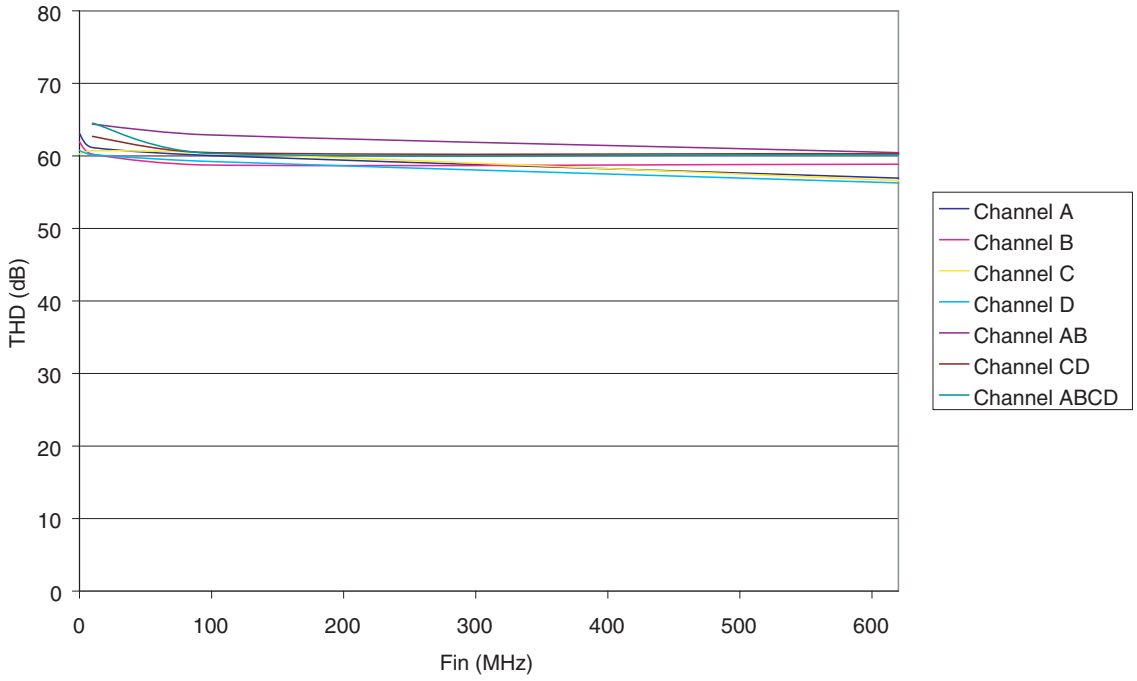


Figure 7-8. SFDR versus Input Frequency (Fc = 2.5 GHz)

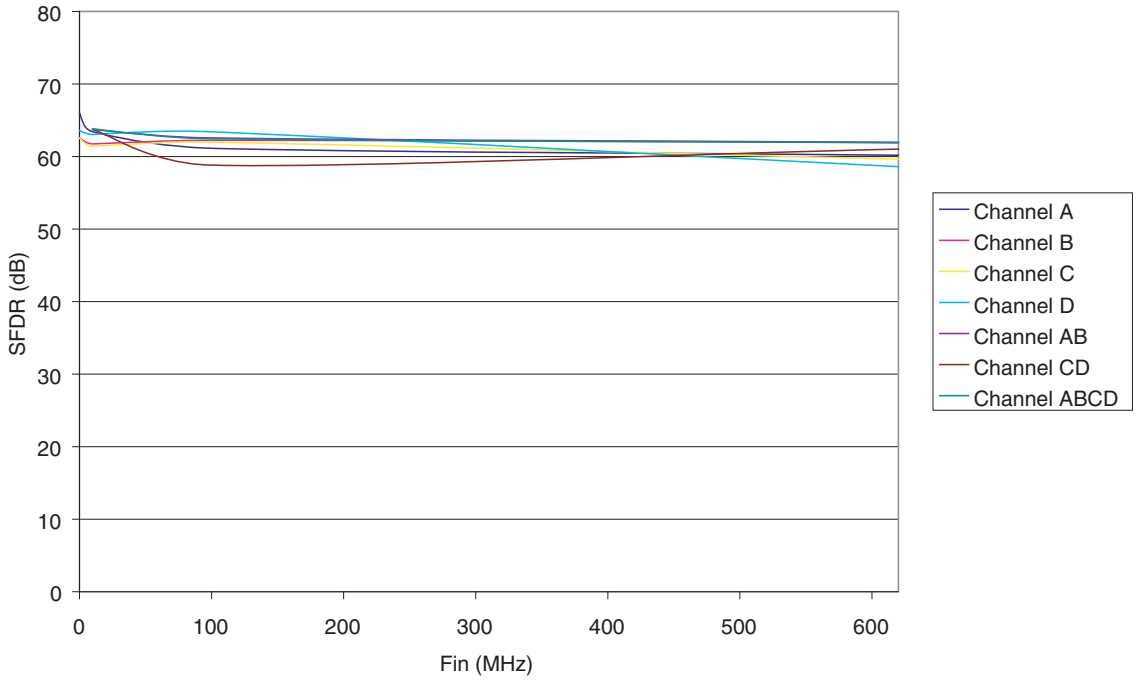


Figure 7-9. ENOB versus Sampling Frequency (Fin = 620 MHz)

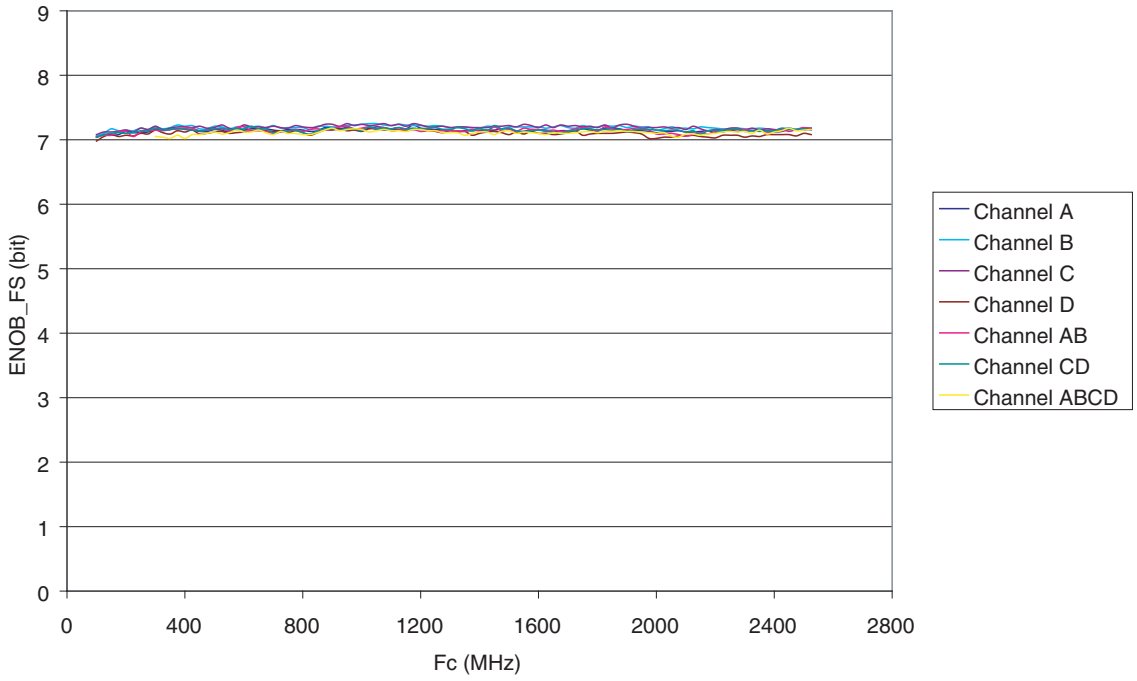


Figure 7-10. SNR versus Sampling Frequency (Fin = 620 MHz)

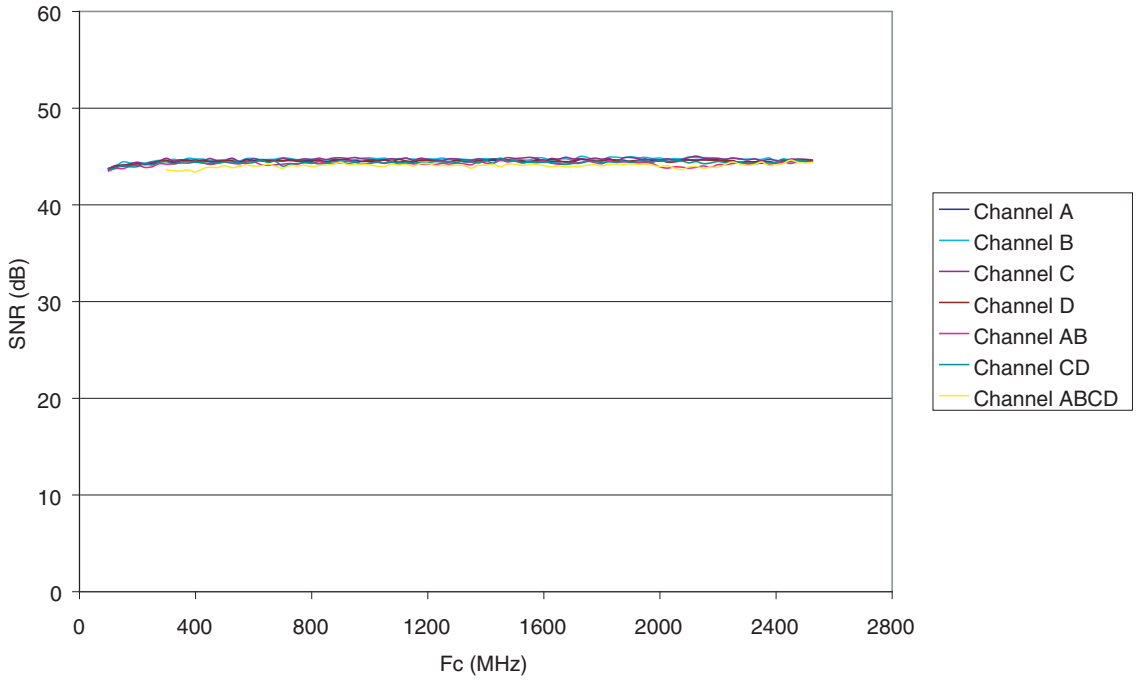


Figure 7-11. THD versus Sampling Frequency (Fin = 620 MHz)

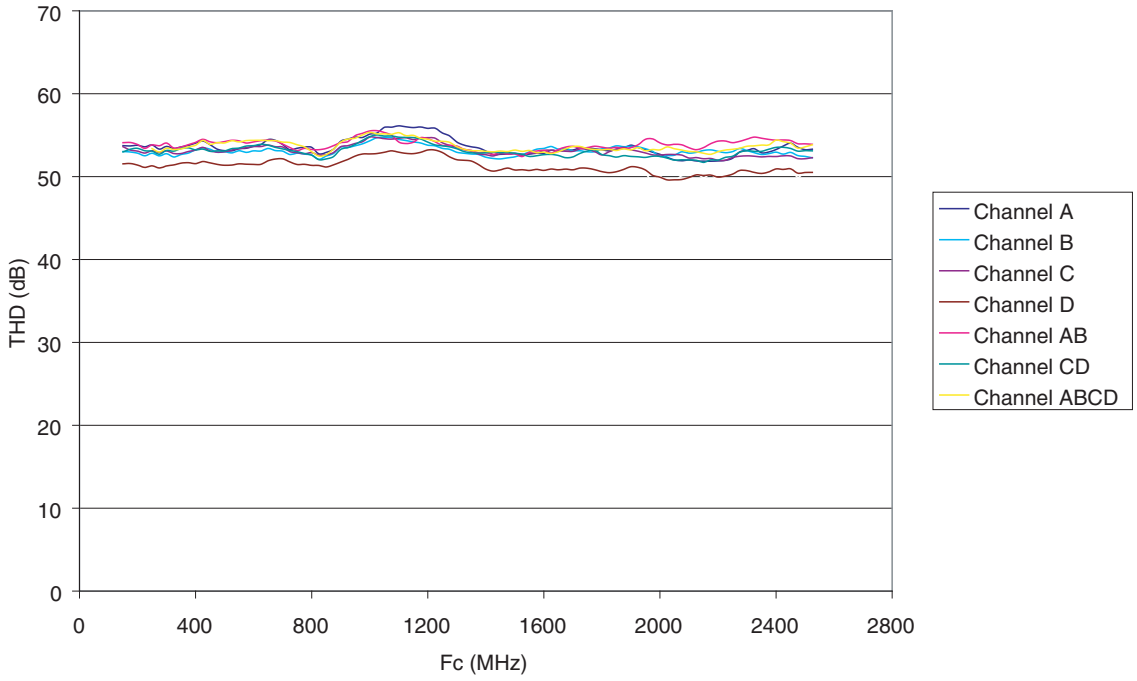


Figure 7-12. SFDR versus Sampling Frequency (Fin = 620 MHz)

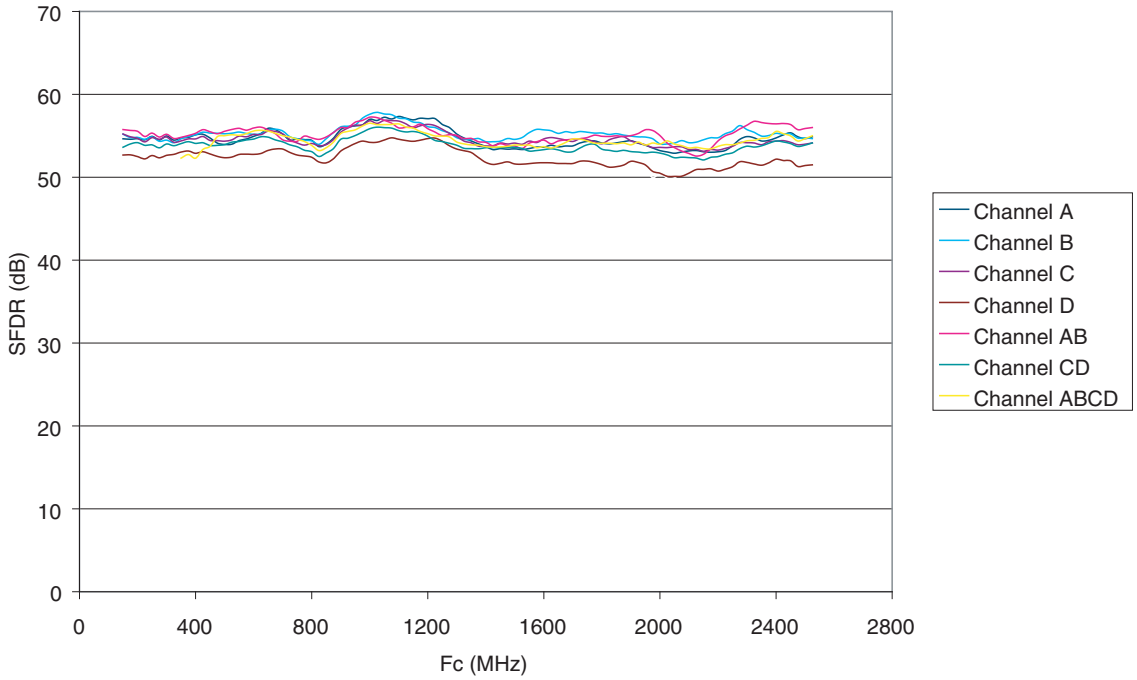


Figure 7-13. ENOB versus Power Supplies (Fc = 2.5 GHz, Fin = 100 MHz)

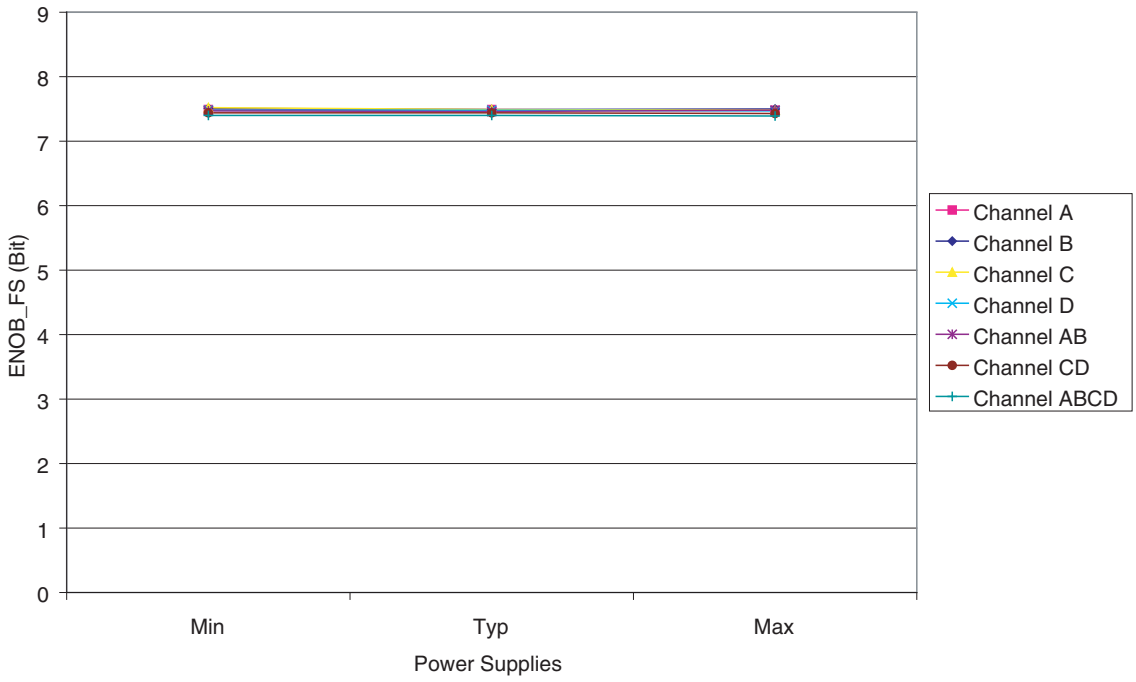


Figure 7-14. SNR versus Power Supplies (Fc = 2.5 GHz, Fin = 100 MHz)

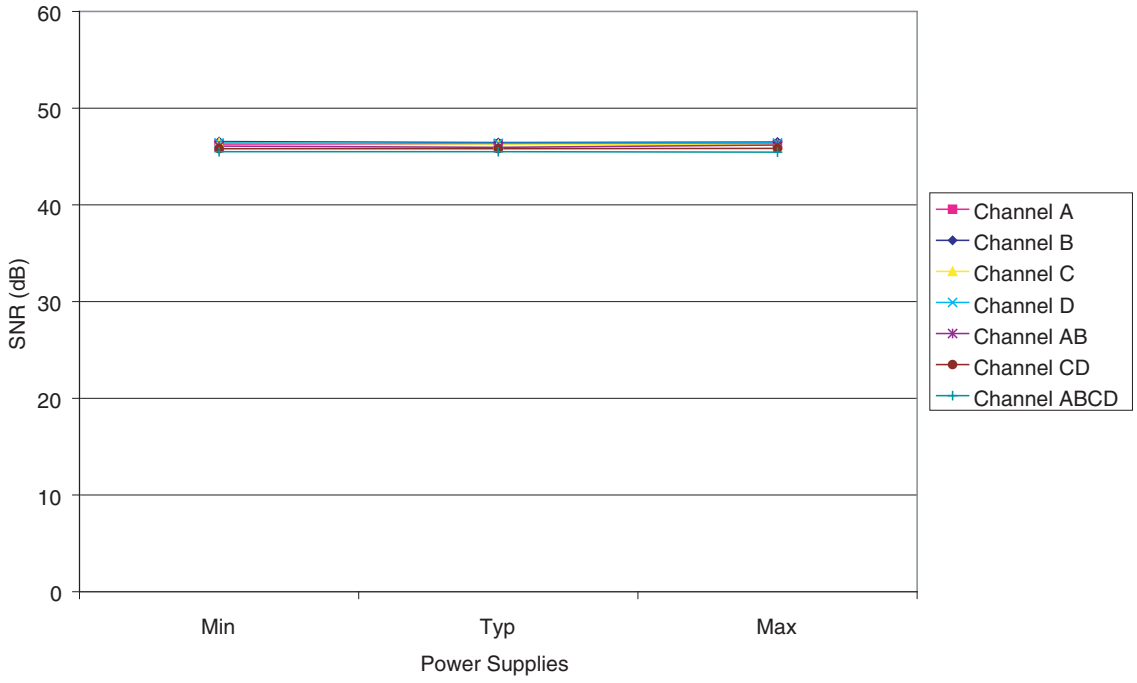


Figure 7-15. THD versus Power Supplies (Fc = 2.5 GHz, Fin = 100 MHz)

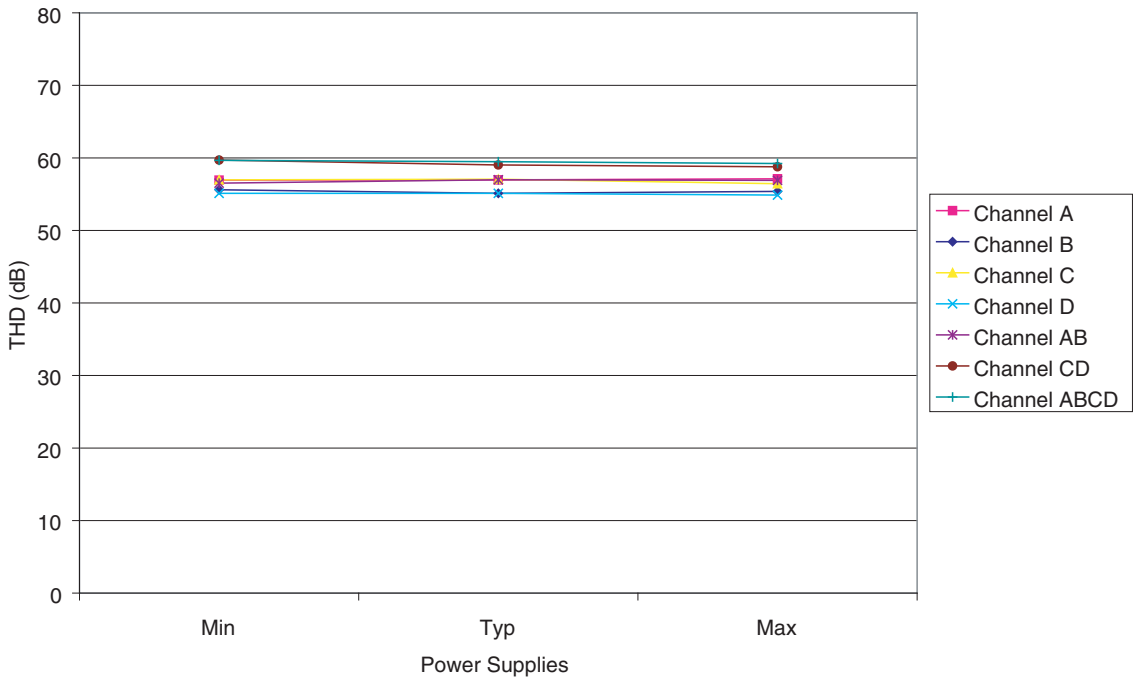


Figure 7-16. SFDR versus Power Supplies (Fc = 2.5 GHz, Fin = 100 MHz)

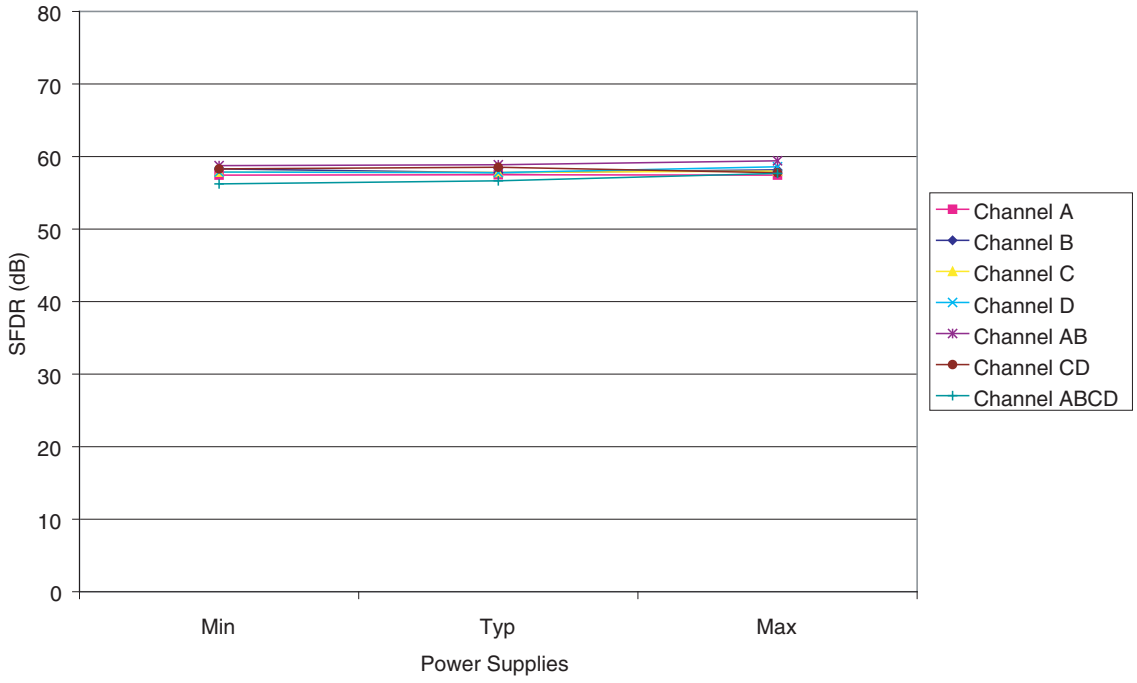


Figure 7-17. ENOB versus Temperature (Fc = 2.5 GHz, Fin = 100 MHz)

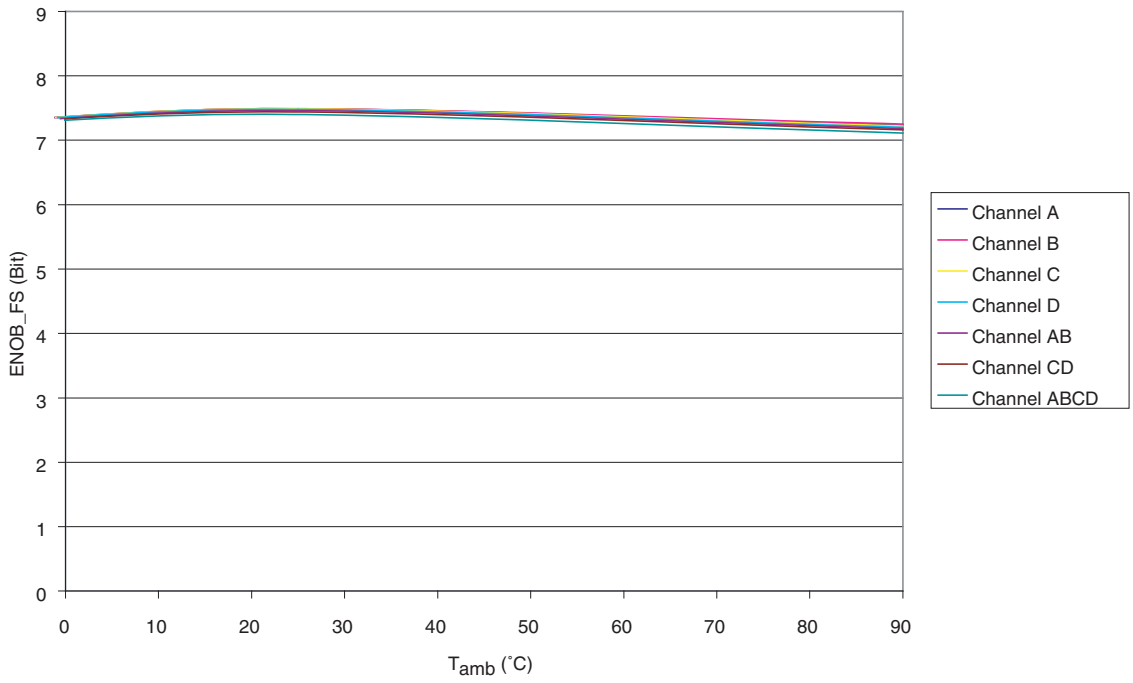


Figure 7-18. SNR versus Temperature (Fc = 2.5 GHz, Fin = 100 MHz)

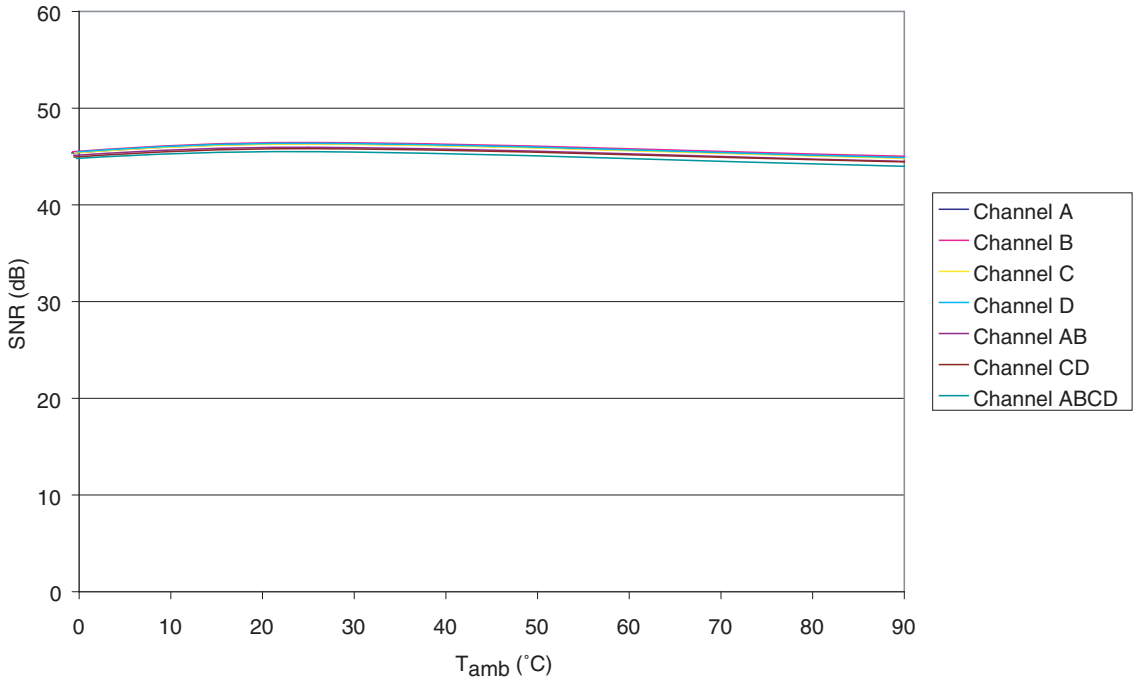


Figure 7-19. THD versus Temperature (Fc = 2.5 GHz, Fin = 100 MHz)

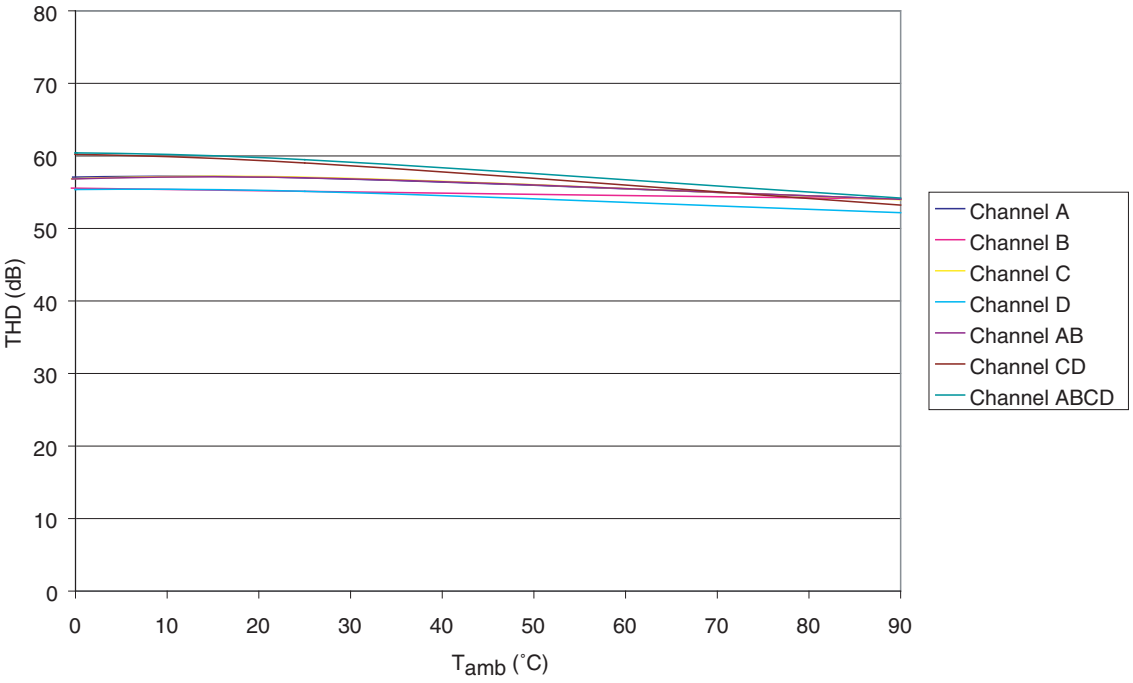


Figure 7-20. SFDR versus Temperature (Fc = 2.5 GHz, Fin = 100 MHz)

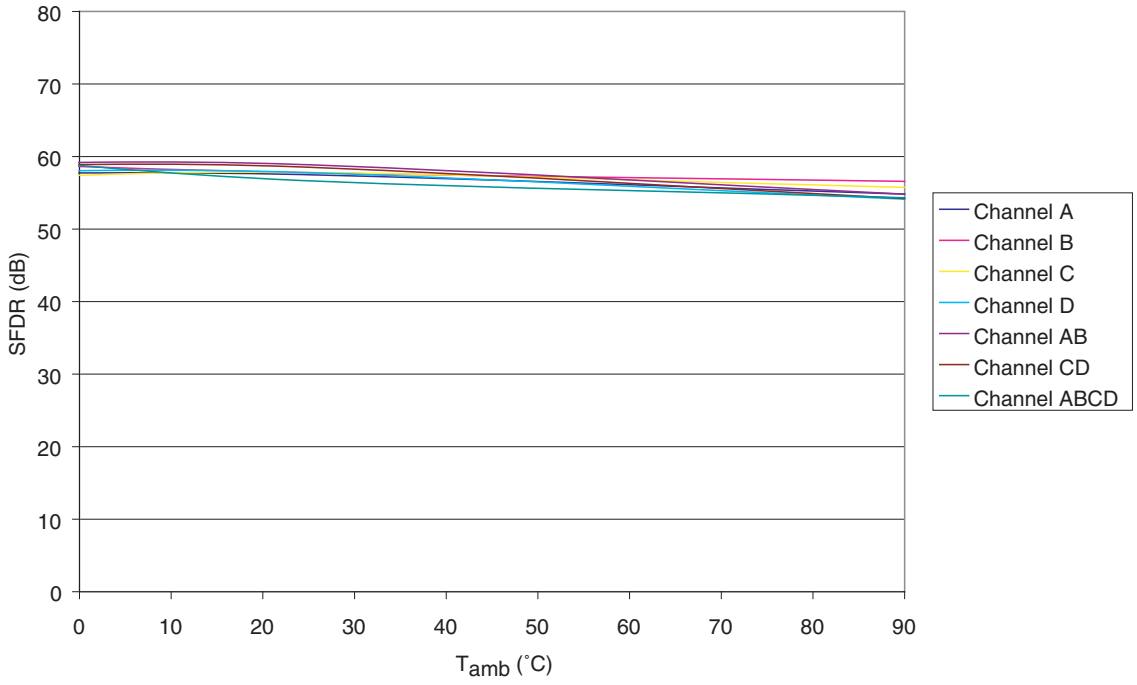
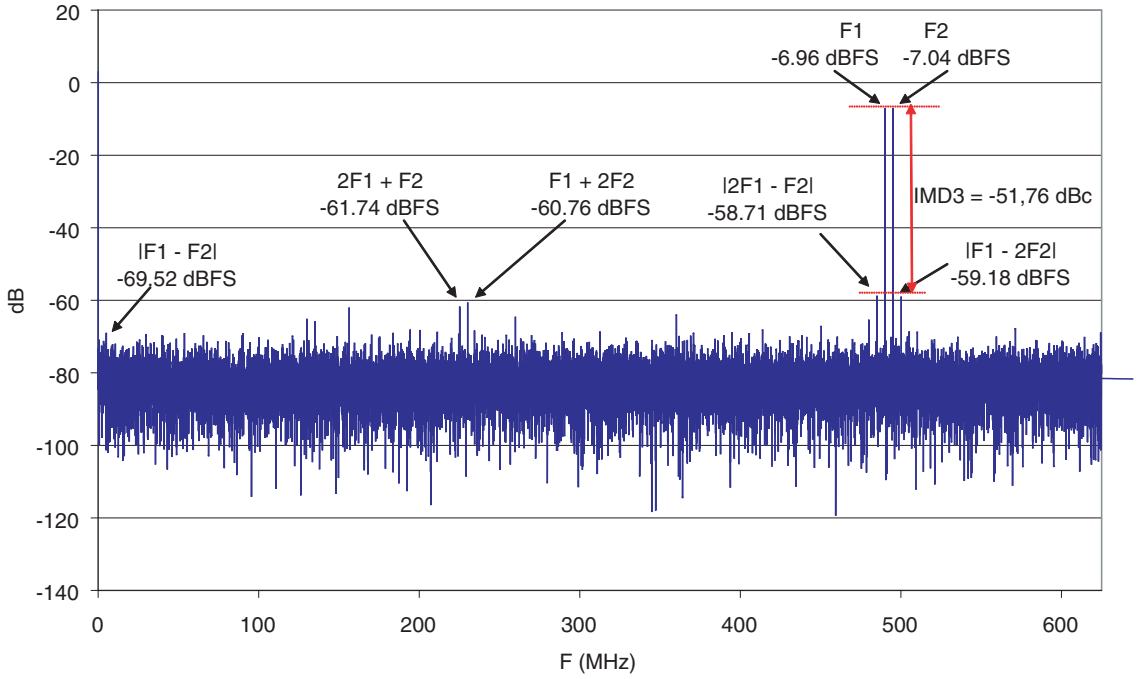


Figure 7-21. Dual Tone Signal Spectrum (Fc = 2.5 GHz, Fin1 = 490 MHz, Fin2 = 495 MHz) in Four-channel Mode



0846J–BDC–03/16

Figure 7-22. Dual Tone Signal Spectrum (Fc = 2.5 GHz, Fin1 = 490 MHz, Fin2 = 495 MHz) in Four-channel Mode

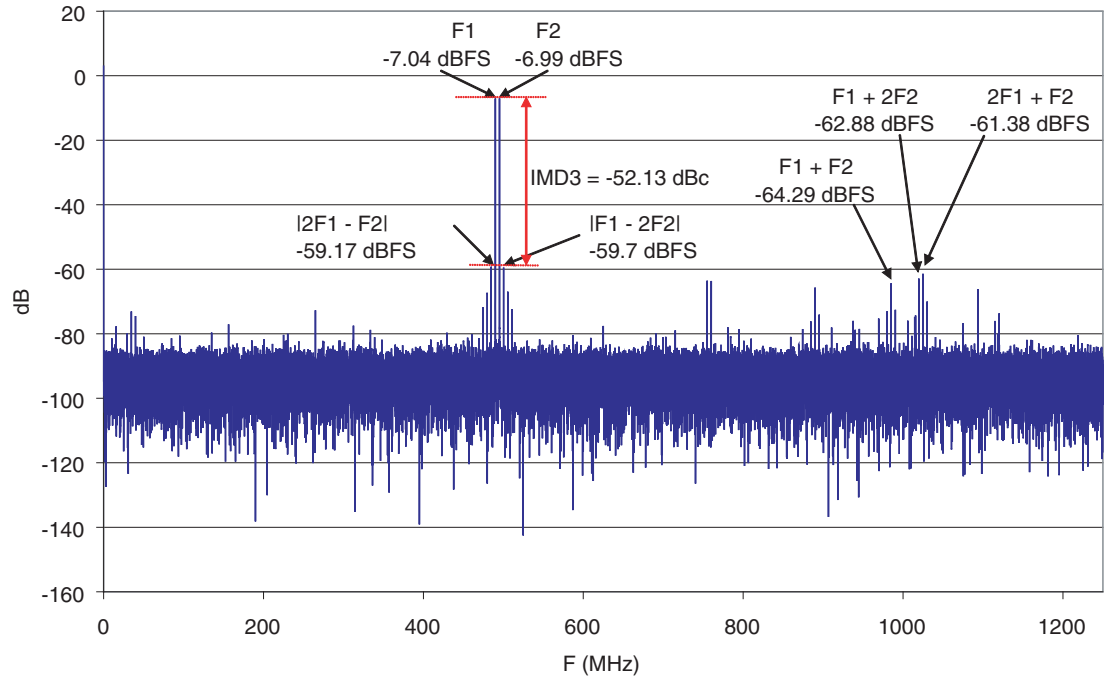
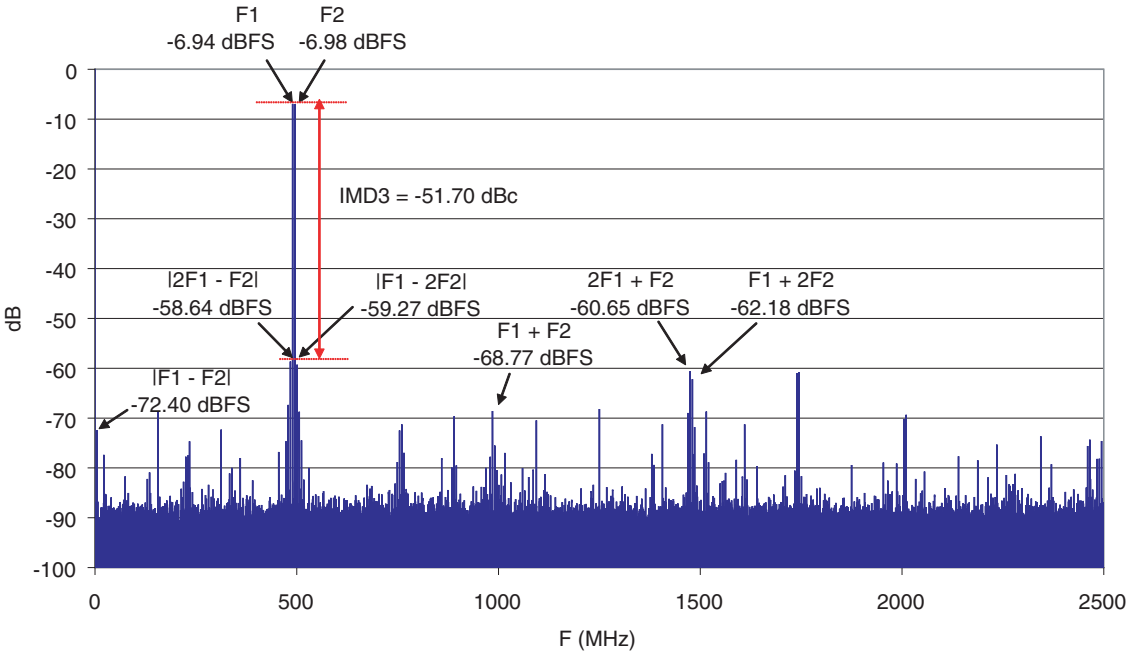


Figure 7-23. Dual Tone Signal Spectrum (Fc = 2.5 GHz, Fin1 = 490 MHz, Fin2 = 495 MHz) in One-channel Mode



8. FUNCTIONAL DESCRIPTION

Figure 8-1. Quad ADC Functional Diagram

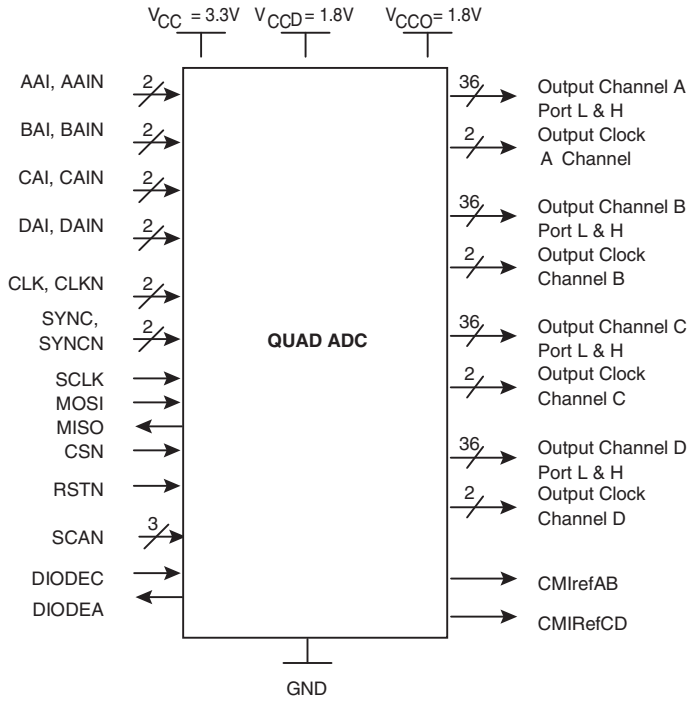


Table 8-1. Functions Description

Name	Function	Name	Function
V_{CCA}	3.3V Analog power supply	CLOR, CLORN	Channel C port L Differential out-of-range
V_{CCD}	1.8V Digital power supply	CHOR, CHORN	Channel C port H Differential out-of-range
V_{CCO}	1.8V Output power Supply	DLOR, DLORN	Channel D port L Differential out-of-range
GND	Ground	DHOR, DHORN	Channel D port H Differential out-of-range
AAI, AAIN	Channel A Differential analog Input	ADR, A DRN	Channel A Differential data ready
BAI, BAIN	Channel B Differential analog Input	BDR, BDRN	Channel B Differential data ready
CAI, CAIN	Channel C Differential analog input	CDR, CDRN	Channel C Differential data ready
DAI, DAIN	Channel D Differential analog Input	DDR, DDRN	Channel D Differential data ready
CLK,CLKN	Differential clock input	SYNC, SYNCN	Synchronization of data ready (LVDS)

Table 8-1. Functions Description (Continued)

Name	Function	Name	Function
[ALD0:ALD7][ALD0N:ALD7N]	Channel A port L Differential output data	SCLK	SPI Clock
[AHD0:AHD7][AHD0N:AHD7N]	Channel A port H Differential output data	MISO	Master In Slave Out SPI output MISO should be pulled up to Vcc using 1K - 3K3 resistor MISO not tristated when inactive
[BLD0:BLD7][BLD0N:BLD7N]	Channel B port L Differential output data	MOSI	Master Out Slave In SPI Input
[BHD0:BHD7] [BHD0N:BHD7N]	Channel B port H Differential output data	CSN	Chip select (active Low)
[CLD0:CLD7] [CLD0N:CLD7N]	Channel C port L Differential output data	RSTN	SPI asynchronous reset (active low)
[CHD0:CHD7][CHD0N:CHD7N]	Channel C port H Differential output data	SCAN<2:0>	Digital scan mode signal - for e2v use only
[DLD0:DLD7][DLD0N:DLD7N]	Channel D port L Differential output data	DIODEA	Diode Anode for die junction temperature monitoring
[DHD0:DHD7][DHD0N:DHD7N]	Channel D port H Differential output data	DIODEC	Diode Cathode for die junction temperature monitoring
ALOR, ALORN	Channel A port L Differential out-of-range	Tdreadyp, Tdreadyn, Trigp, Trign, Tdcop, Tdcon	Reserved pins
AHOR, AHORN	Channel A port H Differential out-of-range	Res50, Res62	50Ω and 62Ω reference resistor inputs
BLOR, BLORN	Channel B port L Differential out-of-range	CMIRefAB, CMIRefCD	Output reference for Input common mode channels A and B and channels C and D
BHOR, BHORN	Channel B port H Differential out-of-range		

8.1 ADC Synchronization Signal (SYNC, SYNCN)

The SYNC, SYNCN signal has LVDS electrical characteristics. It is active high and should last at least 2 clock cycles to work properly.

Once asserted, it has an effect on the output clock signals which are then forced to LVDS low level as described in Figure 8.2. During reset, the output data are not refreshed.

Once de-asserted, the output clock signals restart toggling after (TDR + pipeline delay) + Y clock cycles, where Y can be selected via the Serial Peripheral Interface at address 0x06 (from 0 to 15). This SYNC signal can be used to ensure the synchronization of multiple ADCs.

The SYNCN, SYNCP signal is mandatory whenever the following ADC modes are changed: Standby, DMUX mode, Test mode (see note [(3)]), channel mode. For all other ADC modes there is no need to perform a SYNCN, SYNCP.

Examples:

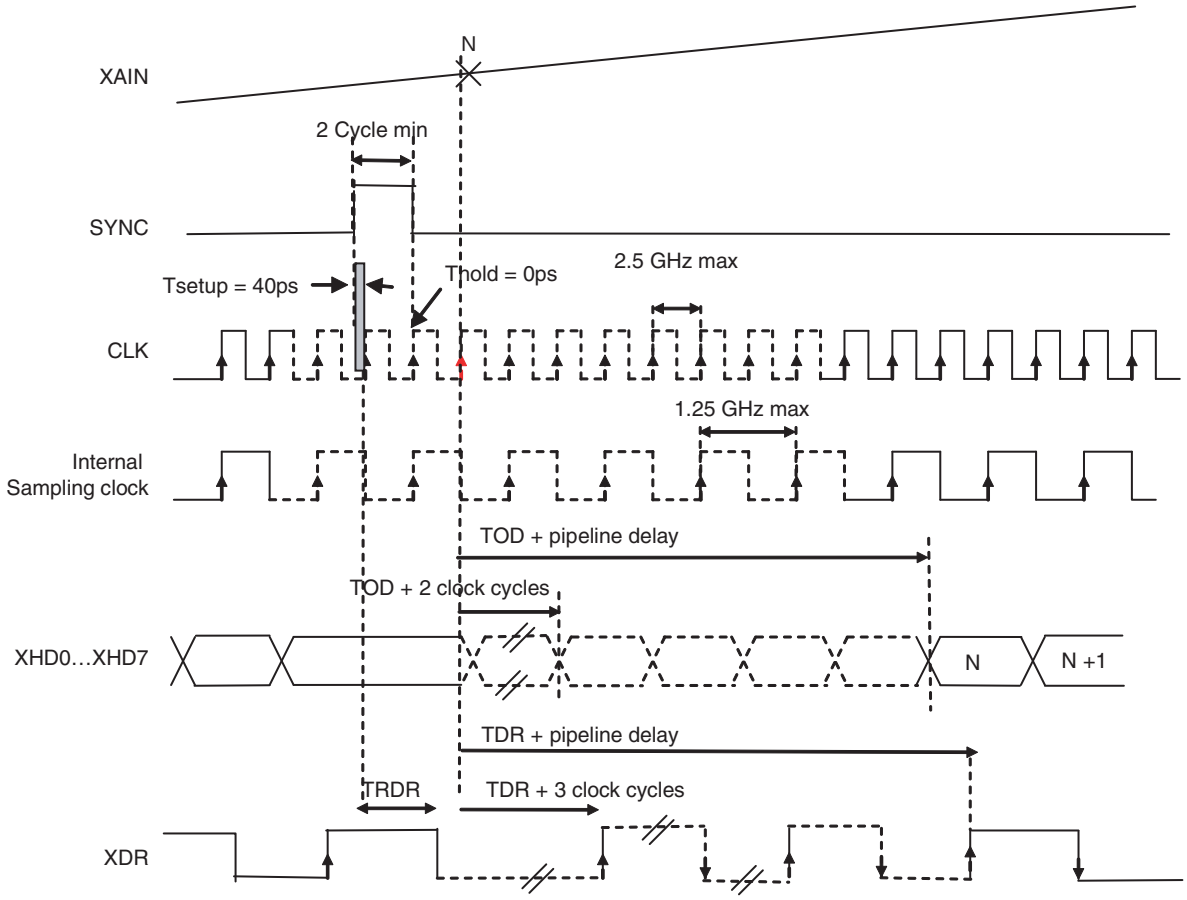
The SYNCN, SYNCP signal is mandatory after power up or power configuration: when switching the ADC from standby (full or partial) to normal mode.

The SYNCN, SYNCP signal is mandatory after channel mode configuration: when switching the ADC from 4-channel mode to 1-channel mode.

The SYNCN, SYNCP signal is mandatory after test sequence: when switching the ADC from normal running mode to ramp or flashing mode but it is no needed when the ADC is switched from test mode (ramp or flashing) to normal running mode.

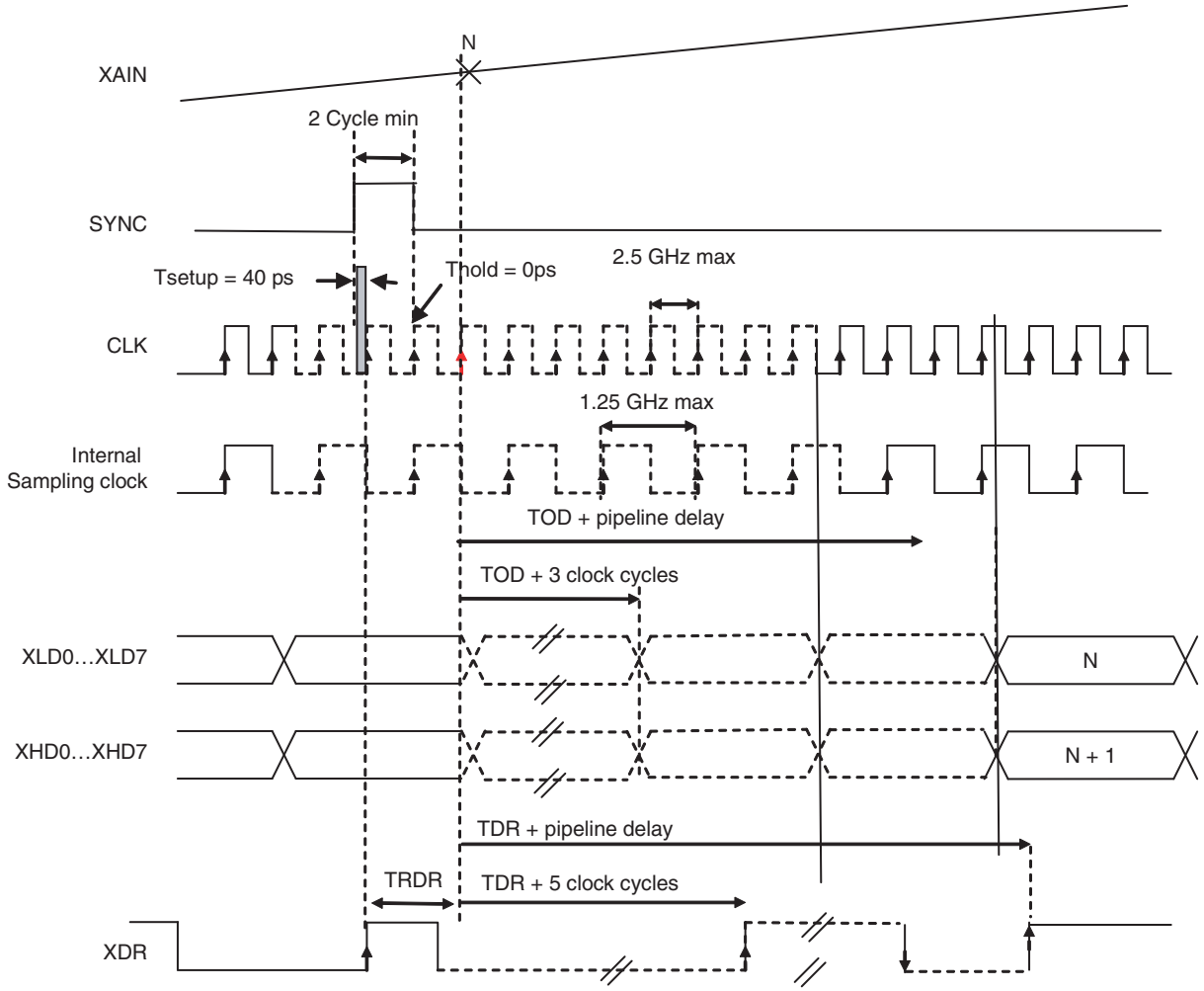
Notes:
1. In DMUX 1:2 mode, the SYNC, SYNCN signal also resets the clock divider for the DMUX.
2. In decimation mode, the SYNC, SYNCN signal also resets the clock dividers for decimation, therefore data outputs are not refreshed or may be corrupted when SYNC, SYNCN is active.
3. Refer to Figure 8-2.

Figure 8-2. ADC Timing in 4-Channel Mode, 1:1 DMUX Mode (For Each Channel)



Notes:
1. X refers to A, B, C and D. This timing has been built with no extra clock cycles (SPI address 0x06 label: SYNC, value = 0).
2. The first edges of output data Ready signal capture an old data (data held before SYNC time), the valid data (data N) arrives after pipeline delay (the number of invalid clock edges depend on ADC configuration).

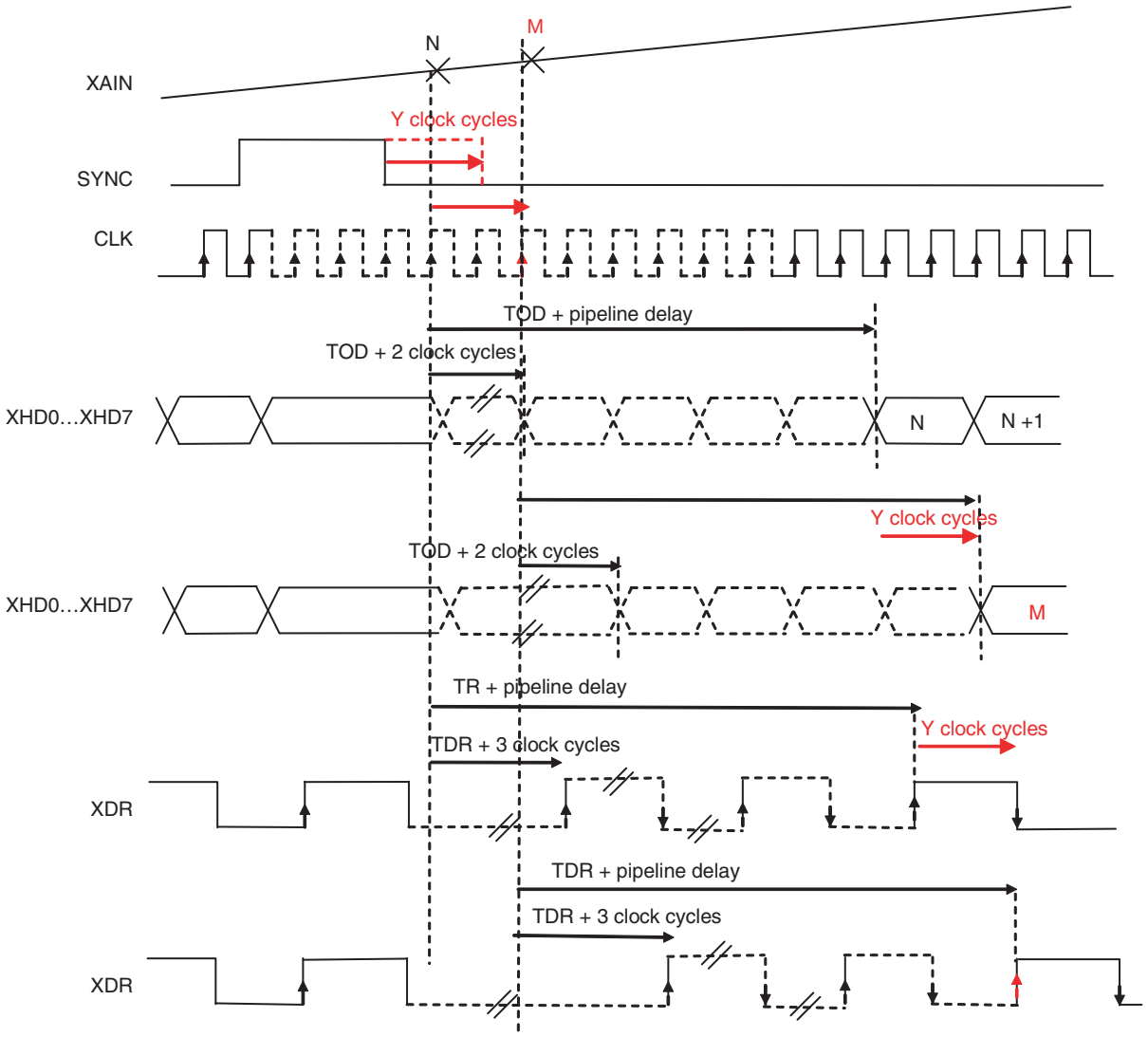
Figure 8-3. ADC Timing in 4-Channel Mode, 1:2 DMUX Mode (For Each Channel)



Notes:
1. X refers to A, B, C and D.
   This timing has been built with no extra clock cycles (SPI address 0x06 label: SYNC, value = 0).
2. The first edges of output data Ready signal capture an old data (data held before SYNC time), the valid data (data N) arrives after pipeline delay (the number of invalid clock edges depend on ADC configuration).

The extra clock configuration allows to delay the restart of output data and data ready after SYNC. With this extra clock delay, the validity range of SYNC signal is extended.

Figure 8-4. Output Data and Data Ready with Extra Delay Configuration



Note: X refers to A, B, C and D.
Y refers to the number of extra clock that can be added (Y = 0 to 15) with programming delay of ADC data ready after SYNC
See Section 8.7 ”Quad ADC Digital Interface (SPI)” on page 50, (register address 0x06).

0846J–BDC–03/16

8.2 Digital Reset (RSTN)

This is a global reset for the SPI register. It is active low. There are two ways to reset the Quad 8-bit 1.25 Gsps ADC:

- By asserting low the RSTN primary pad (hardware reset)
- By writing a “1” in the bit SWRESET of the SWRESET register through the SPI (software reset)

Both ways will clear *all* configuration registers to their reset values.

The RSTN is an asynchronous reset which acts on the SPI. If the RSTN is applied during an access (write or read) to the SPI, this access will be lost and default values will be written in the registers. The RSTN pulse should last at least 10 ns. This RSTN should be applied at power up of the chip (recommended before the clocks are applied).

8.3 Digital Scan Mode (SCAN[2:0])

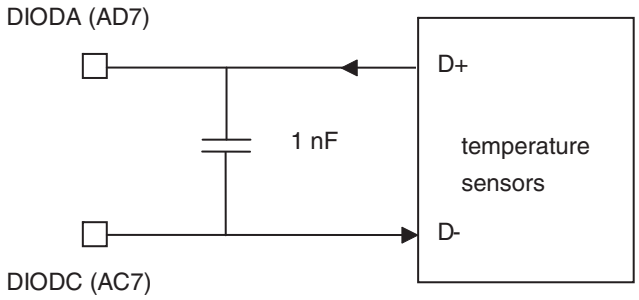
These signals allow to perform a scan of the digital part of the ADC.

- For e2v use only
- Pull up to V_{CC} with 4.7 KΩ

8.4 Die Junction Temperature Monitoring Diode

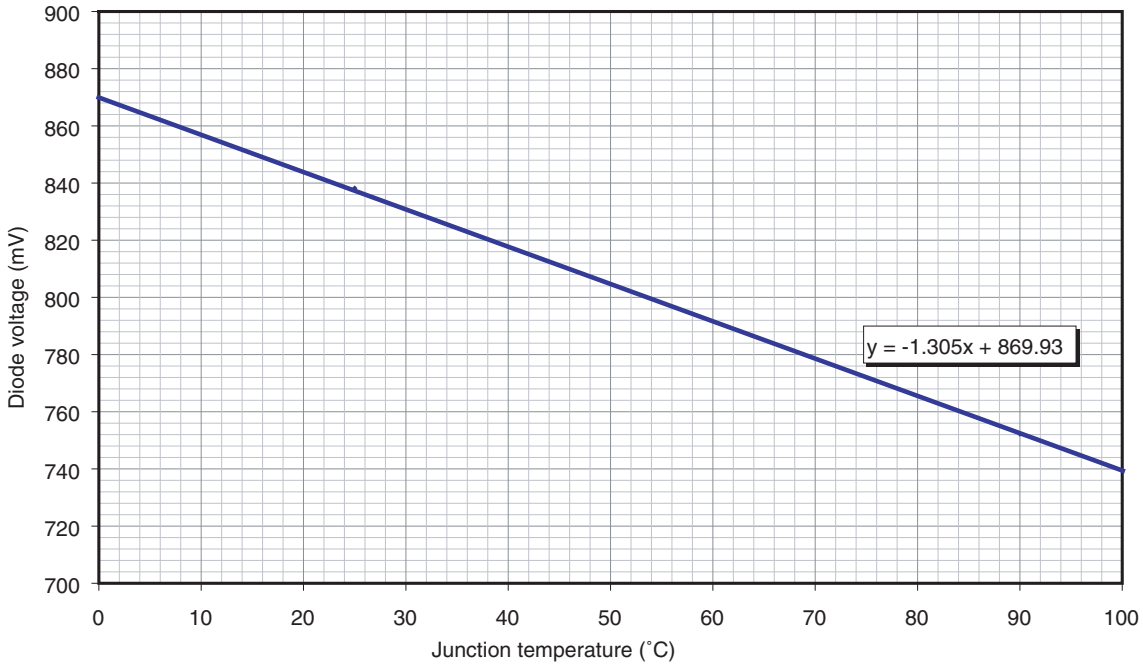
DIODEA, DIODEC: two pins are provided so that the diode can be probed using standard temperature sensors.

Figure 8-5. Junction Temperature Monitoring Diode System



Note: If the diode function is not used, DIODA and DIODC can be left unconnected (open).

Figure 8-6. Diode Characteristics (I = 1 mA)

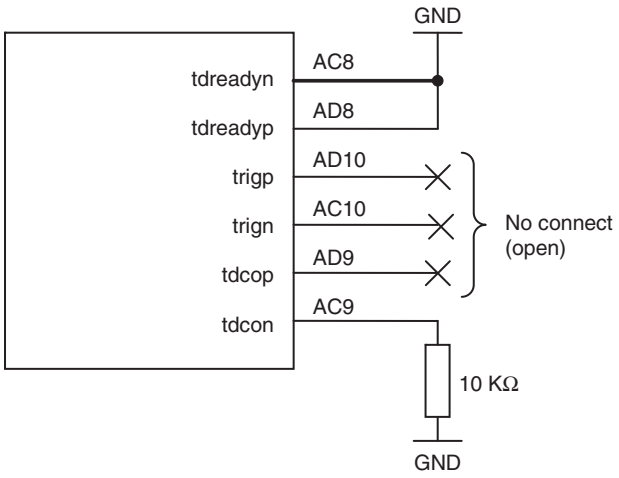


0846J–BDC–03/16

8.5 Test Signals

The reserved signals (trigp pin AD10, trign pin AC10, tdreadyp pin AD8, tdreadyn pin AC8, tdcop pin AD9 and tdcon pin AC9) should be connected as described in Figure 8-7.

Figure 8-7. Reserved Pins Recommended Implementation



8.6 Res50 and Res62

The two pins Res62 and Res50 are for checking the actual centering of the process.

The two point measurement reduces measurement errors .Since the current circulating through ground in normal operation is about 1.25A, a shift of 10mV on the pins RES62 and RES50 is consistent.

One way to get rid of the shift in IR-drop to ground when measuring RES62 of RES50 at actual operational temperature is to use a two step measurement (circuit being normally powered):

1. measure the voltage of these two pins regarding board ground without injecting any current (yields Vres62_0mA and Vres50_0mA, which should be at the same value: the actual ground level in die)
2. measure the voltage of these two pins regarding board ground injecting sequentially 2mA in these pins this yields Vres62_2ma and Vres50_2mA.

Subtracting the actual resistance would then yield R62=(Vres62_2 mA - Vres62_0 mA)/2 mA and measR50=(Vres50_2 mA - Vres50_0 mA)/2 mA. This should minimize the systematic error.

Note: when computing the systematic error an accumulated misreading of ±0.1 Ohm on measR50 and measRes62 can lead to a fluctuation of ±1 Ohm in the estimation of the systematic error e (for obvious physical reasons e cannot be negative, because it represents parasitic resistance between the measure resistor and the measurement apparatus), and of fluctuation of ±0.01666 in the estimation of k.

The measurement of actual input resistance is somehow easier since we have access to both terminals, but of course due to the trimming system this measurement must be performed with the ADC powered.

Performing the measurement as describe here above should reduce the discrepancy between computed value and measured value for input impedance(cf all resistors are now measured at similar temperatures).

Due to extra routing between pad and termination resistor for analog inputs the measured differential value should be ~2 Ohms above the computed value.

As a consequence we should revise the formula for input impedance given in section 7.7.12 as following:

R=1 + (121*k / (2 + 0.006*(8*bit3 + 4*bit2 + 2*bit1 + bit0))) where k is the computed value for RES62 and RES50 measurements, representing the process deviation from ideality (k=1 <==> perfectly centered process), and where the first term 1 is the serial parasitic resistor between pad and actual termination resistor.

The trimming is meant to compensate for die process deviation (accepted value by foundry is ±15%), after trimming it is always possible to reach the 50 Ohm (100 Ohm differential) value ± 2% which is consistent with accepted tolerance of discrete passive devices.

When the die process is well centered (that is when k is close enough to 1) no trimming is necessary (default programming is OK) except if due to PCB process issues the actual input trace impedance deviates significantly from 50 Ohm and need to me matched internally.

The same trimming value should be applied for parts yielding the same measured values for RES62 and RES50.

8.7 Quad ADC Digital Interface (SPI)

The digital interface is a standard SPI (3.3V CMOS) with:

- 8 bits for the address A[7] to A[0] including a R/W bit (A[7] = R/W and is the MSB)
- 16 bits of data D[15] to D[0] with D[15] the MSB

Five signals are required:

- SCLK for the SPI clock
- CSN for the Chip Select
- MISO for the Master In Slave Out SPI Output. MISO should be pulled up to Vcc using 1K – 3K3 resistor. Also MISO does not conform to full SPI specification and is not Tristated when inactive. For full details refer to EV8AQ application note.
- MOSI for the Master Out Slave In SPI Input
- RSTN for SPI RESET

The MOSI sequence should start with one R/W bit:

- R/W = 0 is a read procedure
- R/W = 1 is a write procedure (refer to timing diagram in Section 8.8.1)

8.7.1 Registers Description

Table 8-2. Registers Mapping

Address	Label	Description	R/W	Default Setting
Common Registers				
0x00	Chip ID	Chip ID and version	Read only	0x0119
0x01	Control Register	ADC mode (channel mode) Standby DMUX Binary/Gray Test mode ON/OFF Bandwidth selection Full scale selection	R/W	four-channel mode (1.25 Gsps) No standby DMUX 1:2 Binary coding Test mode OFF Min bandwidth 500 mVpp full scale

Table 8-2. Registers Mapping (Continued)

Address	Label	Description	R/W	Default Setting
0x02	STATUS	Status register	Read only	
0x04	SWRESET	Software SPI reset	R/W	No reset
0x05	TEST	Test Mode	R/W	Test pattern = ramp
0x06	SYNC	Programmable delay on ADC data ready after Reset SYNC, SYNCN (4 bits)	R/W	0 extra clock cycle
0x0F	Channel Select	Channel X Selection	R/W	0x0000
Per Channel Registers (X=A/B/C/D)				
0x10	Cal Ctrl X	Calibration control register of Channel X	R/W	
0x11	Cal Ctrl X Mlbx	Status/Busy of current Calibration of channel X	Read only (poll)	
0x12	Status X	Global status of channel X	Read only	
0x13	Trimmer X	Impedance Trimmer of channel X	R/W	0x08
0x20	Ext Offset X	External offset Adjustment of channel X	R/W	0 LSB
0x21	Offset X	Offset adjustment of channel X	Read only	0 LSB
0x22	Ext Gain X	External Gain Adjustment of channel X	R/W	0 dB
0x23	Gain X	Gain adjustment of channel X	Read only	0 dB
0x24	Ext Phase X	External phase Adjustment of channel X	R/W	0 ps
0x25	Phase X	Phase adjustment of channel X	Read only	0 ps
0x30 to 0x32	Ext INL1 X	External first level INL Adjustment of channel X (3x16bits)	R/W	0x0000 (no INL correction)
0x33 to 0x35	Ext INL2 X	External second level INL Adjustment of channel X (3x16bits)	R/W	0x0000 (no INL correction)
0x36 to 0x38	INL1 X	1st level INL Adjustment of Channel X (3x16bits)	Read Only	0x0000
0x39 to 0x3B	INL2 X	2nd level INL Adjustment of Channel X (3x16bits)	Read Only	0x0000

Notes: 1. All registers are 16 bits long.

2. The *external* gain/offset/phase adjustment registers correspond to the registers where one can write the external values to calibrate the gain/offset/phase parameters of the ADCs. The Gain/offset/phase adjustment registers are read only registers. They provide you with the internal settings for the gain/offset/phase parameters. The *externa*l and read only adjustment registers should give the same results two by two once any calibration has been performed.

8.7.2 Chip ID Register (Read Only)

Table 8-3. Chip ID Register Mapping: Address 0x00

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TYPE								BRANCH<3:0>				MAJVERS<1:0>		MINVERS<1:0>	

Table 8-4. Chip ID Register Description

Bit label	Value	Description	Default Setting
MINVERS <1:0>		Minor version number	00
MAJVERS<1:0>		Major version number	10
BRANCH<3:0>		Branch number	0001
TYPE<7:0>		Chip type	00000001

8.7.3 Control Register

Table 8-5. Control Register Mapping: Address 0x01

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UNUSED		RESERVED	TEST	RESERVED	FS	BDW<1:0>		B/G	DMUX	STDBY <1:0>		ADCMODE <3:0>			

Table 8-6. Control Register Description

Bit label	Value	Description	Default Setting
ADCMODE <3:0>	00XX	Four-channels mode (1.25 Gsps per channel)	0000 Four-channels Mode
	0100	Two-channel mode (channel A and channel C, 2.5 Gsps per channel)	
	0101	Two-channel mode (channel B and channel C, 2.5 Gsps per channel)	
	0110	Two-channel mode (channel A and channel D, 2.5 Gsps per channel)	
	0111	Two-channel mode (channel B and channel D, 2.5 Gsps per channel)	
	1000	One-channel mode (channel A, 5 Gsps)	
	1001	One-channel mode (channel B, 5 Gsps)	
	1010	One-channel mode (channel C, 5 Gsps)	
	1011	One-channel mode (channel D, 5 Gsps)	
	1100	Common input mode, simultaneous sampling (channel A)	
	1101	Common input mode, simultaneous sampling (channel B)	
	1110	Common input mode, simultaneous sampling (channel C)	
	1111	Common input mode, simultaneous sampling (channel D)	

Table 8-6. Control Register Description (Continued)

Bit label	Value	Description	Default Setting
STDBY <1:0>	00	Full Active Mode	00 Full Active Mode
	01	Standby channel A/channel B: If four-channel mode selected then standby of channel A and B If two-channel mode selected, standby of channel A or B If one-channel mode selected then full standby	
	10	Standby channel C/channel D if four-channel mode selected then standby of channel C and D if two-channels mode selected, standby of channel C or D if one-channel mode selected then full standby	
	11	Full standby	
DMUX	0	1:2 DMUX	0 1:2 DMUX
	1	1:1 DMUX	
B/G	0	Binary	0 Binary coding
	1	Gray	
BDW <1:0>	00	Minimum bandwidth (500 MHz typical)	00 Min bandwidth
	01	Reduced bandwidth (600 MHz typical)	
	10	Nominal bandwidth (1.5 GHz typical)	
	11	Full bandwidth (2 GHz typical)	
FS	0	500 mVpp Full scale	0 500 mVpp full scale
	1	625 mVpp full scale	
TEST	0	No test mode	0 No Test Mode
	1	Test mode activated, refer to the test register	

Table 8-7. Control Register Settings (Address 0x01): Bit7 to Bit0

Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Label	**B/G**	**DMUX**	**STDBY <1:0>**		**ADCMODE <3:0>**			
Four-channel mode 1.25 Gsps max. per channel	X	X	X	X	0	0	X	X
Two-channel mode (channel A and channel C)2.5 Gsps max. per channel	X	X	X	X	0	1	0	0
Two-channel mode (channel B and channel C)2.5 Gsps max. per channel	X	X	X	X	0	1	0	1
Two-channel mode (channel A and channel D)2.5 Gsps max. per channel	X	X	X	X	0	1	1	0
Two-channel mode (channel B and channel D)2.5 Gsps max. per channel	X	X	X	X	0	1	1	1
One-channel mode (channel A, 5 Gsps max)	X	X	X	X	1	0	0	0
One-channel mode (channel B, 5 Gsps)	X	X	X	X	1	0	0	1
One-channel mode (channel C, 5 Gsps)	X	X	X	X	1	0	1	0
One-channel mode (channel D, 5 Gsps)	X	X	X	X	1	0	1	1
Simultaneous sampling (channel A)(Note:)	X	X	X	X	1	1	0	0

Table 8-7. Control Register Settings (Address 0x01): Bit7 to Bit0 (Continued)

Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Label	**B/G**	**DMUX**	**STDBY <1:0>**		**ADCMODE <3:0>**			
Simultaneous sampling (channel B)(Note:)	X	X	X	X	1	1	0	1
Simultaneous sampling (channel C)(Note:)	X	X	X	X	1	1	1	0
Simultaneous sampling (channel D)(Note:)	X	X	X	X	1	1	1	1
No standby (except if ADCMODE = 11XX)	X	X	0	0	X	X	X	X
Standby channel A, channel B	X	X	0	1	X	X	X	X
Standby channel C, channel D	X	X	1	0	X	X	X	X
Full Standby	X	X	1	1	X	X	X	X
1:2 DMUX mode	X	0	X	X	X	X	X	X
1:1 DMUX mode	X	1	X	X	X	X	X	X
Binary coding	0	X	X	X	X	X	X	X
Gray coding	1	X	X	X	X	X	X	X

Note: When bit3 bit2 = 11, the external clock signal and analog input signal are applied internally to the four ADC cores. The value of bit1 bit0 gives the channel on which the analog input should be applied.

Table 8-8. Control Register Settings (Address 0x00): Bit15 to Bit8

Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Label	**Unused**	**Unused**	**Reserved**	**TEST**	**Reserved**	**FS**	**BDW<1:0>**	
Min. bandwidth	X	X	0	X	0	X	0	0
Reduced bandwidth	X	X	0	X	0	X	0	1
Nominal bandwidth	X	X	0	X	0	X	1	0
Full bandwidth	X	X	0	X	0	X	1	1
500 mVpp full scale	X	X	0	X	0	0	X	X
625 mVpp full scale	X	X	0	X	0	1	X	X
Test mode OFF	X	X	0	0	0	X	X	X
Test mode ON	X	X	0	1	0	X	X	X

Table 8-9. ADCMODE and STBY Allowed Combinations

Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Label	**B/G**	**DMUX**	**STDBY <1:0>**		**ADCMODE <3:0>**			
Four-channel mode, 1.25 Gsps max No standby	X	X	0	0	0	0	X	X
Four-channel mode,1.25 Gsps max Standby channel A, channel B	X	X	0	1	0	0	X	X
Four-channel mode, 1.25 Gsps max Standby channel C, channel D	X	X	1	0	0	0	X	X
Four-channel mode (1.25 Gsps max) Full Standby	X	X	1	1	0	0	X	X
Two-channel mode, 2.5 Gsps max (Channels A and C) No Standby	X	X	0	0	0	1	0	0
Two-channels mode, 2.5 Gsps max (Channels A and C) Standby channel A	X	X	0	1	0	1	0	0
Two-channel mode, 2.5 Gsps max (Channels A and C) Standby Channel C	X	X	1	0	0	1	0	0
Two-channel mode, 2.5 Gsps max (Channels A and C) Full Standby	X	X	1	1	0	1	0	0
Two-channel mode, 2.5 Gsps max (Channels B and C) No Standby	X	X	0	0	0	1	0	1
Two-channel mode, 2.5 Gsps max (Channels B and C) Standby Channel B	X	X	0	1	0	1	0	1
Two-channel mode, 2.5 Gsps max (Channels B and C) Standby Channel C	X	X	1	0	0	1	0	1
Two-channel mode, 2.5 Gsps max (Channels B and C) Full Standby	X	X	1	1	0	1	0	1
Two-channel mode, 2.5 Gsps max (Channel A and D) No Standby	X	X	0	0	0	1	1	0
Two-channel mode, 2.5 Gsps max (Channels A and D) Standby Channel A	X	X	0	1	0	1	1	0
Two-channel mode, 2.5 Gsps max (Channels A and D) Standby Channel D	X	X	1	0	0	1	1	0
Two-channel mode, 2.5 Gsps max (Channels A and D) Full standby	X	X	1	1	0	1	1	0
Two-channel mode, 2.5 Gsps max (Channels B and D) No standby	X	X	0	0	0	1	1	1
Two-channel mode, 2.5 Gsps max (Channels B and D) Standby channel B	X	X	0	1	0	1	1	1
Two-channel mode, 2.5 Gsps max (channels B and D) Standby channel D	X	X	1	0	0	1	1	1
Two-channel mode, 2.5 Gsps max (channels B and D) Full standby	X	X	1	1	0	1	1	1
One-channel mode (channel A, 5 Gsps max) No standby	X	X	0	0	1	0	0	0
One-channel mode (channel B, 5 Gsps max) No standby	X	X	0	0	1	0	0	1

Table 8-9. ADCMODE and STBY Allowed Combinations (Continued)

Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Label	**B/G**	**DMUX**	**STDBY <1:0>**		**ADCMODE <3:0>**			
One-channel mode (channel C, 5 Gsps max) No standby	X	X	0	0	1	0	1	0
One-channel mode (channel D, 5 Gsps) No standby	X	X	0	0	1	0	1	1
One-channel mode (channel A, 5 Gsps) Full standby	X	X	01 or 10 or 11		1	0	0	0
One-channel mode (channel B, 5 Gsps) Full standby	X	X	01 or 10 or 11		1	0	0	1
One-channel mode (Channel C, 5 Gsps) Full standby	X	X	01 or 10 or 11		1	0	1	0
One-channel mode (Channel D, 5 Gsps) Full standby	X	X	01 or 10 or 11		1	0	1	1
Common input mode (Channel A, 1.25 Gsps) No standby	X	X	0	0	1	1	0	0
Common input mode (Channel B, 1.25 Gsps) No standby	X	X	0	0	1	1	0	1
Common input mode (Channel C, 1.25 Gsps) No standby	X	X	0	0	1	1	1	0
Common input mode (Channel D, 1.25 Gsps) No standby	X	X	0	0	1	1	1	1
Common input mode (Channel A, 1.25 Gsps) Full standby	X	X	01 or 10 or 11		1	1	0	0
Common input mode (Channel B, 1.25 Gsps) Full standby	X	X	01 or 10 or 11		1	1	0	1
Common input mode (Channel C, 1.25 Gsps) Full standby	X	X	01 or 10 or 11		1	1	1	0
Common input mode (Channel D, 1.25 Gsps) Full standby	X	X	01 or 10 or 11		1	1	1	1

8.7.4 STATUS Register (Read Only)

Table 8-10. Status Register Mapping: Address 0x02

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused												ADCXUP<3:0>			

Table 8-11. STATUS Register Description

Bit label	Value	Description	Default Setting
ADCXUP<3:0>	XXX0	ADC A standby	111
	XXX1	ADC A active	
	XX0X	ADC B standby	
	XX1X	ADC B active	
	X0XX	ADC C standby	
	X1XX	ADC C active	
	0XXX	ADC D standby	
	1XXX	ADC D active	

8.7.5 SWRESET Register

Table 8-12. SWRESET Register Mapping: Address 0x04

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused												SWRESET			

Table 8-13. SWRESET Register Description

Bit label	Value	Description	Default Setting
SWRESET	0	No Software Reset	0 No software reset
	1	Unconditional Software Reset, see (Note:)	

Note: Global software reset will reset *all* design registers (configuration registers as well as any flip-flop in the digital part of the design). This bit is automatically reset to 0 after some ns. There is no need to clear it by an external access.

8.7.6 TEST Register

Table 8-14. TEST Register Mapping: Address 0x05

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused													RESERVED		TEST M

Notes: 1. TESTM is taken into account only if bit12 (TEST) of Control register (address 0x01) is at 1.

2. It is mandatory to apply a SYNC, SYNCN signal to the ADC whenever the test mode is activated or deactivated. There is no need to perform a SYNCP, SYNCN when the ADC returns to normal running mode.

Table 8-15.

Bit label	Value	Description	Default Setting
TESTM	0	Increasing simultaneous ramp	0 Increasing ramp
	1	Flashing 1 (1 FF pattern every ten 00 patterns) on each ADC	

8.7.7 SYNC Register

Table 8-16. SYNC Register Description

Bit label	Value	Description	Default Setting
SYNC<3:0>	0000	0 extra clock cycle before starting up	00000 Clock cycle
	0001	1 extra clock cycle before starting up	
	...		
	1111	15 extra clock cycles before starting up	

8.7.8 CHANNEL SELECTOR Register

Table 8-17. CHANNEL SELECTOR Register Mapping: Address 0x0F

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused													Channel Selector <2:0>		

Table 8-18. CHANNEL SELECTOR Register Description

Bit label	Value	Description	Default Setting
Channel Selector <2:0>	000	No channel selected (only common registers are accessible)	000 No channel selected
	001	Channel A selected to access to "per-channel" registers	
	010	Channel B selected to access to "per-channel" registers	
	011	Channel C selected to access to "per-channel" registers	
	100	Channel D selected to access to "per-channel" registers	
	Any others	No channel selected (only common registers are accessible)	

Note: The CHANNEL SELECTOR register should be set before any access to *per-channel* registers in order to determine which channel is targeted.

8.7.9 CAL Control Registers

Applies to CAL Control registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 8-19. CAL Control Register Mapping: Address 0x10

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused								PCALCTRL X <1:0>		GCALCTRL X <1:0>		OCALCTRL X <1:0>		INLCALCTRL X <1:0>	

Table 8-20. CAL Control Register Description

Bit label	Value	Description	Default Setting
INLCALCTRL X <1:0>	00	Idle mode (no external INL tuning requested) for selected channel	00
	01	Forbidden Mode	
	10	External INL adjust for selected channel (transfer contents of Ext INL1 & INL2 registers into current INL1 and INL2 registers)	
	11	Idle mode (no external INL tuning requested) for selected channel	
OCALCTRL X <1:0>	00	Idle mode for selected channel	00
	01	Idle mode for selected channel	
	10	External offset adjust for selected channel (transfer of Ext Offset register content into current Offset register)	
	11	Idle mode for selected channel	
GCALCTRL X <1:0>	00	Idle mode for selected channel	00
	01	Idle mode for selected channel	
	10	External gain adjust for selected channel (transfer of Ext Gain register content into current Gain register)	
	11	Idle mode for selected channel	
PCALCTRL X <1:0>	00	Idle mode for selected channel	00
	01	Idle mode for selected channel	
	10	External phase adjust for selected channel (transfer of Ext Phase register content into current Phase register)	
	11	Idle mode for selected channel	

Notes:
1. Writing to the register will starts the corresponding operation(s). In that case, the Status/Busy bit of the mailbox (see below) is asserted until the operation is over. (At the end of a calibration/tuning process, CAL Control register relevant bit slice is NOT reset to default value.)
2. If different calibrations are ordered, they are performed successively following the priority order defined hereafter:
   - –INL has priority over any other
   - –Gain has priority over Offset, and Phase
   - –Offset has priority over Phase

   The transfer function of the ADC is given by the following formula transfer function result = offset + (input × gain).

8.7.10 CAL Control Registers Mailbox (Read Only)

Applies to CAL Control Registers Mailbox A, B, C and D according to CHANNEL SELECTOR register contents.

Table 8-21.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused															STATUS/BUSY X

Table 8-22. CAL Control Registers Mailbox Description

Bit label	Value	Description	Default Setting
STATUS/BUSY X	0	Selected channel is ready (to receive new calibration orders)	0
	1	Selected channel is busy	

Note: When selected channel is busy, it will not be able to deal any new calibration orders coming from SPI.

8.7.11 GLOBAL STATUS Register (Read Only)

Applies to GLOBAL STATUS registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 8-23. GLOBAL STATUS Register Mapping: Address 0x12

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused															STBY X

8.7.12 GLOBAL STATUS Register Description

Table 8-24. GLOBAL STATUS Register Description

Bit label	Value	Description	Default Setting
STBY X	0	Selected Channel is in standby	0
	1	Selected Channel is active	

8.7.13 TRIMMER Register

Applies to TRIMMER registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 8-25. TRIMMER Register Mapping: Address 0x13

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused												TRIMMER X <3:0>			

Table 8-26. TRIMMER Register Description

Bit label	Value	Description	Default Setting
TRIMMER X <3:0>	0000	+11.71Ω	1000 +0Ω
	0001	+9.95Ω	
	0010	+8.29Ω	
	0011	+6.71Ω	
	0100	+5.23Ω	
	0101	+3.82Ω	
	0110	+2.48Ω	
	1000	+1.21Ω	
	1000	0.00Ω	
	1001	–1.15Ω	
	1010	–2.25Ω	
	1011	–3.30Ω	
	1100	–4.31Ω	
	1101	–5.27Ω	
	1110	–6.18Ω	
	1111	–7.07Ω	

Notes: 1. R = 1 + (121*k / (2 + 0.006*(8*bit3 + 4*bit2 + 2*bit1 + bit0))) – the practical results (simulated) are not exactly the ones given above.

2. Please refer to Section 8.6 for more information.

8.7.14 External Offset Registers

Applies to External Offset Registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 8-27. External Offset Control Register Mapping: Address 0x20

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused								EXTERNAL OFFSET X <7:0> (1)							

Table 8-28. External Offset Control Register Description

Bit label	Value	Description	Default Setting
EXTERNAL OFFSET X <7:0>	0x00	Maximum negative offset applied	0x800 LSB Offset
	0x7F	Minimum negative offset applied	
	0x80	Minimum positive offset applied	
	0xFF	Maximum positive offset applied	

Notes: 1. Offset variation range: ~± 50 mV, 256 steps (1 step ~0.4 mV ~0.2 LSB).

2. Current offset of the selected channel is controlled by the External Offset Control Register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.

8.7.15 Offset Registers (Read Only)

Applies to offset registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 8-29. Offset Control Register Mapping: Address 0x21

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused								EXTERNAL OFFSET X <7:0> (1)(2)							

Table 8-30. External Offset Control Register Description

Bit label	Value	Description	Default Setting
OFFSET X <7:0	0x00	Maximum negative offset applied	0x80 0 LSB Offset
	0x7F	Minimum negative offset applied	
	0x80	Minimum positive offset applied	
	0xFF	Maximum positive offset applied	

Notes:
1. Offset variation range: ~± 50 mV, 256 steps (1 step ~0.4 mV ~0.2 LSB).
2. Current offset of the selected channel is controlled by the External Offset Control Register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.

8.7.16 External Gain Control Registers

Applies to External Gain Control registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 8-31. External Gain Control Register Mapping: Address 0x22

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused								EXTERNAL GAIN X <7:0> (1)(2)							

Table 8-32. External Gain Control Register Description

Bit label	Value	Description	Default Setting
EXTERNAL GAIN X <7:0>	0x00	Gain shrunk to minimum accessible value	0x80 0 dB gain
	0x80	Gain at default value (no correction, actual gain follow process scattering)	
	.....		
	0xFF	Gain increased to maximum accessible value	

Notes:
1. Gain variation range: ~±18%, 255 steps (1 step ~0.14%).
2. Current gain of the selected channel is controlled by the External Gain Control Register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.

8.7.17 Gain Control Registers (Read Only)

Applies to gain control registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 8-33. Gain Control Register Mapping: Address 0x23

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused								GAIN X <7:0> (1)(2)							

Table 8-34. Gain Control Register Description

Bit Label	Value	Description	Default Setting
GAIN X <7:0>	0x00	Gain shrunk to minimum accessible value	0x80 0 dB gain
	0x80	Gain at default value (no correction, actual gain follow process scattering)	
	…..		
	0xFF	Gain increased to max accessible value	

Notes:
1. Gain variation range: ~±18%, 255 steps (1 step ~0.14%).
2. Current gain of the selected channel is controlled by the external gain control register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.

8.7.18 External Phase Registers

Applies to phase registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 8-35. External Phase Register Mapping: Address 0x24

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused								EXTERNAL PHASE X <7:0> (1)(2)							

Table 8-36. External Phase Control Register Description

Bit label	Value	Description	Default Setting
EXTERNAL PHASE X <7:0>	0x00	~ –14 ps correction on selected channel aperture delay	0x80 0ps correction on ADC X aperture Delay
	…..		
	0xFF	~ +14 ps correction on selected channel aperture delay	

Notes:
1. Delay control range for edges of internal sampling clocks: ~±14 ps (1 step ~110 fs).
2. Actual Aperture Delay of the selected channel is controlled by the External Phase Control Register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.

8.7.19 Phase Registers (Read Only)

Applies to Phase Registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 8-37. Phase Register Mapping: Address 0x25

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused								PHASE X <7:0> (1)(2)							

Table 8-38. Phase Control Register Description

Bit label	Value	Description	Default Setting
PHASE X <7:0>	0x00	~ –14 ps correction on selected channel aperture delay	0x80 0ps correction on ADC X aperture delay
	…..		
	0xFF	~ +14 ps correction on selected channel aperture delay	

Notes:
1. Delay control range for edges of internal sampling clocks: ~±14 ps (1 step ~110 fs).
2. Actual Aperture Delay of the selected channel is controlled by the External Phase Control Register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.

8.7.20 External First level INL Registers

Applies to External first level INL registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 8-39. External First level INL Register Mapping: Address 0x30 to 0x31

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXTERNAL INL1 X <15:0> (1)(2)															

Table 8-40. External First level INL Register Description

Bit label	Value	Description	Default Setting
EXTERNAL INL1 X <15:0>	0x0000		0x0000
	0XFFFF		

Table 8-41. External First level INL Register Mapping: Address 0x32

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXTERNAL INL1 X <7:0> (1)								DO NOT USE (0x00)							

Table 8-42. External First level INL Register Description

Bit label	Value	Description	Default Setting
EXTERNAL INL1 X <7:0>	0x00		0x00
	0XFF		

Notes: 1. Actual first level INL of the selected channel is controlled by the transfer of External first level INL Register (addresses 0x30 to 0x32) upon request placed through the SPI in the CAL control register of the selected channel.
2. Refer to the INL Calibration procedure for more information.

8.7.21 External Second Level INL Registers

Applies to External second level INL registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 8-43. External Second level INL Register Mapping: Address 0x33 to 0x34

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXTERNAL INL2 X <15:0> (1)															

Table 8-44. External Second Level INL Register Description

Bit label	Value	Description	Default Setting
EXTERNAL INL2 X <15:0>	0x0000		0x0000
	0XFFFF		

Table 8-45. External Second level INL Register Mapping: Address 0x35

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXTERNAL INL2 X <7:0> (1)								DO NOT USE (0x00)							

Table 8-46. External Second Level INL Register Description

Bit label	Value	Description	Default Setting
EXTERNAL INL2 X <7:0>	0x00		0x00
	0XFF		

Notes: 1. Actual second level INL of the selected channel is controlled by the transfer of External second level INL Register (addresses 0x33 to 0x35) upon request placed through the SPI in the CAL control register of the selected channel.
2. Refer to the INL Calibration procedure for more information.

8.7.22 First Level INL Registers (Read only)

Applies to first level INL registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 8-47. First Level INL Register Mapping: Address 0x36 to 0x38

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INL1 X <15:0>															

Table 8-48. First Level INL Register Description

Bit label	Value	Description	Default Setting
INL1 X <15:0>	0x0000		0x0000
	0XFFFF		

8.7.23 Second Level INL Registers (Read only)

Applies to second level INL registers A, B, C and D according to CHANNEL SELECTOR register contents.

Table 8-49. Second Level INL Register Mapping: Address 0x39 to 0x3B

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INL2 X <15:0>															

Table 8-50. Second Level INL Register Description

Bit label	Value	Description	Default Setting
INL2 X <15:0>	0x0000		0x0000
	0XFFFF		

8.8 INL Calibration Procedure

The calibration of the INL abides by the following rule:

If there is an INL peak (+0.5 LSB) around a specific code, then this peak can be decreased by 0.15 LSB by writing a “1” on the bit given by the table below for the first level of correction (fifth column). If this is not sufficient to decrease the INL peak, then you can write a “1” on the bit given by the table in the first level INL column (fourth column). The effect will be then to decrease the INL by 0.6 LSB (the effect of columns four and five are added).

The procedure is similar when the INL should be increased (columns one and two).

Example:

The intrinsic INL obtained with the ADC has a peak (+0.5 LSB) around code 128. By writing a “1” on bit 9 of register at address 0x34, you will be able to decrease the INL peak. If this is not sufficient, you can write another “1” on bit 9 at address 0x31.

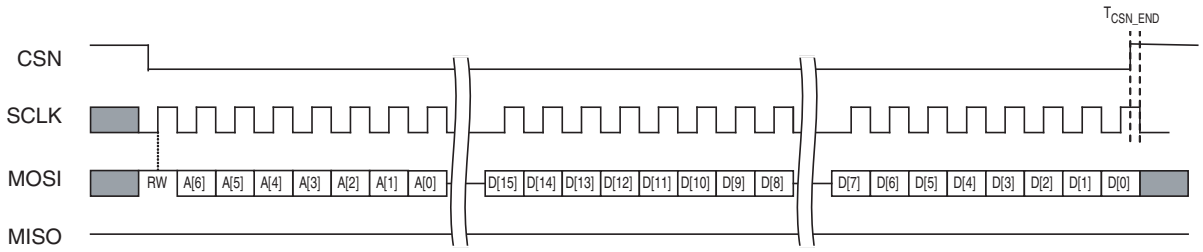
Table 8-51. INL Calibration Table

	First Level INL	Second Level INL	First Level INL	Second Level INL
INL Code	**Increase by 0.45 LSB**	**Increase by 0.15 LSB**	**Decrease by 0.45 LSB**	**Decrease by 0.15 LSB**
0	0x32 bit 8	0x35 bit 8	0x32 bit 9	0x35 bit 9
16	0x32 bit 10	0x35 bit 10	0x32 bit 11	0x35 bit 11
32	0x32 bit 12	0x35 bit 12	0x32 bit 13	0x35 bit 13
48	0x32 bit 14	0x35 bit 14	0x32 bit 15	0x35 bit 15
64	0x31 bit 0	0x34 bit 0	0x31 bit 1	0x34 bit 1
80	0x31 bit 2	0x34 bit 2	0x31 bit 3	0x34 bit 3
96	0x31 bit 4	0x34 bit 4	0x31 bit 5	0x34 bit 5
112	0x31 bit 6	0x34 bit 6	0x31 bit 7	0x34 bit 7
128	0x31 bit 8	0x34 bit 8	0x31 bit 9	0x34 bit 9
144	0x31 bit 10	0x34 bit 10	0x31 bit 11	0x34 bit 11
160	0x31 bit 12	0x34 bit 12	0x31 bit 13	0x34 bit 13
176	0x31 bit 14	0x34 bit 14	0x31 bit 15	0x34 bit 15
192	0x30 bit 0	0x33 bit 0	0x30 bit 1	0x33 bit 1
208	0x30 bit 2	0x33 bit 2	0x30 bit 3	0x33 bit 3
224	0x30 bit 4	0x33 bit 4	0x30 bit 5	0x33 bit 5
240	0x30 bit 6	0x33 bit 6	0x30 bit 7	0x33 bit 7
255	0x30 bit 8	0x33 bit 8	0x30 bit 9	0x33 bit 9

Note: The INL correction value varies with the temperature. The typical value is 0.15 LSB at T_J = 50°C but can vary from 0.1 LSB to 0.2 LSB from low to high temperatures.

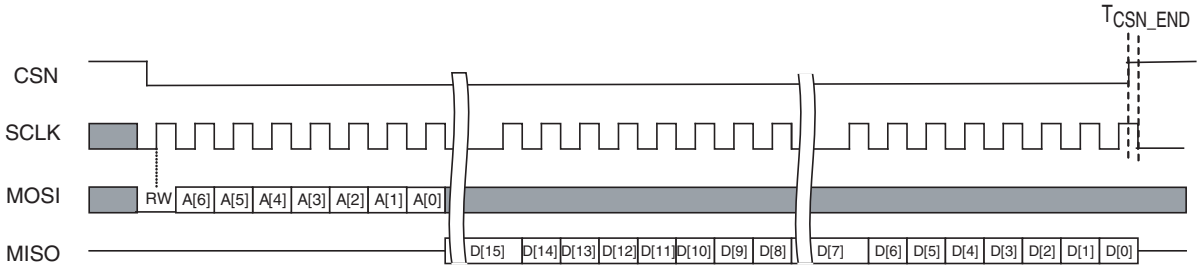
8.8.1 Timings

Figure 8-8. Register Write to a 16-bit Register



Note: Last falling edge of sclk should occur only once csn is back to high level at the end of the write procedure

Figure 8-9. Register Read from a 16-bit Register



Note: $T_{CSN\_END} = T_{SCLK}/4 = 12.5$ ns (see note [3]).

Table 8-52. Timing Characteristics

Pin	Max Frequency	Setup [1]	Hold [1]	Propagation Time TPD
SCLK	20 MHz			
CSN (to SCLK) [2]		1 ns	1 ns	
MOSI (to SCLK)		1.2 ns	1.0 ns	
MISO (to SCLK)				min 1.5 ns/max 4 ns

Notes:
1. First value is in minimum conditions, second value is in maximum conditions.
2. Setup/Hold to both SCLK edges.
3. Last falling edge of sclk should occur once csn is set to 1, due to an internal operation.

9. DEFINITION OF TERMS

Table 9-1. Definition of Terms

(Fs max)	Maximum Sampling Frequency	Sampling Frequency for Which ENOB < 6bits
(Fs min)	Minimum sampling frequency	Sampling frequency for which the ADC Gain has fallen by 0.5 dB with respect to the gain reference value. Performances are not guaranteed below this frequency.
(BER)	Bit Error Rate	Probability to exceed a specified error threshold for a sample at maximum specified sampling rate. An error code is a code that differs by more than ± 4 LSB from the correct code.
(FPBW)	Full power input bandwidth	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full scale –1 dB (–1 dBFS).
(SSBW)	Small signal input bandwidth	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full scale –10 dB (–10 dBFS).
(SINAD)	Signal-to-noise and distortion ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below full scale (–1dBFS), to the RMS sum of all other spectral components, including the harmonics except DC.
(SNR)	Signal-to-noise ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below full scale, to the RMS sum of all other spectral components including the nine first harmonics.
(THD)	Total harmonic distortion	Ratio expressed in dB of the RMS sum of the first nine harmonic components, to the RMS input signal amplitude, set at 1 dB below full scale. It may be reported in dB (that is, related to converter –1 dB full scale), or in dBc (i.e, related to input signal level).
(SFDR)	Spurious free dynamic range	Ratio expressed in dB of the RMS signal amplitude, set at 1dB below full scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dB (that is, related to converter –1 dB full scale), or in dBc (that is, related to input signal level).
(ENOB)	Effective number of bits	$ENOB = \frac{SINAD - 1.76 + 20\log(A/FS/2)}{6.02}$ Where A is the actual input amplitude and FS is the full scale range of the ADC under test.
(DNL)	Differential nonlinearity	The Differential Non Linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
(INL)	Integral nonlinearity	The Integral Non Linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all INL (i).
(TA)	Aperture delay	Delay between the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point), and the time at which (XAI, XAIN, where X = A, B, C, D) is sampled.
(JITTER)	Aperture uncertainty	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
(TS)	Settling time	Time delay to achieve 0.8% accuracy at the converter output when a 80% full scale step function is applied to the differential analog input.
(ORT)	Overvoltage recovery time	Time to recover 0.8% accuracy at the output, after a 150% full scale step applied on the input is reduced to midscale.
(TOD)	Digital data output delay	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
(TDR)	Data ready output delay	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
TD1	Time delay from Data transition to Data ready	The difference TD1-TD2 gives an information if Data Ready is centred on the output data If Data ready is in the middle to data TD1 = TD2 = Tdata/2
TD2	Time delay from Data ready to Data transition	

Table 9-1. Definition of Terms (Continued)

(Fs max)	Maximum Sampling Frequency	Sampling Frequency for Which ENOB < 6bits
(TC)	Encoding clock period	TC1 = Minimum clock pulse width (high) TC = TC1 + TC2 TC2 = Minimum clock pulse width (low)
(TPD)	Pipeline Delay	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD).
(TRDR)	Data ready reset delay	Delay between the first rising edge of the external clock after reset (SYNC, SYNCN) and the reset to digital zero transition of the data ready output signal (XDR, XDRN, where X = A, B, C or D).
(TR)	Rise time	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
(TF)	Fall time	Time delay for the output DATA signals to fall from 20% to 80% of delta between low level and high level.
(PSRR)	Power supply rejection ratio	Ratio of input offset variation to a change in power supply voltage.
(NRZ)	Nonreturn to zero	When the input signal is larger than the upper bound of the ADC input range, the output code is identical to the maximum code and the out-of-range bit is set to logic one. When the input signal is smaller than the lower bound of the ADC input range, the output code is identical to the minimum code, and the out-of-range bit is set to logic one. (It is assumed that the input signal amplitude remains within the absolute maximum ratings).
(IMD)	Intermodulation distortion	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products.
(NPR)	Noise power ratio	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
(VSWR)	Voltage standing wave ratio	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20 dB return loss (ie. 99% power transmitted and 1% reflected).

10. THERMAL AND MOISTURE CHARACTERISTICS

Assumptions:

- No air
- Pure conduction
- No radiation

10.1 Thermal Characteristics

- Rth Junction bottom of balls = 4.47°C/W
- Rth Junction board = 5.28°C/W
- Rth Junction top of case = 2.0°C/W
- Rth Junction top of case with 50 µm thermal grease = 2.7°C/W
- Rth Junction ambient (JEDEC standard, 49 × 49 mm² board size) = 14.1°C/W
- Rth Junction ambient (180 × 170 mm² evaluation board size) = 10.6°C/W

10.2 Thermal Management Recommendations

In still air and 25°C ambient temperature conditions, the maximum temperature for the device soldered on the evaluation board is 67.4°C. In this environment, no cooling is necessary. In the case of the need of an external thermal management, it is recommended to have an external heatsink on top of the EBGA380 with a thermal resistance of 5°C/W max.

10.3 Moisture Characteristics

This device is sensitive to the moisture (MSL3 according to JEDEC standard). Shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH). After this bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temp. 220°C) must be:

– Mounted within 168 hours at factory conditions of ≤ 30°C/60% RH, or

– Stored at ≤ 20% RH

Devices require baking, before mounting, if Humidity Indicator is > 20% when read at 23°C ± 5°C. If baking is required, devices may be baked for:

– 192 hours at 40°C + 5°C/–0°C and <5% RH for low temperature device containers, or

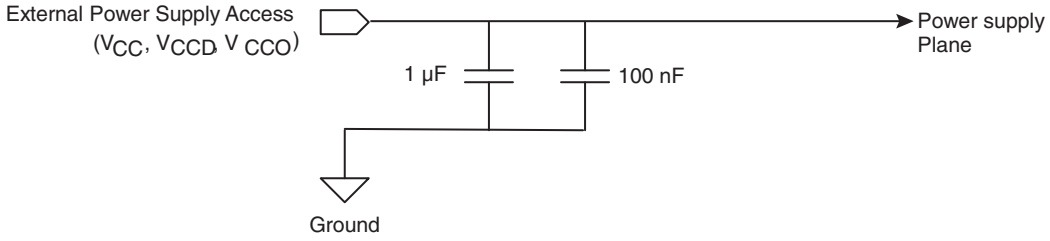
– 24 hours at 125°C ± 5°C for high-temperature device containers

11. QUAD ADC APPLICATION INFORMATION

11.1 Bypassing, Decoupling and Grounding

All power supplies have to be decoupled to ground as close as possible to the signal accesses to the board by 1 µF in parallel to 100 nF.

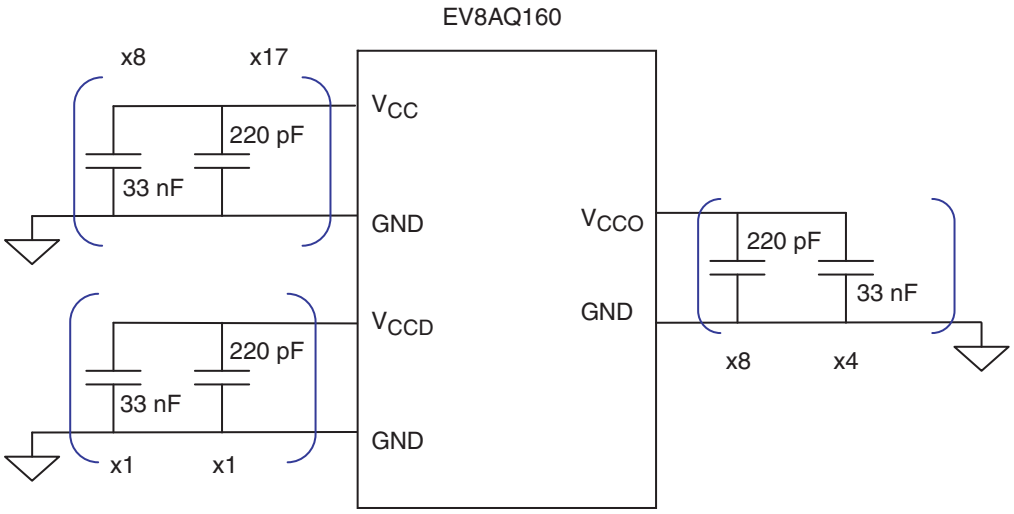
Figure 11-1. EV8AQ160 Power supplies Decoupling and grounding Scheme



Note: V_{CCD} and V_{CCO} planes should be separated but the two power supplies can be reunited by a strap on the board.

It is recommended to decouple all power supplies to ground as close as possible to the device balls with 220 pF in parallel to 33 nF capacitors. The minimum number of decoupling pairs of capacitors can be calculated as the minimum number of groups of neighboring pins. 17 capacitors of 220 pF and 8 capacitors of 33 nF for V_{CC}; 8 capacitors of 220 pF and 4 capacitors of 3 3 nF for V_{CCO} and 1 220 pF capacitor with 1 ""nF capacitor for V_{CCD}.

Figure 11-2.

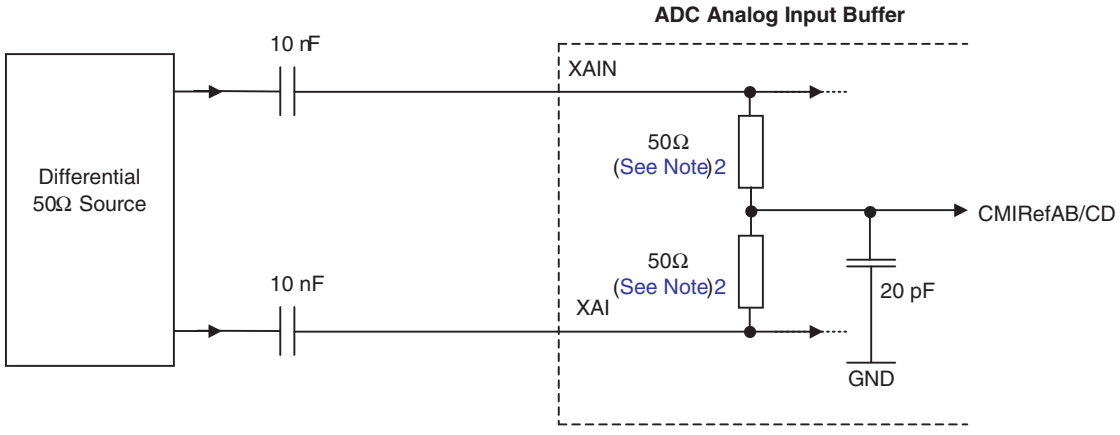


11.2 Analog Inputs (V_{IN}/V_{INN})

11.2.1 Differential Analog Input

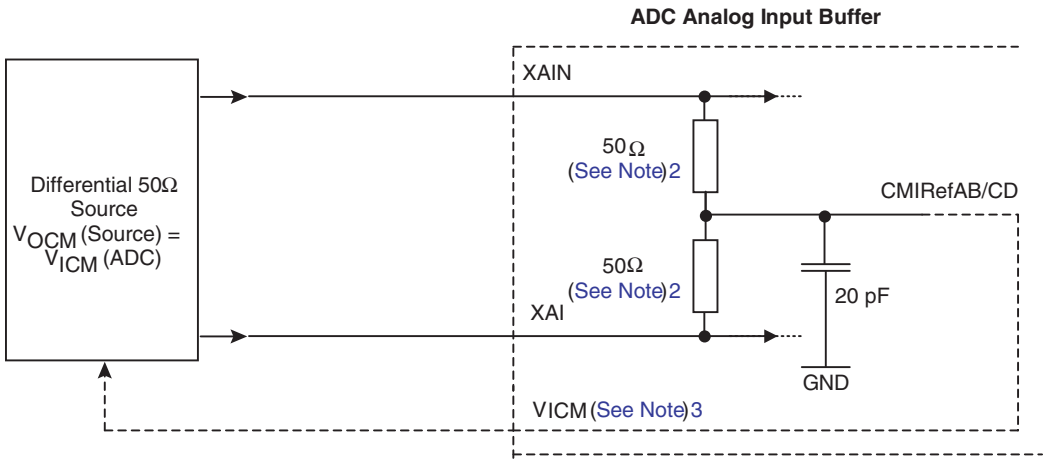
Differential mode is the recommended input scheme. A balun can be used to convert a single-ended source to a differential signal for use with this ADC. The analog input can be either DC or AC coupled as described in Figure 11-3 and Figure 11-4.

Figure 11-3. Differential Analog Input Implementation (AC Coupled)



Notes:
1. X = A, B, C or D.
2. 2. The 50Ω terminations are implemented on-chip and can be fine tuned (TRIMMER register at address 0x13).
3. CMIRefAB/CD = 1.8V. This Common mode is output on signal CMIRefAB for A and B channels and CMIRefCD for C and D channels.

Figure 11-4. Differential Analog Input Implementation (DC Coupled)

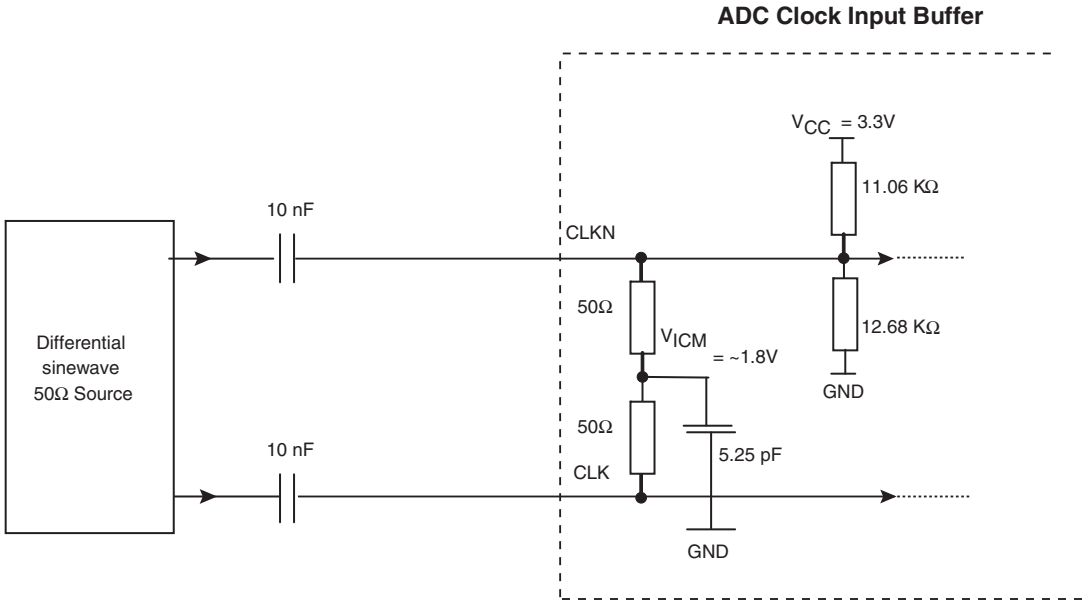


Notes:
1. X = A, B, C or D.
2. The 50Ω terminations are implemented on-chip and can be fine tuned (TRIMMER register at address 0x13).
3. CMIRefAB/CD = 1.8V. This Common mode is output on signal CMIRefAB for A and B channels and CMIRefCD for C and D channels.

11.3 Clock Inputs (CLK/CLKN)

Differential mode is the recommended input scheme.Single-ended clock input is not recommended due to performance limitations. Since the clock input common mode is 1.8V, we recommend to AC couple the input clock as described in Figure 11-5.

Figure 11-5. Differential Clock Input Implementation (AC Coupled)

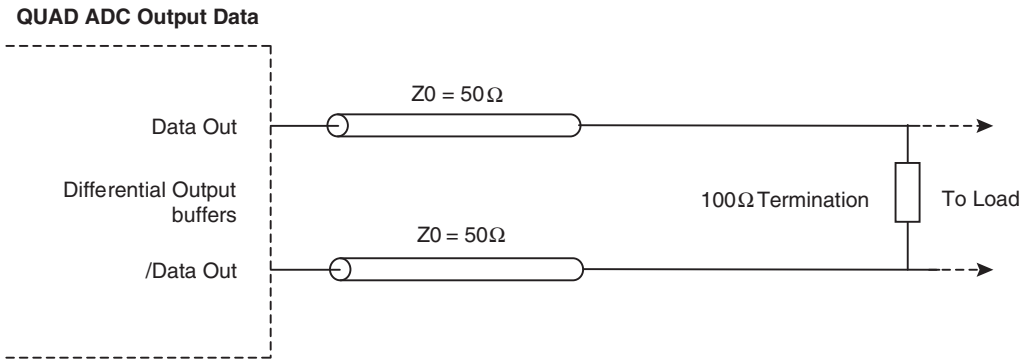


0846J–BDC–03/16

11.4 Digital Outputs

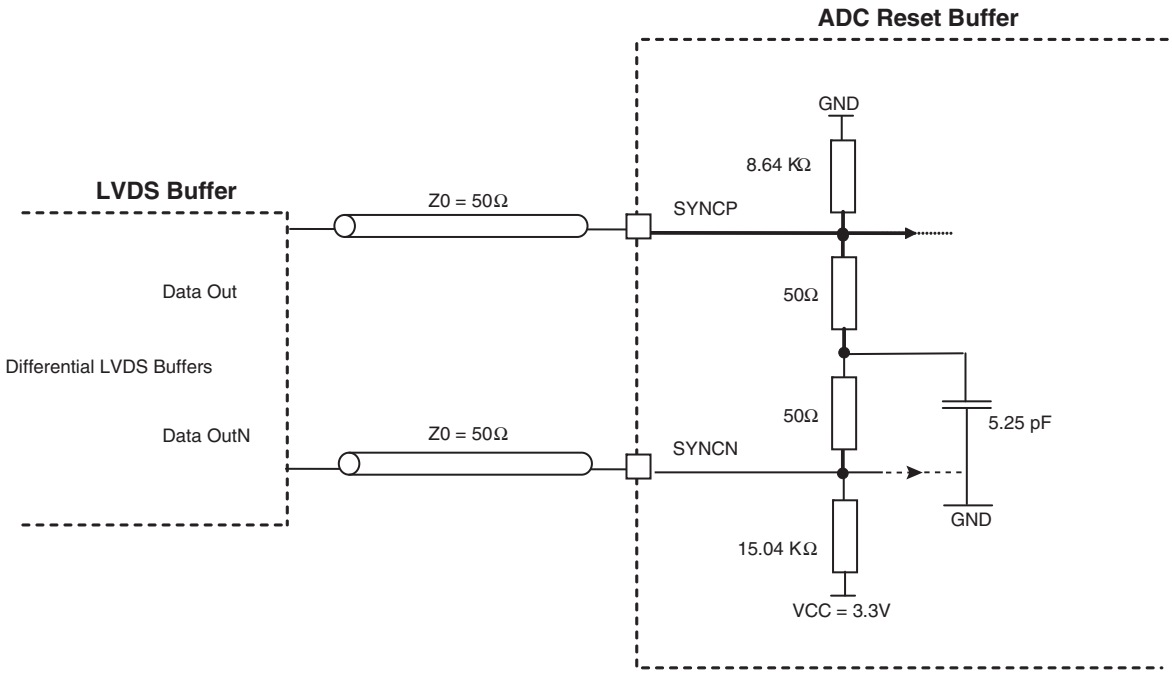
The digital outputs are LVDS compatible. They have to be 100Ω differentially terminated.

Figure 11-6. Differential Digital Outputs Terminations (100Ω LVDS)



11.5 Reset Buffer (SYNCP, SYNCN)

Figure 11-7. Reset Buffer (SYNCP, SYNCN)



Note: We recommend to drive the SYNC, SYNCN signal using an LVDS buffer.

12. EBGA380 QUAD ADC PACKAGE OUTLINE

Figure 12-1. EBGA380 Quad ADC Package Outline

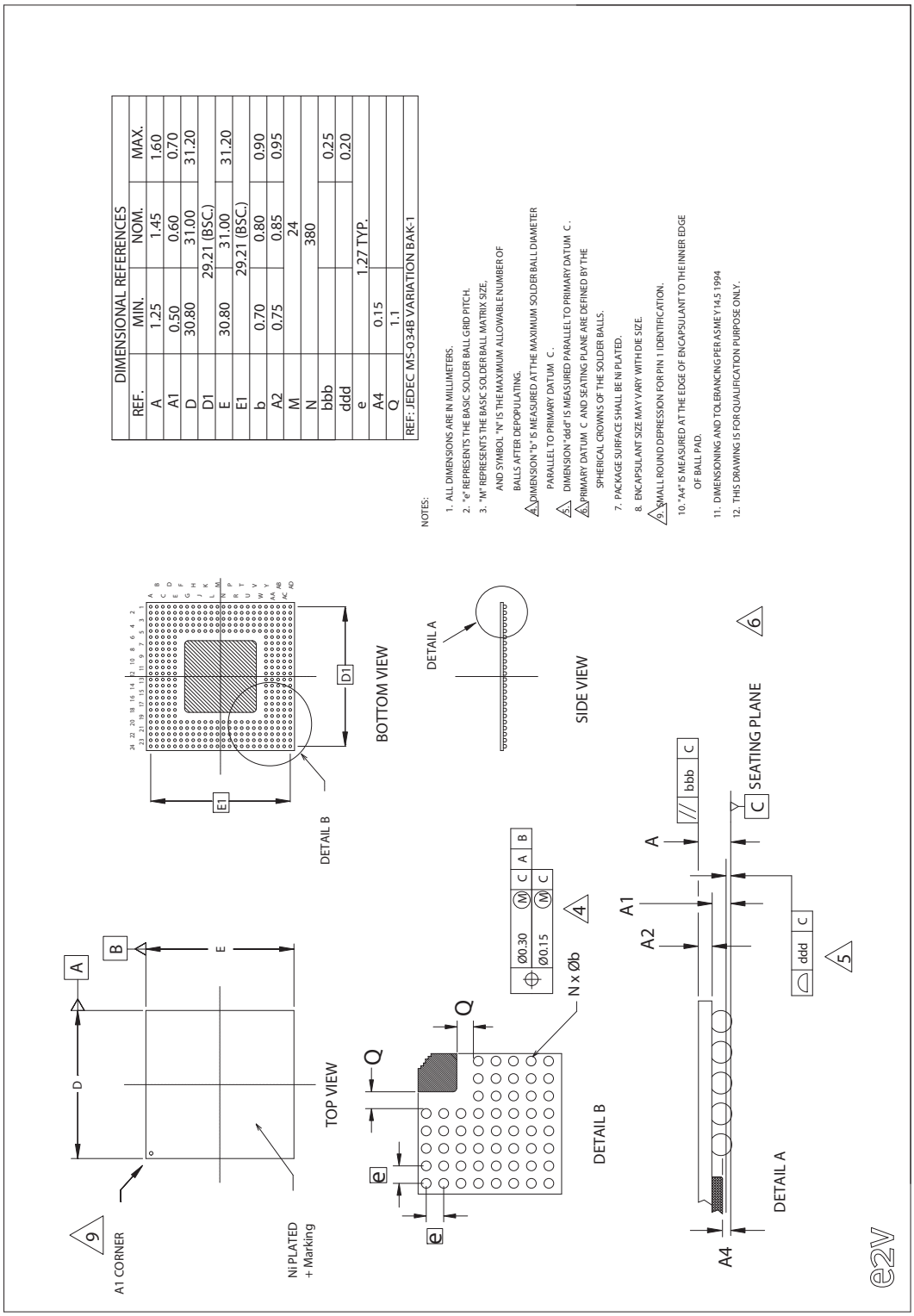
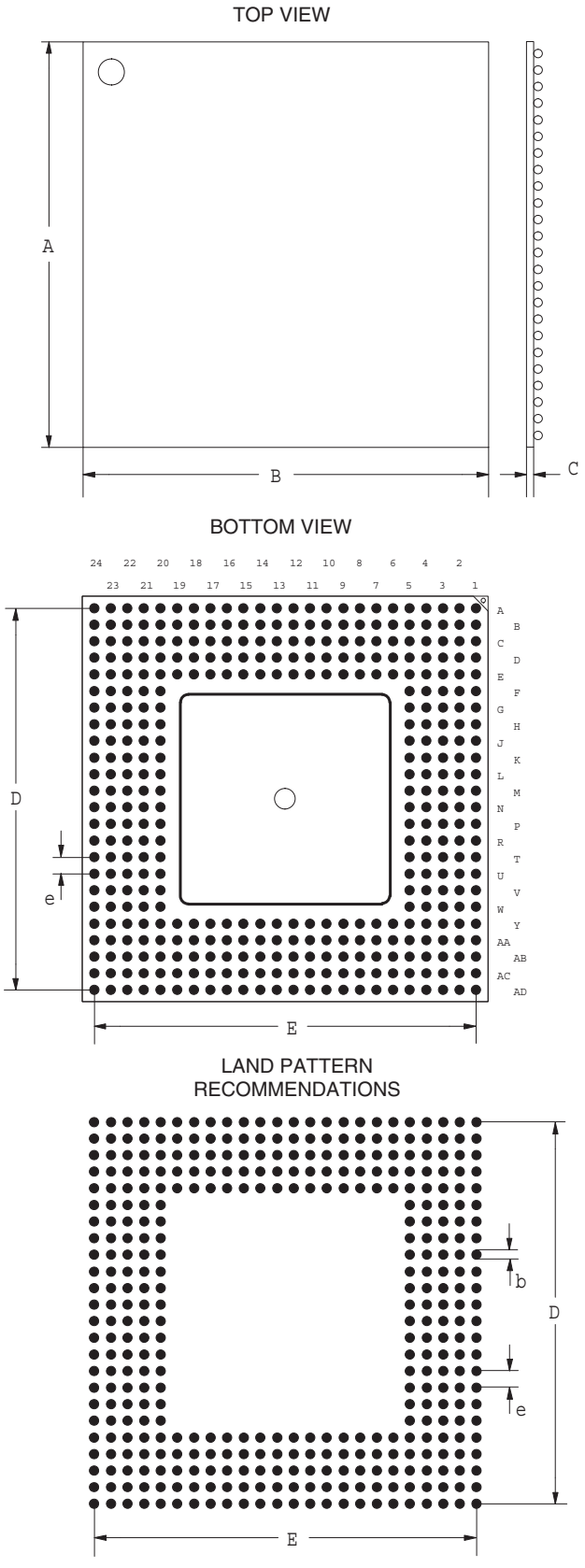


Figure 12-2. EBGA380 Land Pattern Recommendation



A	B	C	D	E	e	b
31.00	31.00	0.85	29.21	29.21	1.27	0.70

All dimensions are in millimeters

13. ORDERING INFORMATION

Table 13-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EVX8AQ160TPY	EBGA380 RoHS	Ambient	Prototype	
EV8AQ160CTPY	EBGA380 RoHS	Commercial *C* grade $0°C < T_{amb} < 70°C$	Standard	
EV8AQ160TPY-EB	EBGA380 RoHS	Ambient	Prototype	Evaluation board

0846J–BDC–03/16

Table of Contents