Preliminary

MB81256

MOS Memories **FUJITSU**

■ MB81257-10, MB81257-12, MB81257-15

NMOS 262,144-Bit Dynamic Random Access Memory With Nibble Mode

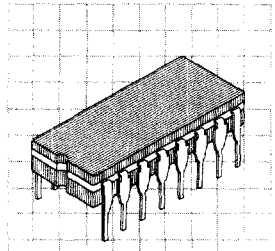
Description

The Fujitsu MB81257 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

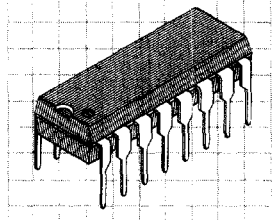
The MB81257 features "nibble mode" which allows high speed serial access of up to four bits of data. Additionally, the MB81257 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability that is an upward compatible version of the MB8266A. Multiplexed row and column address inputs permit the MB81257 to be housed in a Jedec standard 16-pin dual in-line package and 18-pad LCC.

The MB81257 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including dynamic sense amplifiers.

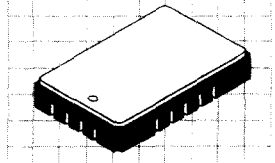
Clock timing requirements are noncritical, and the power supply tolerance is very wide. All inputs are TTL compatible.



Cerdip Package
DIP-16C-C04



Plastic Package
DIP-16P-M03

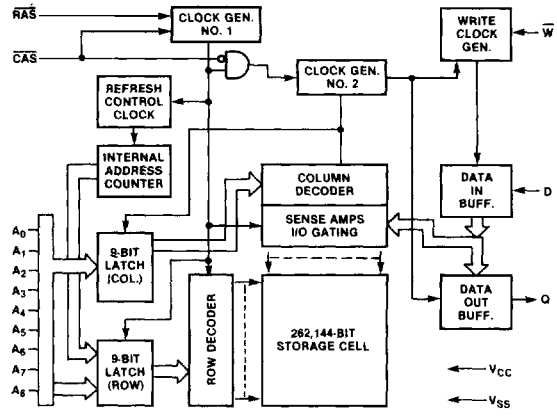


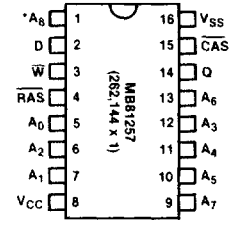
Ceramic LCC
LCC-18C-F04

Features

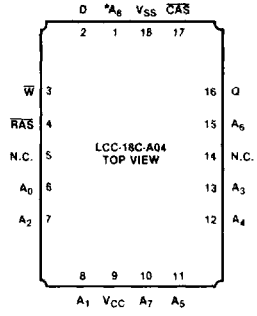
- 262,144 x 1-bit organization
- Row Access Time/Cycle Time:
  MB81257-10 100 ns Max/ 210 ns Min.
  MB81257-12 120 ns Max/ 230 ns Min.
  MB81257-15 150 ns Max/ 260 ns Min.
- Low Power Dissipation:
  314 mW max. (t_{RC} = 260 ns)
  25 mW (Standby)
- +5V supply voltage, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- Common I/O capability using "Early Write" operation
- On-chip substrate bias generator
- Nibble mode capability for faster access
- Fast Read-Write Cycle, TRWC = TRC
- t_{AR} t_{WCR}, t_{DHR}, t_{RWD} eliminated
- $\overline{CAS}$-before-$\overline{RAS}$ on chip refresh
- Hidden $\overline{CAS}$ before-$\overline{RAS}$ on-chip refresh
- $\overline{RAS}$-only refresh
- Refresh 4 ms/256 cycles
- Output unlatched at cycle end allows two dimensional chip select
- On-chip Address and Data-In latches
- Industry standard 16-pin package

MB81257 Block Diagram and Pin Assignments





*: A_8 (Pin 1) is Assigned for Nibble (4-bit) Address.



NOTE: The following IEEE Std. 662-1980 symbols are used in this data sheet: D = Data In, $\overline{W}$ = Write Enable, Q = Data Out.

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−1.0 to 7.0	V
Operating Temperature (ambient)	T_{OP}	0 to 70	°C
Storage Temperature Cerdip / Plastic	T_{STG}	−55 to +150 / −55 to +125	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OS}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be *restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions* for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Value Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C ambient
	V_{SS}	0	0	0	V	
Input High Voltage All Inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage All Inputs	V_{IL}	−1.0	—	0.8	V	

R3

Capacitance
(T_A = 25 °C)

Parameter	Symbol	Value Min	Typ	Max	Unit
Input Capacitance A_0 to A_8, D	C_{IN1}	—	—	7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$	C_{IN2}	—	—	10	pF
Output Capacitance Q	C_{OUT}	—	—	7	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

R9

Parameter	Symbol	MB81257-10 Min	Max	MB81257-12 Min	Max	MB81257-15 Min	Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	I_{CC1}	—	70	—	65	—	57	mA
STANDBY CURRENT Power Supply Current ($\overline{RAS}$/$\overline{CAS}$ = V_{IH})	I_{CC2}	—	4.5	—	4.5	—	4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min.)	I_{CC3}	—	60	—	55	—	50	mA
NIBBLE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = Min.)	I_{CC4}	—	22	—	20	—	18	mA
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = Min.)	I_{CC5}	—	65	—	60	—	55	mA
INPUT LEAKAGE CURRENT Any Input, (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)	I_{OL}	−10	10	−10	10	−10	10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	—	0.4	—	0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4	—	2.4	—	2.4	—	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	Symbol *Standard	MB81257-10 Min	MB81257-10 Max	MB81257-12 Min	MB81257-12 Max	MB81257-15 Min	MB81257-15 Max	Unit
Time between Refresh		t_{REF}	TRVRV	—	4	—	4	—	4	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	210	—	230	—	260	—	ns
Read-Write Cycle Time		t_{RWC}	TRELREL	210	—	230	—	260	—	ns
Access Time from $\overline{RAS}$	(4), (6)	t_{RAC}	TRELQV	—	100	—	120	—	150	ns
Access Time from $\overline{CAS}$	(5), (6)	t_{CAC}	TCELQV	—	50	—	60	—	75	ns
Output Buffer Turn off Delay		t_{OFF}	TCEHQZ	0	25	0	25	0	30	ns
Transition Time		t_T	TT	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	TREHREL	90	—	100	—	100	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	TRELREH	110	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	TCELREH	60	—	60	—	75	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	TCELCEH	60	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	TRELCEH	110	—	120	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	(4), (7)	t_{RCD}	TRELCEL	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	TCEHREL	15	—	20	—	20	—	ns
Row Address Set Up Time		t_{ASR}	TAVREL	0	—	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	TRELAX	10	—	12	—	15	—	ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0	—	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	TCELAX	15	—	20	—	25	—	ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{CAS}$	(10)	t_{RCH}	TCEHWX	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	(10)	t_{RRH}	TREHWX	20	—	20	—	20	—	ns
Write Command Set Up Time	(8)	t_{WCS}	TWLCEL	0	—	0	—	0	—	ns
Write Command Pulse Width		t_{WP}	TWLWH	15	—	20	—	25	—	ns
Write Command Hold Time		t_{WCH}	TCELWH	15	—	20	—	25	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	TWLREH	40	—	50	—	60	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	TWLCEH	20	—	30	—	40	—	ns
Data In Set Up Time		t_{DS}	TDVCEL	0	—	0	—	0	—	ns
Data In Hold Time		t_{DH}	TCELDX	15	—	20	—	25	—	ns
$\overline{CAS}$ to $\overline{W}$ Delay	(8)	t_{CWD}	TCELWL	15	—	20	—	25	—	ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$		t_{FCS}	TCELREL	20	—	25	—	30	—	ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$		t_{FCH}	TRELCEX	20	—	25	—	30	—	ns
Nibble Mode Read-Write Cycle Time		t_{NRWC}	TCEHCEH	50	—	65	—	80	—	ns
Nibble Mode Read/Write Cycle Time		t_{NC}	TCEHCEH	50	—	65	—	80	—	ns
Nibble Mode Access Time		t_{NCAC}	TCELQV	—	20	—	30	—	40	ns
Nibble Mode $\overline{CAS}$ Pulse Width		t_{NCAS}	TCELCEH	20	—	30	—	40	—	ns
Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	TCEHCEL	20	—	25	—	30	—	ns
Nibble Mode Read $\overline{RAS}$ Hold Time		t_{NRRSH}	TCELREH	20	—	30	—	40	—	ns
Nibble Mode $\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$		t_{RNH}	TREHCEL	20	—	20	—	20	—	ns
Nibble Mode Write $\overline{RAS}$ Hold Time		t_{NWRSH}	TCELREH	40	—	50	—	60	—	ns
Refresh Counter Test Cycle Time	(9)	t_{RTC}	TRELREL	330	—	375	—	430	—	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	(9)	t_{CPT}	TCEHCEL	50	—	60	—	70	—	ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	(9)	t_{TRAS}	TRELREH	230	10000	265	10000	320	10000	ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	TREHCEL	20	—	20	—	20	—	ns
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle		t_{CPR}	TCEHCEL	20	—	25	—	30	—	ns

See Notes on following page.

*These symbols are described in IEEE STD. 662-1980: IEEE Standard terminology for semiconductor memory.

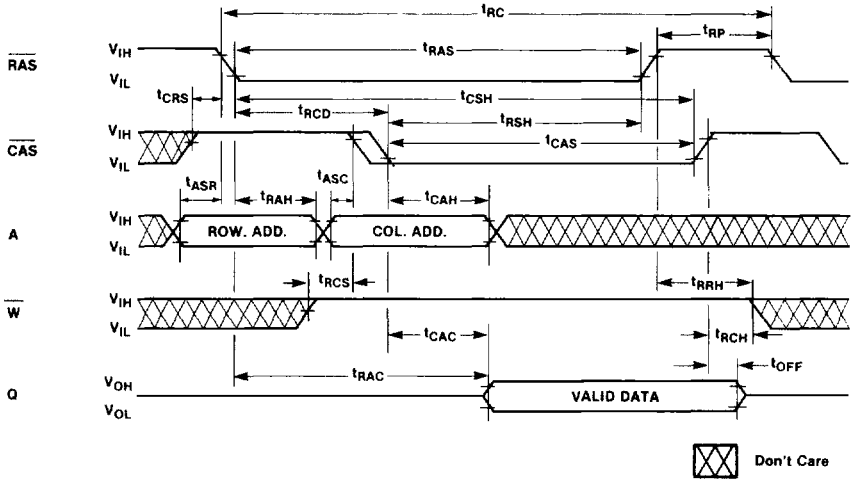
AC Characteristics

Notes:

1. An initial pause of 200μs is required after power up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved.
   If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh initialization cycles are required.
2. AC characteristics assume t_T = 5ns.
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (Max.) the specified maximum value of t_{RAC} (Max.) can be met. If $t_{RCD} > t_{RCD}$ (Max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (Max.).
5. Assumes that $t_{RCD} > t_{RCD}$ (Max.).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{RCD} (Min.) = t_{RAH} (Min.) + $2t_T$ + t_{ASC} (Min.).
8. t_{WCS} and t_{CWD} are non restrictive operating parameters, and are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (Min.), the cycle is an early write cycle, and the data out pin will remain open circuit (High Impedance) throughout the entire cycle.
   If $t_{CWD} > t_{CWD}$ (Min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
9. Test mode cycle only.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

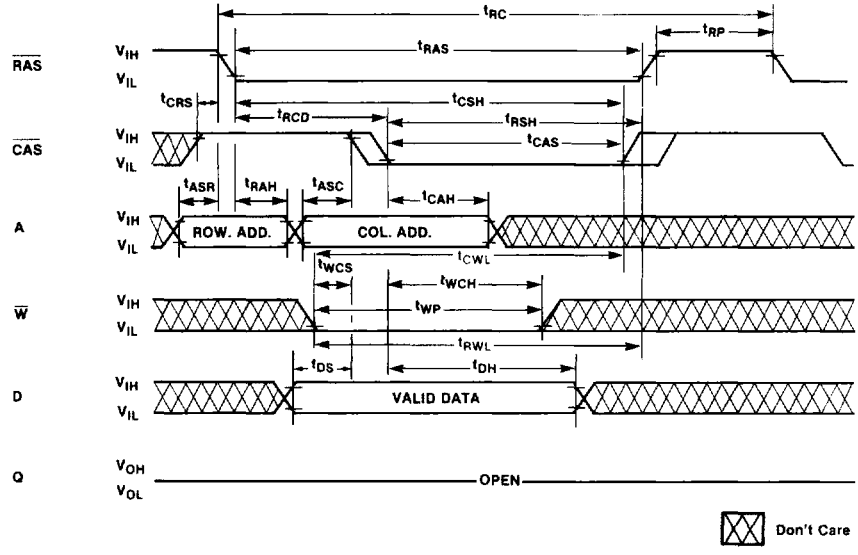
Timing Diagrams

Read Cycle

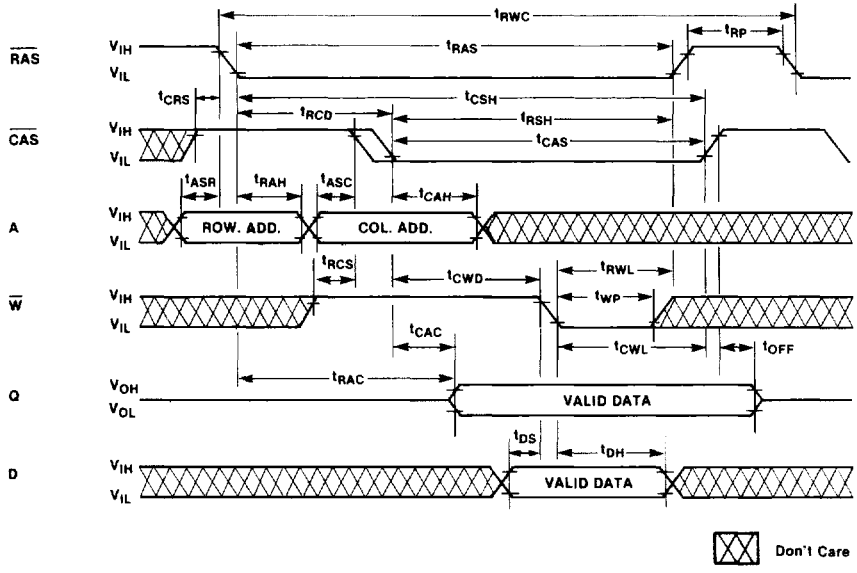


Timing Diagrams, continued

Write Cycle (Early Write)



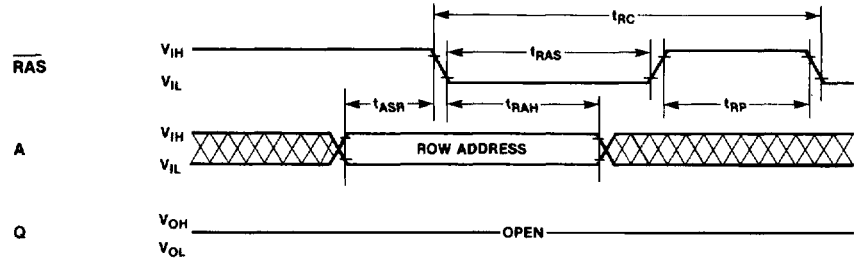
Read-Write/Read-Modify-Write Cycle



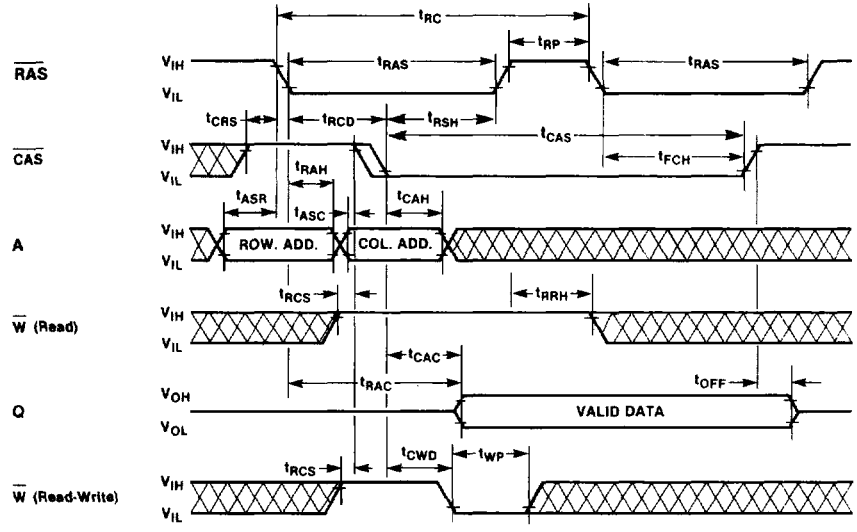
Timing Diagrams, continued

"$\overline{RAS}$-Only" Refresh Cycle

NOTE: $\overline{CAS}$ = V_{IH}, W, D = Don't Care

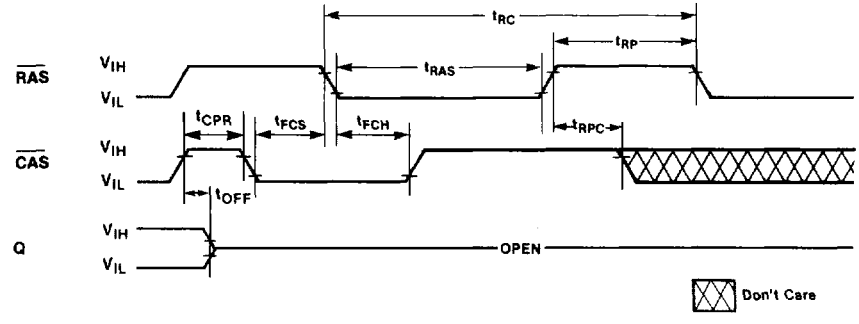


Hidden Refresh Cycle



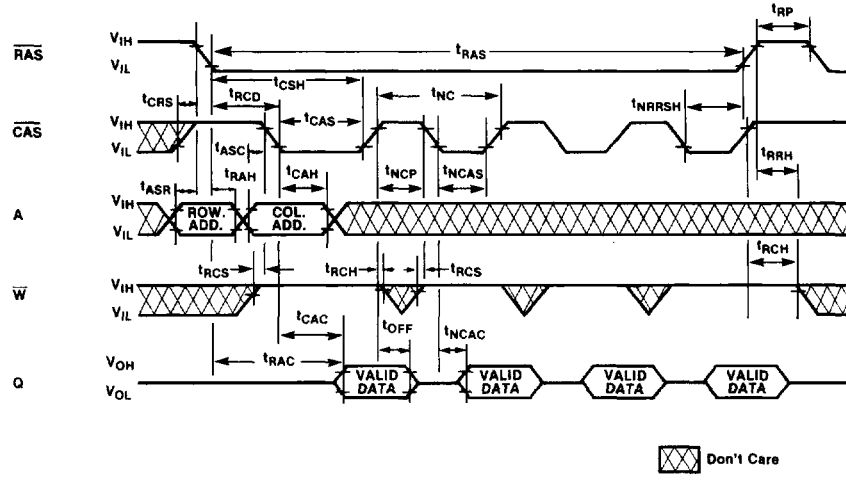
"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Cycle

NOTE: Address, $\overline{W}$, D = Don't Care

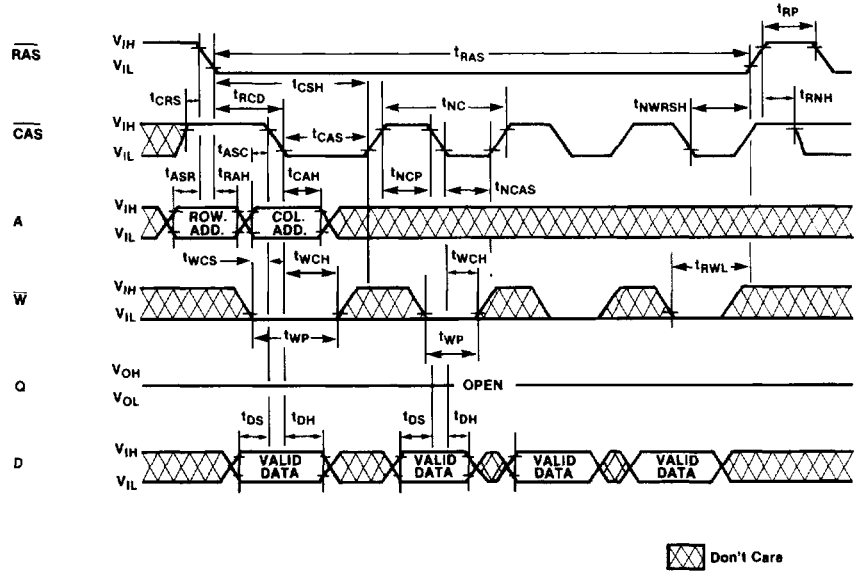


Timing Diagrams, continued

Nibble Mode Read Cycle

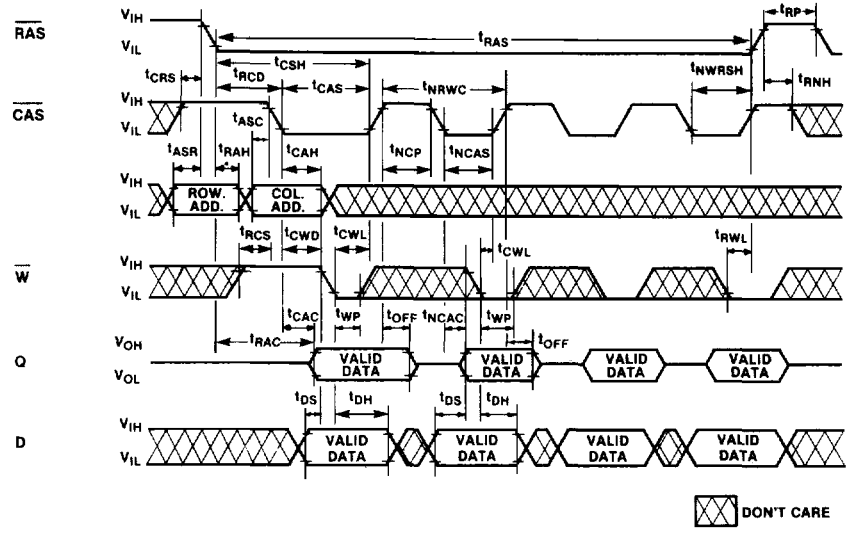


Nibble Mode Write Cycle

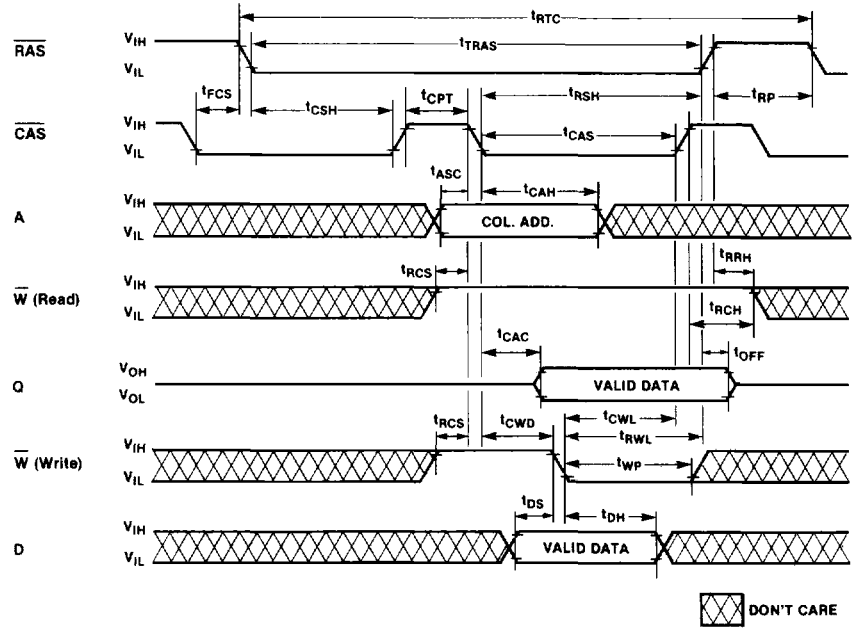


Timing Diagrams, continued

Nibble Mode Read-Write Cycle



"CAS-Before-RAS" Refresh Counter Test Cycle



Description

Simplified Timing Requirement
The MB81257 has improved circuitry that eases timing requirements for high speed access operations. The MB81257 can operate under the condition of t_{RCD} (max) = t_{CAC}, thus providing optimal timing for address multiplexing. In addition, the MB81257 has minimal hold times for Addresses (t_{CAH}), Write-Enable (t_{WCH}) and Data-in (t_{DH}). The MB81257 provides higher throughput in interleaved memory system applications. Fujitsu has made the timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Fast Read-Write Cycle
The MB81257 has a fast read-modify-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes "low". When $\overline{W}$ is "low" during a $\overline{CAS}$ transition to "low", the MB81257 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. When $\overline{W}$ goes "low", after t_{CWD} following a $\overline{CAS}$ transition to "low", the MB81257 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D is written into the cell selected. Therefore, a very fast read-write cycle ($t_{RWC} = t_{RC}$) is possible with the MB81257.

Address Inputs
A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB81257. Nine row address bits are established on the input pins (A_0 through A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable
The read or write mode is selected with the $\overline{W}$ input. A logic "high" on $\overline{W}$ dictates read mode. A logic "low" dictates write mode. The data input is disabled when the read mode is selected.

Data Input
Data is written into the MB81257 during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the Data-in (D) register. In a write cycle, if $\overline{W}$ is brought "low" (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when $t_{RCD(max)}$ is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after $t_{RCD(max)}$. Data remains valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Nibble Mode
Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA_8, RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by the normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See table I below).

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the three-state control of the D_{OUT} pin is determined by the first normal access cycle.

The data output is controlled

Table 1
Nibble Mode Address Sequence Example

Sequence	Nibble Bit	RA_8	Row Address	CA_8	Column Address	Comments
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	generated internally
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	sequence repeats

Description, continued

only by the $\overline{W}$ state referenced at the $\overline{CAS}$ negative transition of the normal cycle (first nibble bit). That is, when $t_{WCS} > t_{WCS}$(min.) is met, the data output will remain open circuit throughout the succeeding nibble cycle regardless of the $\overline{W}$ state. When $t_{CWD} > t_{CWD}$(min.) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of the $\overline{W}$ state. The write operation is done during the period in which the $\overline{W}$ and $\overline{CAS}$ clocks are low. Therefore, the write operation can be performed bit by bit during each nibble operation regardless of the timing conditions of $\overline{W}$ (t_{WCS} and t_{CWD}) during the normal cycle (first nibble bit). (See table II and Figure 2 below).

$\overline{RAS}$-Only Refresh
Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-adresses ($A_0 \sim A_7$) at least every 4 ms. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought "low". Strobing each of the 256 row-addresses ($A_0 \sim A_7$) with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB81257 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh
A hidden refresh cycle may take place while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time. For the MB81257, a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh addresses as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle
A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to "high" and then goes to "low" again while $\overline{RAS}$ is held "low", the read and write operation are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

A ROW ADDRESS
Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.

A COLUMN ADDRESS
All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure
The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all the following operations:

(1). Initialize the internal refresh counter. For this operation, 8 cycles are required.

(2). Write a test pattern of "low"s into memory cells at a single column address and 256 row address.

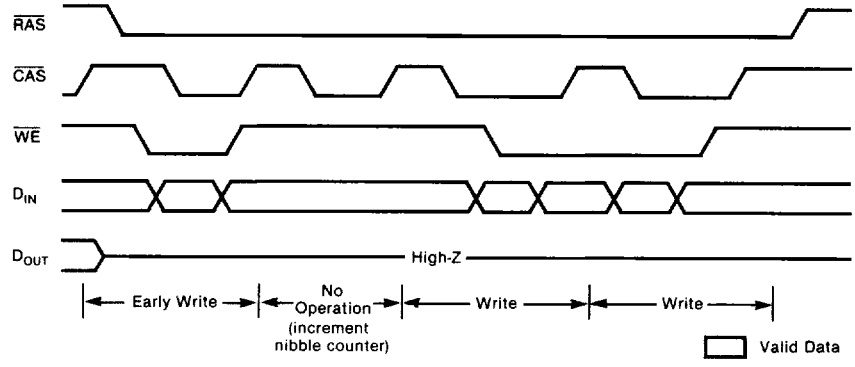
(3). Using a read-modify-write cycle, read the "low" written at the last operation (Step (2)) and write a new "high" in the same cycle. This cycle is repeated 256 times, and "high"s are written into the 256 memory cells.

(4). Read the "high"s written at the last operation (Step 3).

(5). Complement the test pattern and repeat steps (2), (3) and (4).

Figure 2
Nibble Mode

1) In this case the first nibble cycle is an Early Write cycle.



2) In this case the first nibble cycle is a delayed write (Read-Write) cycle.

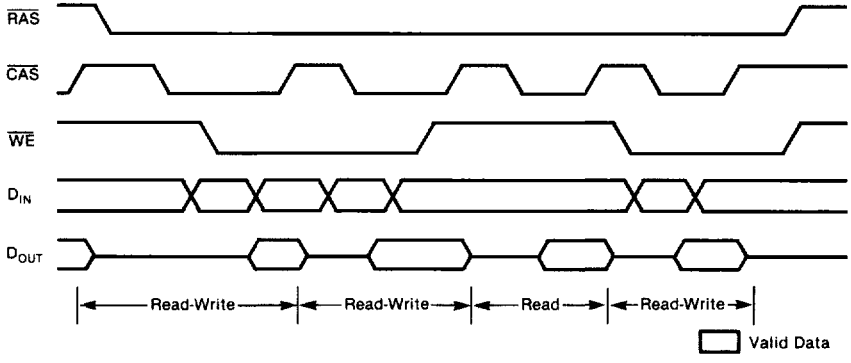


Table 2
Functional Truth Table

$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby.
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read.
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geq t_{WCS}$ (min).
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write $t_{CWD} \geq t_{CWD}$ (min).
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	$\overline{RAS}$ Only Refresh.
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	$\overline{CAS}$-before-$\overline{RAS}$ Refresh. Valid data selected at previous Read or Read-Write cycle is held.
H	L	Don't Care	Don't Care	High-Z	No	No	No	$\overline{CAS}$ disturb.