DPS Power Supply

A Server System Infrastructure Specification
For Distributed Power Systems

Version 2.0

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1 Purpose

This document specifies a 48 VDC, single rail power supply for use in distributed schemes for server systems. The intent of the document is to define a power supply specification that enables the development of reliable, upgradable and extensible server components. Its intention is not to provide interoperability among different vendors of power supplies. Protection of producer and consumer investment is an important factor in the decision to implement this specification. Power supplies must meet all of the required features to be compliant to this specification.

2 Conceptual Overview

Servers using the power supply defined in this specification can be implemented either as modular or integrated systems. Modular systems are designed as multiple rack-mounted modules, with each module performing a specific function. Integrated systems are designed as one, integrated, rack-mountable server unit. Each of these system designs contains the following sub-systems:

- Electronics Bay (processor and memory)
- I/O Bay(s) (PCI I/O)
- Power Bay
- Peripheral bays

The processor/memory complex of the target server is generally designed to expand to a minimum of four processors; however, some server processor complexes may be expanded to up to eight or more processors. The memory expansion capacity and memory technology is sized to processor speed and a quantity of processors.

I/O functions are typically implemented with PCI add-in cards. In the integrated system design, the PCI cards are in the same module as the processor and memory. In the modular system, the PCI cards may be in a separate bay.

Integrated systems and modular systems both require additional peripheral expansion bays for sufficient mass storage capacity.

2.1 Distributed Power Architectural Overview

The goals of a distributed power system are to simplify the architecture of the power supply, and to move voltage conversion to the components, external to the power supply. A pictorial overview of the distributed power scheme is shown in Figure 1.

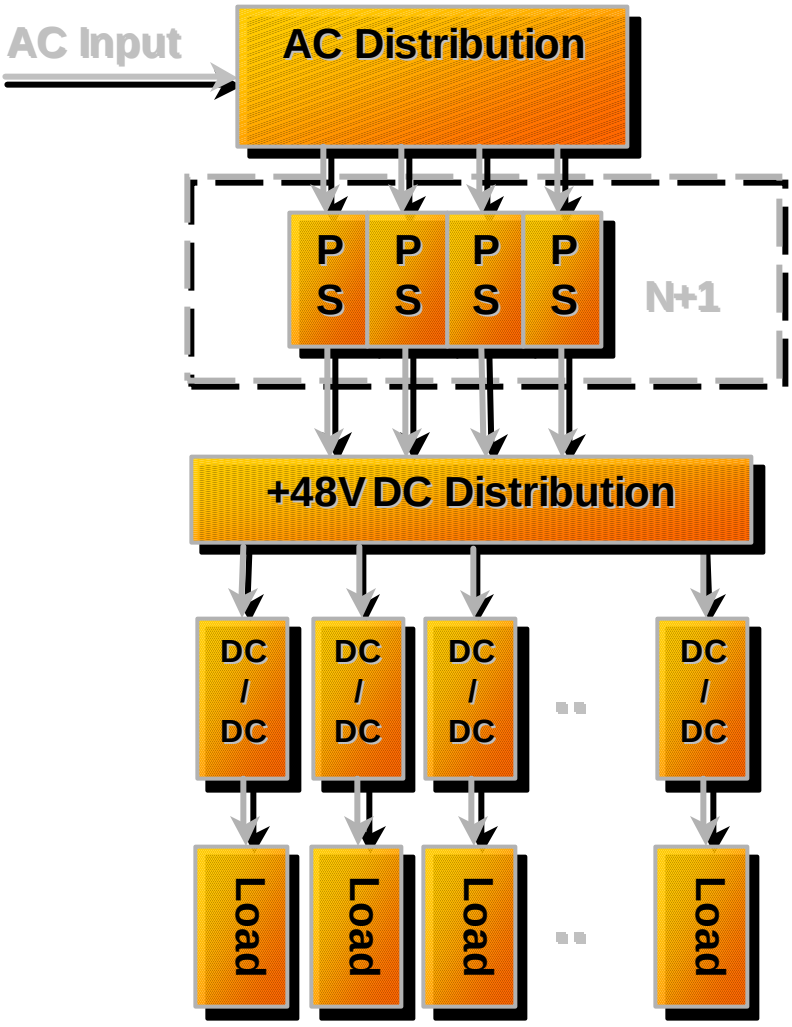

Figure 1: Distributed Power Scheme Overview

3 Definitions/Terms/Acronyms

CFM	Cubic Feet per Minute (airflow).
Electronics Bay	The volume and mechanical chassis to support the standard Electronics-Bay unit containing the processor, memory, and minimal I/O.
EMI	Electromagnetic Interference
FRU	Field Replaceable Unit.
IPMI	Intelligent Platform Management Interface. Refer to http:\\developer.intel.com\design\servers\ipmi\spec.htm for detials.
I/O Bay	The volume and mechanical chassis to support the standard 'I/O-Bay' unit containing I/O expansion devices, such as HDDs, peripherals, or adapter cards
Monotonically	A waveform changes from one level to another in a steady fashion without negative slope or oscillation.
Noise	The periodic or random signals over frequency band of 0 Hz to 20 MHz.
PFC	Power Factor Corrected.
Power Bay	The mechanical chassis supporting the power conversion from AC power to +48 VDC.
Power Supply	The volume, connector, and mechanical interface required in a chassis to support the standard power supply unit.
PSU	Power Supply Unit.
Ripple	The periodic or random signals over frequency band of 0 Hz to 20 MHz.
Rise Time	Rise time is defined as the time it takes any output voltage to rise from 10% to within regulation limits.
Sag	The condition where the AC line voltage drops below the nominal voltage conditions.
SMBus	System Management Bus. This is a serial communication bus for low speed communication. Refer to www.smbus.org for details.
Surge	The condition where the AC line voltage rises above nominal voltage.
VSB or Standby Voltage	An output voltage that is present whenever AC power is applied to the AC inputs of the supply.

4 General

This specification describes the requirements for power supply that provides a minimum of 1200 W at 200-240 VAC. The AC input and DC output connectors are located on the side of the supply opposite the side where the handle is located. These connectors make contact with the system or power bay when the power supply is inserted. The power supply is designed to have parallel DC outputs, with active load sharing. Each power supply contains its own cooling fan(s). The power supply has a dual rating of 1200 W minimum over an input range of 180-264 VAC and 700 W minimum over an input range of 90-132 VAC.

5 Mechanical Overview

STATUS
Required

The physical form factors of the power supply are depicted in the following figures. The insertion and extraction force without the assistance of the handle must be less than 20 lb.

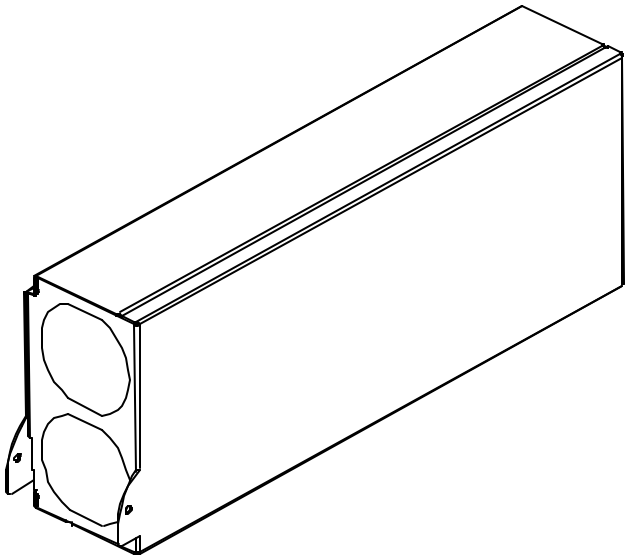

Figure 2: Form Factor

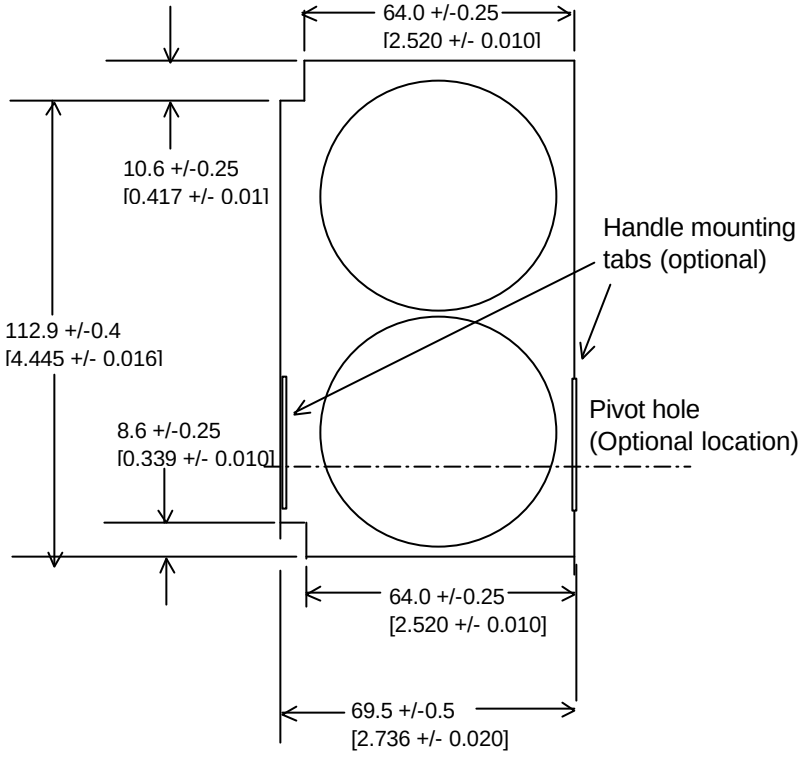

Figure 3: External Face

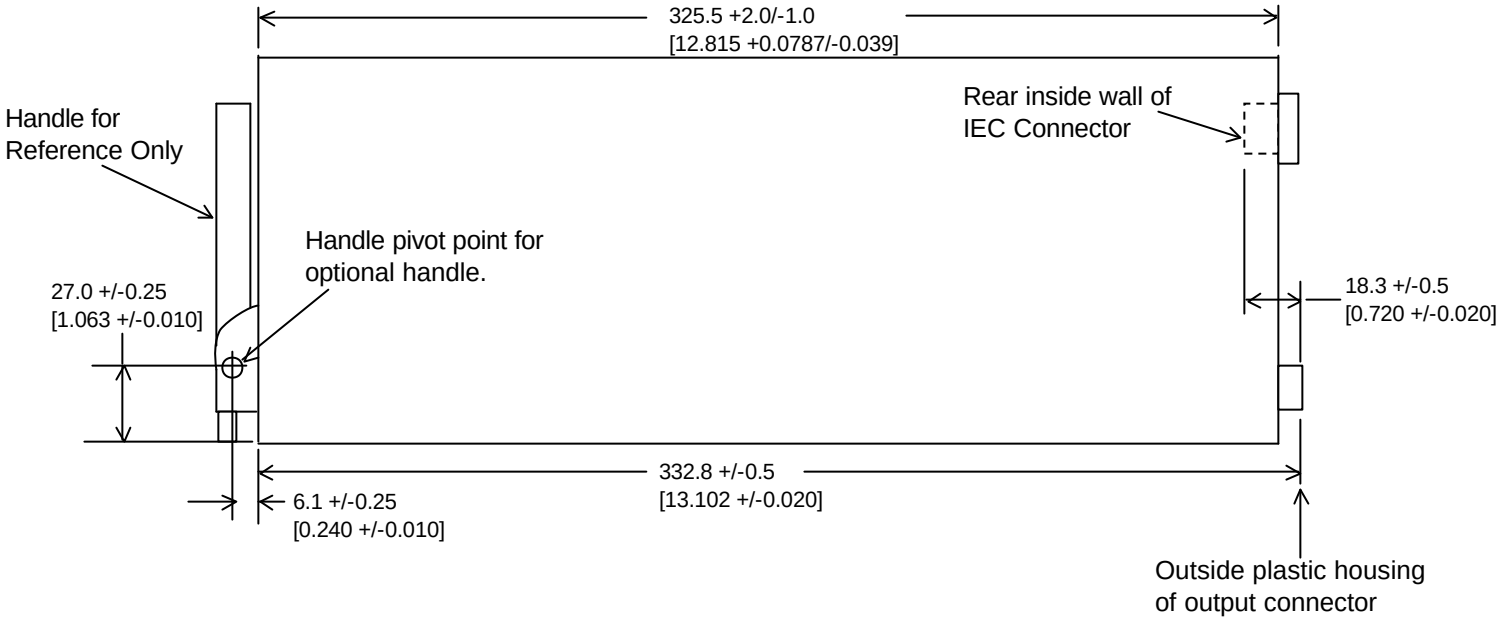

Figure 4: Side View

5.1 Connector Locations

STATUS
Required

The location of the DC output connector and AC inlet connector are shown in Figure 5. The location three guide holes are also shown. These holes provide a guide feature for mating the AC connector into the system or power bay. There must be clearance inside the power supply to allow a 1" guide pin to be inserted into these holes. These holes also provide keying for different versions of power supply that have different airflow directions. Refer to Section 5.3 for more description of airflow keying.

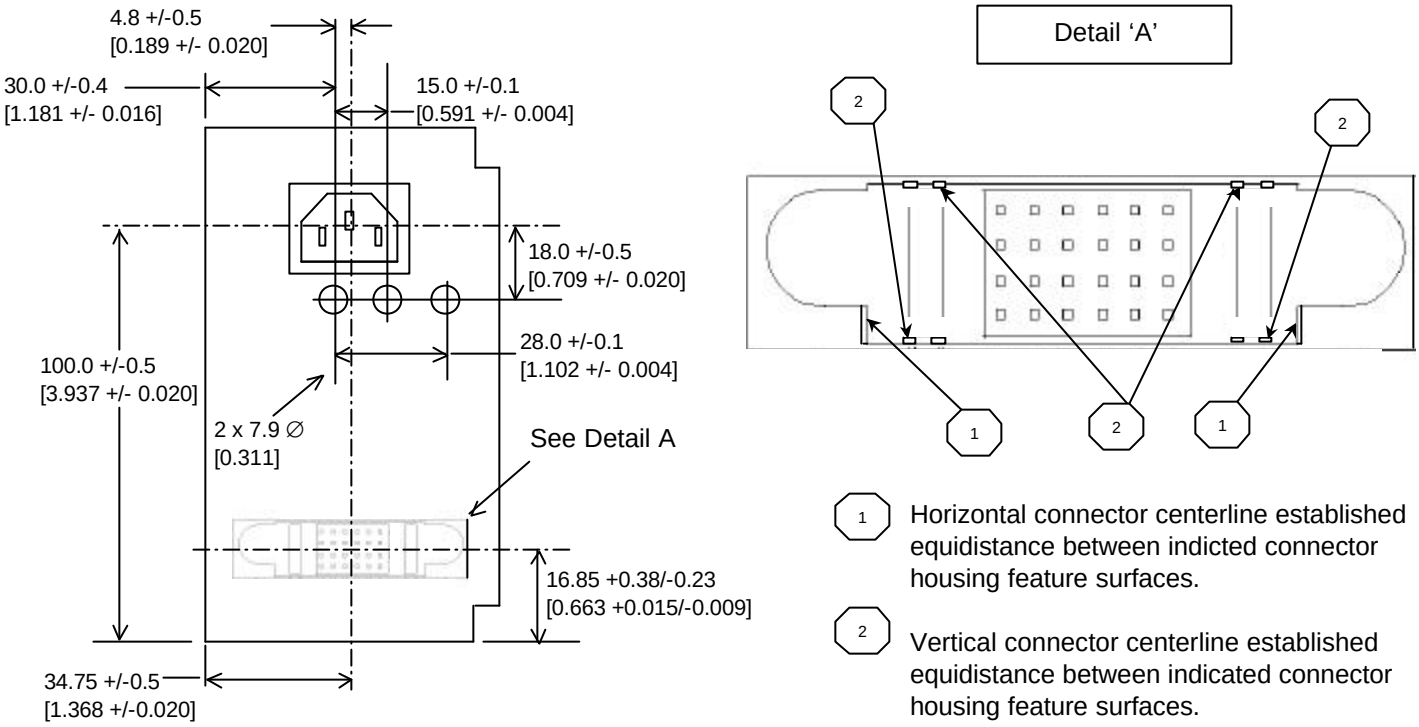

Figure 5: Interior Face

5.2 Handle and Retention Mechanism

STATUS
Required

The power supply must dock and undock into the power bay or system with less than 10 lb of insertion and extraction force when using the assistance of the power supply handle.

The retention method must hold the supply in the system during the specified shock and vibration tests without the power supply backing out of the system. The power supply retention feature must allow for functionality in the four possible orientations of the power supply. The retention mechanism must not require that a tool be used remove or insert the supply.

5.2.1 Handle/Retention Concept

STATUS
Optional

A concept drawing of an optional mechanism is shown in Figure 6.

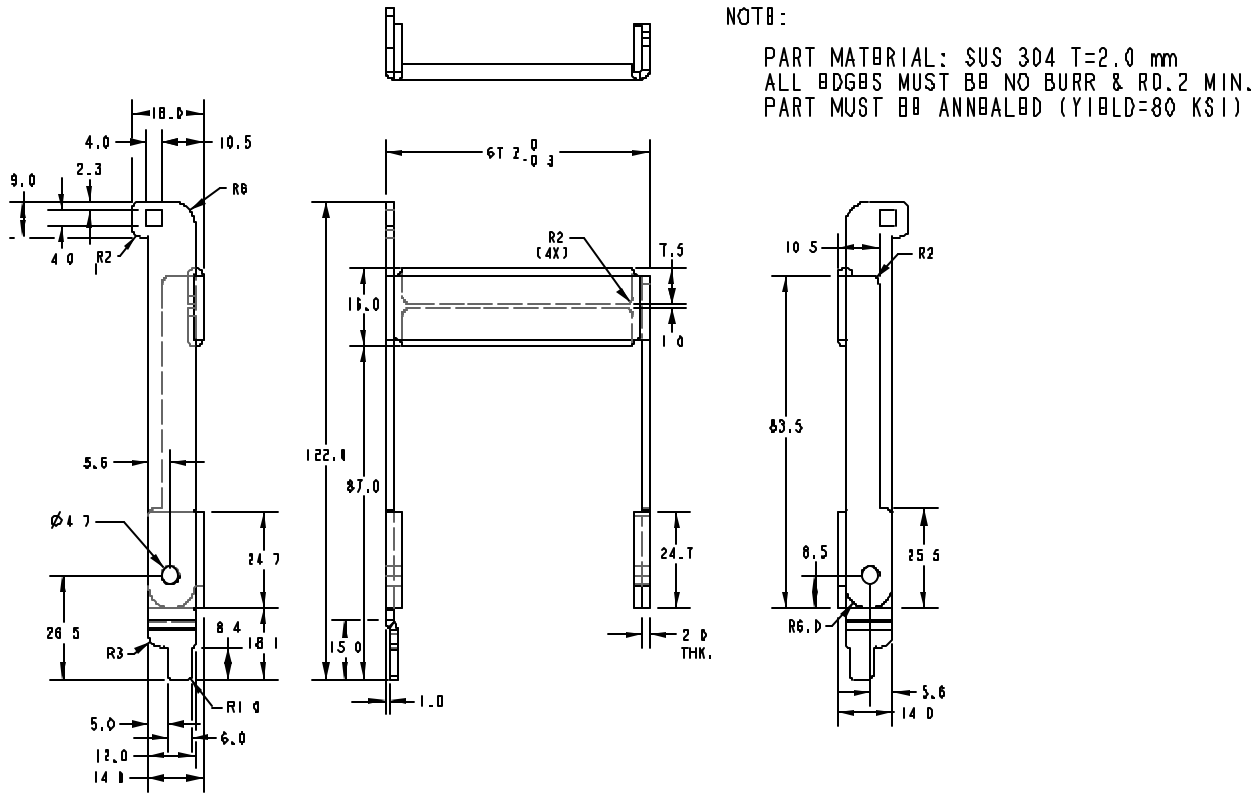

Figure 6: Handle/Retention Mechanism

5.3 Power Supply Case Keying for Airflow

STATUS
Required

The case is keyed to guarantee that power supplies with the proper airflow direction are used in the correct systems and power bays. This is done by providing different locations for the AC guide holes. Refer to Figure 7 for location details of these holes.

Keying Hole Location[1]	Side of Power Supply Air is Exhausted
1 and 3	Internal Face
1 and 2	External Face

1. Only two of the three positions are open to accept keying pins. The other must be plugged or not available to accept a keying pin.

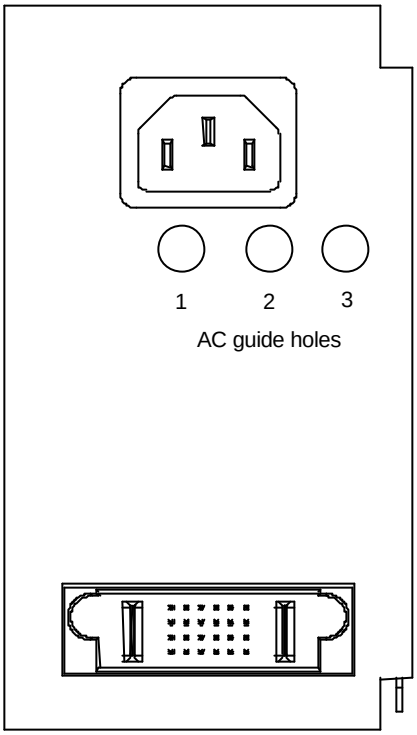

Figure 7: Airflow Keying

5.4 Airflow Requirements

STATUS
Required

The airflow direction is intake from the DC connector face and the air is exhausted on the handle face of the supply. An optional airflow direction is intake from the handle face and exhaust from the DC connector face. The power supply airflow requirements are shown in Figure 8. There are two fan performance P-Q curves shown ($PQ_{high\ fan}$, $PQ_{low\ fan}$) which may be selected by the system via the FANC signal to the power supply. These P-Q curves are the airflow of the assembled fan and power supply. The power supply may override the FANC signal and operate the fan at HIGH speed if the conditions of the power supply exceed the description for Q_{low} in the table below. The minimum airflow required by the power supply for cooling (Q_{high}, Q_{low}) are shown in Table 1. Q_{high} and Q_{low} can be tested by applying back pressure or reducing fan RPM to obtain the needed airflow for testing. The maximum back pressure which a system can present to the power supply ($PQ_{sys\ imp}$) is shown in Figure 8.

Table 1: Airflow Requirements

Item	Description	MIN	MAX	Units
Q_{high}	Airflow through power supply; max load, Tambient = 50 °C, 5000 ft elevation	20		CFM
Q_{low}	Airflow through power supply; max load, Tambient = 35 °C, 5000 ft elevation	15		CFM
$PQ_{high\ fan}$	Pressure vs airflow curve required from power supply at HIGH fan speed.	Refer to High Speed curve in Figure 8		inches H2O vs CFM
$PQ_{low\ fan}$	Pressure vs. airflow curve required from power supply at LOW fan speed.	Refer to Low Speed curve in Figure 8		Inches H2O vs CFM
PQ_{sys_imp}	Pressure vs airflow curve representing worst case backpressure on the power supply by a system.		Refer to Max System Impedance curve in Figure 8	inches H2O vs CFM

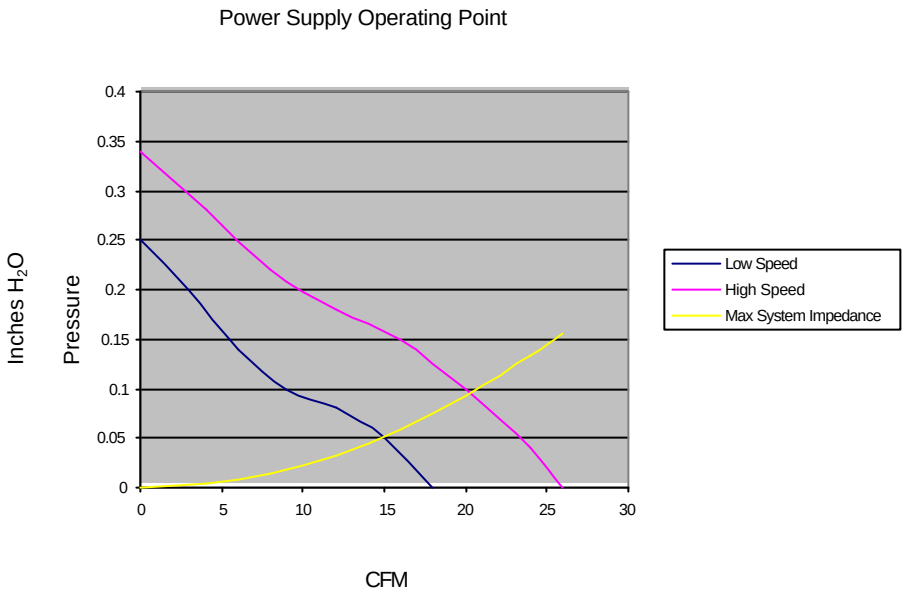

Figure 8: Power Supply Airflow P-Q Curve

5.4.1 Optional Airflow Constructions

STATUS
Optional

The power supply's internal design provides the option to create two airflow directions. The fan can be mounted to draw air through the power supply with inlet air being pulled in through the DC connector face or the fan can be mounted to push air through the power supply with exhaust air being blown out the DC connector face. These are two optional power supply constructions. Power supplies will be keyed to guarantee the proper power supply airflow direction is used for each system design. The keying method is shown in Section 5.3.

5.5 Thermal Requirements

STATUS
Required

Table 2: Thermal Requirements

Item	Description	MIN	MAX	Units
T_{op}	Operating temperature range.	0	50	°C
ΔT_{ps}	Temperature rise from inlet air to outlet air of power supply. 20 CFM, 1200 W output power, Sea level 15 CFM, 1200 W output power, Sea level		 20 27	 °C °C

T_{non-op}	Nonoperating temperature range.	-40	70	°C

The power supply must meet UL enclosure requirements for temperature rise limits. All sides of the power supply with exception to the air exhaust side, must be classified as “Handle, knobs, grips, etc. held for short periods of time only”.

5.6 Acoustic Requirement

STATUS
Required

The power supply must run at LOW fan speed under the conditions defined for Q_{low} in Table 1. The power supply must have less than 41 dBA of sound pressure noise (L_p) at any bystander microphone location when operating at LOW fan speed.

The test setup shall be as follows: The PSU is a desktop module with bystander locations only. The PSU is to be placed on a table 28 to 36 inches high with the position of four bystander microphones. The microphones will be 1 meter away, centered on each side, 1.5 meters high, as measured from the floor, and placed at a 30° down angle. The A-weighted (100 -10 kHz) sound pressure must be measured at the four bystander positions. Sound pressure is a measurement of the total noise at the specified microphone location in the room.

6 AC Input Requirements

STATUS
Required

The power supply shall incorporate universal power input with active power factor correction, which shall reduce line harmonics in accordance with the *EN61000-3-2* and *JEIDA MITI* standards.

6.1 AC Inlet Connector

STATUS
Required

The AC input connector is an *IEC 320 C-14* power inlet.

6.2 AC Input Specification

STATUS
Required

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% THD must not cause the power supply to go out of specified limits.

Table 3: AC Input Voltage

Parameter	MIN	Rated	MAX	MAX Input Current	O/P Power
Vin	90 V_{rms}	100-120 V_{rms}	140 V_{rms}	10.0 A_{rms}	700 W
Vin	180 V_{rms}	200-240 V_{rms}	264 V_{rms}	9.0 A_{rms}	1200 W
Vin Frequency	47 Hz	50/60 Hz	63 Hz		

Note: The Max Input Current shall scale with amount of output power. Example: For a power supply with 1400 W of output power at 200-240 V_{rms}, the Max Input Current shall be 9.0 * (1400/1200) = 10.5 A_{rms}.

6.3 Efficiency

STATUS
Required

The power supply will have a minimum efficiency of 80% at maximum load and 90 VAC.

The power supply will have a minimum efficiency of 85% at maximum load and 180 VAC.

6.4 AC Multiple Phase Input Capability

STATUS
Required

Power supplies must be designed to enable power bay and system implementations that use multiple-phase AC input power. In this configuration, not all power supplies in a power bay are required to be on the same AC power phase.

6.5 AC Line Dropout

STATUS
Required

An AC line dropout is defined to be when the AC input drops to 0 VAC for one cycle or less of the AC input during any phase of the AC line. During an AC dropout the power supply must meet voltage regulation requirements (Table 10) over the rated load. An AC line dropout shall not cause any tripping of control signals or protection circuits. If the AC dropout lasts longer than one cycle of the AC line, then the power supply should recover and meet all turn on requirements. The power supply must meet the AC dropout requirement over rated AC voltages, frequencies, and output loading conditions. Any dropout of the AC line shall not cause damage to the power supply.

6.6 AC Brownout Requirement

STATUS
Optional

To meet the AC Brownout Requirements the optional ACOK# and ACRange signals must be implemented along with circuits external from the power supply. The circuits external from the power supply control the PSON# signal based upon the ACOK# signals received from the power supplies. When enough ACOK# signals are asserted from the power supplies, all power supplies are enabled via the PSON# signal. The ACRange signal enables the ability to meet the brownout requirement over the 200-240 VAC range, otherwise, it defaults to the 100-240 VAC range.

AC Turn Off Requirement
The Power system must be able to return to normal power up state after a slow brownout condition. The brownout is tested in all valid redundant power system configurations. While the power system is operating at full rated DC load, the AC line voltage is reduced from 180 VAC/50 Hz to 0 VAC and 90 VAC/60 Hz to 0 VAC at a constant rate over a period of 30 minutes. The power is then reapplied at 180 VAC/50 Hz and 90 VAC/60 Hz. The system must return to a normal power up state.

AC Turn On Requirement
The power system must be able to return to normal power up state after a slow recovery condition. The recovery is tested in all valid redundant power system configurations the system. With the test loads configured for maximum system DC output in resistive mode, the AC line voltage is increased from 0 VAC to 180 VAC/50 Hz and 0 VAC to 90 VAC/60 Hz at a constant rate over 30 minutes. The system must return to a normal power up state.

6.7 AC Line Fuse

STATUS
Required

The power supply shall have two line fuses, one for each side of the AC input. AC line fusing shall be acceptable for all safety agency requirements. AC inrush current shall not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

6.8 AC Line Inrush

STATUS
Required

AC line inrush current shall not exceed 35 A peak for one-quarter or more of the AC cycle. The inrush current must not exceed the I^2t curve shown in Figure 9. The inrush current must not exceed 100 A peak for any duration of time.

The power supply must meet the inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, during hot plug, during any AC dropout condition, over the specified temperature range (T_{op}), and during AC power cycling. The AC power cycling test condition is defined as cycling the AC power off and back on five times after the power supply has been operating at maximum load and has reached thermal stability. The period between the five AC power cycles could anywhere between 1 ms to 1 s. The duration of the off time for each the power cycles could be anywhere between 1 ms and 1 s.

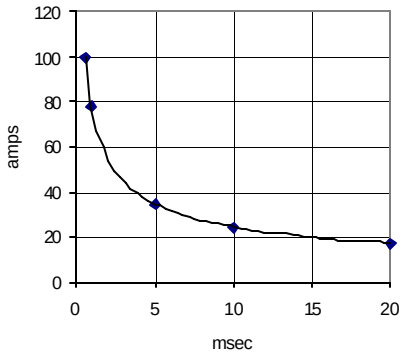

Figure 9: Inrush Limit

6.9 Maximum AC Leakage Current to Ground

STATUS
Required

The maximum leakage current to ground for each power supply is 0.75 mA when tested at 240 VAC.

6.10 AC Line Transient Specification

STATUS
Required

AC line transient conditions are defined as “sag” and “surge” conditions. Sag conditions also commonly referred to as “brownout”; these conditions are defined as the AC line voltage dropping below nominal voltage conditions. “Surge” is defined to refer to conditions when the AC line voltage rises above nominal voltage. The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 4: AC Line Sag Transient Performance

AC Line Sag				
Duration	**Sag**	**Operating AC Voltage**	**Line Frequency**	**Performance Criteria**
Continuous	10%	Nominal AC Voltage	50/60 Hz	No loss of function or performance
0 to 1 AC Cycle	100%	Nominal AC Voltages	50/60 Hz	No loss of function or performance
>1 AC cycles	>10%	Nominal AC Voltages	50/60 Hz	Loss of function acceptable, self recoverable

Table 5: AC Line Surge Transient Performance

AC Line Surge				
Duration	**Surge**	**Operating AC Voltage**	**Line Frequency**	**Performance Criteria**
Continuous	10%	Nominal AC Voltages	50/60 Hz	No loss of function or performance
0 to ½ AC cycle	30%	mid-point of nominal AC Voltages	50/60 Hz	No loss of function or performance

6.11 AC Line Fast Transient Specification

STATUS
Required

The power supply shall meet the *EN61000-4-5* directive and any additional requirements in *IEC1000-4-5:1995* and the Level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

- These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits.
- The surge-withstand test must not produce damage to the power supply.
- The supply must meet surge-withstand test conditions under maximum and minimum DC-output load conditions.

7 DC Output Specification

The power supply must have a main 48 VDC output and a low current 12 VSB output. The 12 VSB output is always available when AC input power is applied to the power supply (with the exception of a fault condition that has opened the AC line fuse(s)). 12 VSB is used to power system components (i.e., server management) that must be available when the system is powered down.

7.1 DC Power Connector Requirements

STATUS
Required

The DC connector shall have the pin-out illustrated in Table 7. The DC power connector is the Berg 51415-001 or equivalent. The connector is illustrated in Figure 10. The connector location on the power supply is shown in Figure 5.

NOTE

Signals that can be defined as low true or high true use the following convention: signal# = low true

Table 6: Signal Descriptions

Signal	Description	Signal	Description	Signal	Description
48LS	48 V load share bus	PWOK	Power OK output	SCL	I^2C Clock signal
12 VSB	12 V standby output	ACOK#	AC OK output	SDA	I^2C Data signal
12 VSB Return	12 V standby return	ACRange	AC input range select	A0	I^2C address bit 0
PSON#	Power enable input	PSKILL	Supply fast shutdown	A1	I^2C address bit 1
PRESENT#	Power supply present	FAIL	Failure signal	A2	I^2C address bit 2
FANC	Fan control signal	PRFL	Predictive failure	PSAlert#	Power supply alert
FANP	Fan power input pin				

Table 7: Output Connector Pin-out

Signal Pins						
	1	2	3	4	5	6
D	12 VSB	12 VSB Return	48LS	ACRange	SCL	A0
C	12 VSB	12 VSB Return	ACOK#	PRFL	Reserved	A1
B	12 VSB	12 VSB Return	PSON#	PSKILL[1]	SDA	A2
A	FANP	PSAlert#	PRESENT#	PWOK	FAIL	FANC

Power Blades	
P1	P2
48 VDC Return	48 VDC

1. Pin B4 is shortened to allow the PSKill pin to shut down the power supply properly during hot swapping of the power supply.

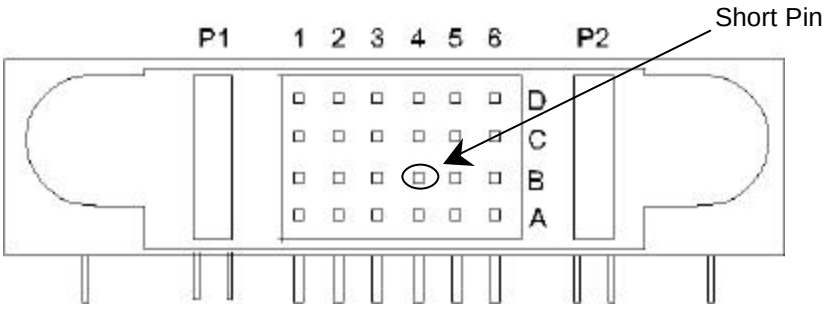

Figure 10: DC Output Connector

7.2 DC Output Rating

STATUS
Required

The 48 VDC and 12 VSB outputs must meet ALL requirements over the loading and AC input conditions as shown in Table 8. The 12 VSB output must meet all requirements with the power supply operational (PSON = Low) or in standby mode (PSON = Open). When in standby mode the power supply fan must be OFF.

Table 8: DC Output Rating

Output	Low Load (Amps)	High Load (A)	Input Voltage (VAC)
48 VDC	10% of Max	24	180 - 264 VAC
12 VSB	0	4.0	180 - 264 VAC
48 VDC	10% of Max	13.5	90 - 132 VAC
12 VSB	0	4.0	90 - 132 VAC

The 48 VDC output shall have a peak output capacity 110% of maximum load. The duration of the peak current capacity shall be 10 s.

7.2.1 No Load Operation

STATUS
Required

The power supply operation at no load shall meet all requirements with the exception of the transient loading requirements.

7.3 Grounding

STATUS
Required

The 12 VSB Return must be connected to the power supply chassis and to earth ground of the AC inlet internally to the supply. All control signals are referenced to the 12 VSB Return (chassis ground). The 48 VDC Return and 48 VDC output must be isolated from the 12 VSB Return and 12 VSB output by greater than 10 kΩ. The resistance from chassis ground to either side of the 48 VDC output must be greater than 10 kΩ. The power supply must be able to operate within specified limits if a voltage of V_{CMop} is applied at 48 VDC Return referenced to the 12 VSB Return (power supply chassis ground). If V_{CMop} exceeds this range, the power supply may shut down, however, this must not damage the power supply. The power supply must not be damaged if a voltage of $V_{CMfloat}$ is applied at 48 VDC Return referenced to the 12 VSB Return (power supply chassis ground). The voltage at 48 VDC Return referenced to 12 VSB Return (power supply chassis ground) must not exceed $V_{CMfloat}$ if the 48 VDC output is floating.

Table 9: 48 VDC Isolation Requirements

Characteristic	Description	MIN	MAX
$R_{isolation}$	Isolation from 12 VSB Return (chassis ground) to the 48 VDC Return.	10 kΩ	
V_{CMop}	Voltage applied to 48 VDC Return referenced to 12 VSB Return. The power supply must operate within all specified limits.	-1.0 V	0 V
$V_{CMfloat}$	Voltage applied between 48 VDC Return and 12 VSB Return by an external voltage. The supply must not be damaged under this condition. Voltage present between 48 VDC Return and 12 VSB Return during normal operation with the 48 VDC Return floating.	-50 V	+50 V

7.4 Regulation

STATUS
Required

The 48 VDC and 12 VSB outputs do not require remote sensing. All voltage regulation measurements are made at the output connector of the power supply. These limits do not include the peak-peak ripple/noise specified in Section 7.7. The power supply must hold regulation limits under all operating conditions (AC line, transient loading, and output loading) as shown in Table 10.

Table 10: DC Output Regulation

Output	MIN	NOM	MAX	Units	% Reg
48 VDC	+45.6	+48.0	+50.4	Volts	+/-5%
12 VSB	+12.0	+12.5	+13.00	Volts	+/-4%

7.5 Transient Loading

STATUS
Required

The power supply must operate within specified limits and meet regulation requirements over the following transient loading conditions. The transient load can occur anywhere within the load range of the power supply. This is tested with no additional bulk capacitance.

Table 11: Transient Response

Output	Step Size	Slew Rate	Number of Power Supplies in Parallel
48 VDC	50% of max	0.25 A/µs	1
48 VDC	50% of max	0.50 A/µs	2
48 VDC	50% of max	0.75 A/µs	3
48 VDC	50% of max	1.0 A/µs	4
48 VDC	50% of max	1.0 A/µs	5
48 VDC	50% of max	1.0 A/µs	6
12 VSB	100% of max	1.0 A/µs	1

7.6 Capacitive Load

STATUS
Required

The power supply must operate within specified limits over a capacitive load range define in Table 12.

Table 12: Capacitive Loading

Output	MIN	MAX	Number of Power Supplies in Parallel
48 VDC	0 µF	10,000 µF	1
48 VDC	0 µF	20,000 µF	2
48 VDC	0 µF	30,000 µF	3
48 VDC	0 µF	40,000 µF	4
48 VDC	0 µF	50,000 µF	5
48 VDC	0 µF	60,000 µF	6

7.7 Ripple and Noise

STATUS
Required

Ripple and noise are measured with 0.1 µF of ceramic capacitance and 10 µF of tantalum capacitance on each of the power supply outputs. These capacitors are located at the power supply output connector. The ripple and noise requirements shall be met over all load ranges and AC line voltages with one to six power supplies in parallel operation. The output noise requirements apply over a 0 Hz to 20 MHz bandwidth. These requirements are specified in Table 13.

Table 13: Ripple and Noise

Output	Maximum Ripple and Noise
48 VDC	480 mVp-p
12 VSB	120 mVp-p

7.8 12 VSB

STATUS
Required

12 VSB is a standby voltage that may be used to power circuits that require power during the powered-down state of all power rails. 12 VSB is required for the implementation of PSON# and other system circuits that must stay powered when the system is turned off.

7.9 Hot Swap Requirement

STATUS
Required

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits specified in Table 10 with the capacitive load specified Table 12. The hot swap test must be conducted when the system is operating under both static and dynamic conditions. The power supply can be hot swapped by the following methods:

- Up to four power supplies may be on a single AC line. Extraction: The AC power will be disconnected from the power supply as the power supply is being extracted from the system. This could occur in standby mode or powered on mode. Insertion: The AC power will be connected to the power supply as the supply is inserted into the system and the supply will power on into standby mode or powered on mode.

- Server management turning on the hot swapped power supply. Extraction: Server management turns off only one of the power supplies via the PSON# signal, then the power supply is removed from the system. Insertion: Power supply is inserted into the system, server management looks for power supply, depending upon the state of the system (on or off), the system then turns on the power supply via the PSON# signal or goes to standby mode operation.

Many variations of the above are possible. Supplies need to be compatible with these different variations. In general, a failed (off by internal latch or external control) supply may be removed, then replaced with a good power supply, however, hot swap needs to work with operational as well as failed power supplies. The newly inserted power supply may get turned on by inserting the supply into the system or by system management recognizing an inserted supply and explicitly turning it on.

7.9.1 Output Isolation

STATUS
Required

All outputs must have an isolating device to isolate the power supply from the system power during a power supply failure or during a hot swap operation. This device must be located in the power supply. This device can be an or'ing diode or functional equivalent.

7.10 Timing Requirements

STATUS
Required

These are the timing requirements for single power supply operation. Timing is defined for turn on and turn off of the power supply. The output voltage must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 300 ms. Outputs must rise monotonically. The timing of signals and power are specified in Table 14 and described in Figure 11.

Table 14: Turn On/Off Timing

Item	Description	MIN	MAX	Units
T_{vout_rise}	Output voltage rise time from each main output.	5	300	ms
$T_{sb\_on\_delay}$	Delay from AC being applied to 12 VSB being within regulation.		1500	ms
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	ms
T_{vout_holdup}	Time all output voltages, including 12 VSB, stay within regulation after loss of AC.	21		ms
T_{pwok_holdup}	Delay from loss of AC to deassertion of PWOK	20		ms
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
T_{pson_pwok}	Delay from PSON# deactive to PWOK being deasserted.		50	ms
T_{acok_delay}	Delay from loss of AC input to deassertion of ACOK#.	20		ms
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	1000	ms
T_{pwok_off}	Delay from PWOK deasserted to 48 VDC or 12 VSB dropping out of regulation limits.	1		ms
T_{pwok_low}	Duration of PWOK being in the deasserted state during an off/on cycle using AC or the PSON# signal.	100		ms
T_{sb_vout}	Delay from 12 VSB being in regulation to 48 VDC being in regulation at AC turn on.	50	1000	ms

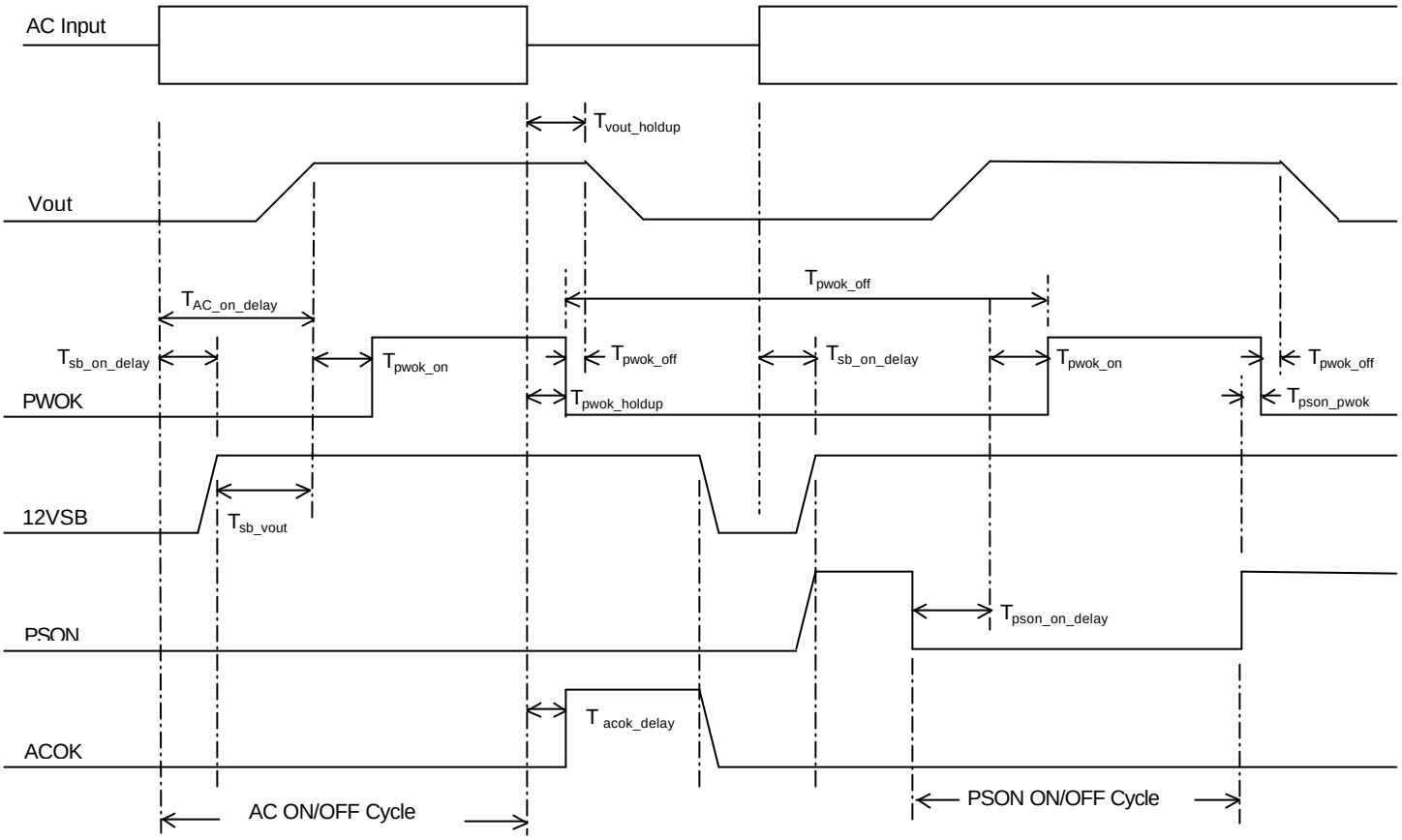

Figure 11: Turn On/Off Timing

7.11 Forced Load Sharing

STATUS
Required

The 48 VDC output shall have forced load sharing. The output must share within 6.7% at full load, as shown in the example below and in Table 15. All current sharing functions are implemented internal to the power supply by making use of the 48LS signal. The system connects the 48LS signals between the power supplies. The supplies must be able to load share with up to six power supplies in parallel and operate in a hot swap/redundant n+1 configuration where n=1, 2, 3, 4, and 5.

Example: Power supply #1 = 15.0 A
Power supply #2 > 14.0 A and < 16.0 A

Table 15: System Load

Number of Power Supplies	System Maximum Current (Amps) for Non-redundant Power Supply Configurations			System Maximum Power (W)	
	100-120 VAC	200-240 VAC	100-120 VAC and 200-240 VAC	100-120 VAC	200-240 VAC
	48 VDC	48 VDC	12 VSB		
1	13.5	24	4	700	1200
2	26	46	8	1350	2300
3	38	68	12	2000	3400
4	51	91	16	2650	4550
5	63	113	20	3300	5650
6	76	135	24	3950	6750

7.11.1 Load Sharing Control

STATUS
Required

The power supplies load share by using a single load share bus signal connected between the power supplies for the 48 VDC output. If the load sharing is disabled by shorting the load share bus to ground, the power system must continue to operate within regulation limits for loads less than or equal to one power supply. The failure of a power supply should not effect the load sharing or output voltages of the other supplies still operating. The power supplies must be able to load share with up to 100 mV of drop between the grounds of the different power supply outputs.

7.11.2 Load Share Signal Characteristics

STATUS
Recommended

The load share signal provides both output current information and the load sharing function. The characteristics of the load share signal is defined below in Table 16.

Table 16: Load Share Bus Output Characteristic

Item	Description	MIN	NOM	MAX	Units
V_{share}; I_{out}=max	Voltage of load share bus at specified max output current.		8		V
$\Delta V_{share}/\Delta I_{out}$; I_{out}>1 A	Slope of load share bus voltage with changing load.		8 / I_{outmax}		V / A
I_{share} sink; V_{share}=8 V	Amount of current the load share bus output from each power supply sinks.			0.5	mA
I_{share} source; V_{share}=8 V	Amount of current the load share bus output from each power supply sources.	4.0			mA
T_{share} ; I_{out}=max	Delay from output voltages in regulation to load sharing active with maximum load of one power supply and two power supplies in			100	ms

	parallel.				

7.11.3 Standby Load Sharing

STATUS
Required

The 12 VSB output must be able to provide an additional 4.0 A of output current for each additional power supply added in parallel. Each power supply in the system will deliver current up to the current limit point, as stated in Section 8.2. At this point the power supply will go into constant current mode and allow other power supplies in the system to deliver additional standby current.

Table 17: Standby Load Sharing

Number of Supplies in Parallel	12 VSB Load
1	4.0 A
2	8.0 A
3	12.0 A
4	16.0 A
5	20.0 A
6	24.0 A

8 Protection Circuits

STATUS
Required

Protection circuits inside the power supply shall cause only the power supply's main outputs to shutdown. The 12 VSB output shall remain powered on if the failure does not involve this output. When a protection circuit shuts down the power supply both the FAIL LED and the FAIL signal will be activated. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15 s and a PSON# cycle HIGH for 1 s must be able to reset the power supply.

8.1 Over-voltage Protection

STATUS
Required

The power supply's over voltage protection shall be locally sensed. The power supply shall shutdown in a latch off mode after an over voltage condition. This latch can be cleared by toggling the PSON# signal or by an AC power interruption. Table 18 contains the over voltage limit. The values are measured at the output of the Power Supply DC connector.

Table 18: Over-voltage Protection Requirements

Output	MAX	Units
48 VDC	55	volts

8.2 Over-current / Short Circuit Protection

STATUS
Required

The power supply shall have current limit to prevent the 48 VDC output from exceeding the value shown in Table 19. The current limiting shall be of the constant current type for both the 48 VDC and 12 VSB outputs. When in current limit for loads less then 600% of maximum, the output current must not decrease as the load resistance decreases.

The over current limit level for the 48 VDC output shall be maintained for a period of 2.5 s minimum and 6 s maximum. For loads greater than 600% of maximum rating on the 48 VDC output the power supply may shutdown in less than 2600 ms.

The over current limit for the 12 VSB output shall be maintained indefinitely, without shutting down the power supply, for loads less than 24 A. For loads greater than 24 A on the 12 VSB output the power supply may shutdown in less than 1500 ms.

After this current limit time for the 48 VDC output the power supply shall latch off. If the load on the 12 VSB output is greater than 24 A the power supply may latch off to protect the power supply. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition.

Table 19: Over Current Protection

VOLTAGE	OVER CURRENT LIMIT(Iout limit)
48 VDC	110% minimum; 150% maximum
12 VSB	100% minimum; 125% maximum

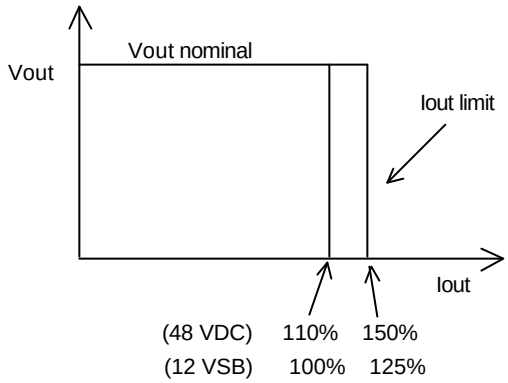

Figure 12: Current Limit Characteristic

8.3 Thermal Protection

STATUS
Required

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will be shutdown with the exception of the 12 VSB output. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically. The OTP circuit must have built in hysteresis such that the power supply will not oscillate on and off due to temperature recovering condition. The power supply shall alert the system of the OTP condition via the power supply FAIL signal and the FAIL LED indicator.

9 Control and Indicator Functions

The following sections define the input and output signals from the power supply. Signals that can be defined as low true or high true use the following convention: *signal#* = low true.

9.1 PSON# (Power Supply Enable)

STATUS
Required

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the 48 VDC power rail. When this signal is not pulled low by the system, or left open, the 48 VDC output turns off and the 12 VSB output remains on. The power supply is in standby mode when PSON# is not pulled low or left open. When the power supply is in standby mode the power supply fan must be OFF. PSON# is pulled to a bias voltage by a pull-up resistor internal to the power supply. This bias voltage shall be present when the power supply shuts down due to any protection circuits or when the 12 VSB goes into current limit. Refer to Figure 11 for the timing diagram.

Table 20: PSON# Signal Characteristic

Signal Type	Accepts an open collector/drain input from the system. Pull-up to housekeeping voltage independent of 12 VSB located in power supply.	
PSON# = Low, PSKILL = Low	ON	
PSON# = Open, PSKILL = Low or Open	OFF	
PSON# = Low, PSKILL = Open	OFF	
	MIN	**MAX**
Logic level low (power supply ON)	0 V	1.0 V
Logic level high (power supply OFF)	2.0 V	5.25 V
Source current, Vpson = low		1 mA
Power up delay: $T_{pson\_on\_delay}$	5 ms	400 ms
PWOK delay: T_{pson_pwok}		50 ms

9.2 PSKill

STATUS
Required

The purpose of the PSKill pin is to allow for hot swapping of the power supply. The PSKill pin on the power supply is shorter than the other signal pins. When a power supply is operating in parallel with other power supplies and then extracted from the system, the PSKill pin will quickly turn off the power supply and prevent arching of the DC output contacts. The DC output contacts must not arch under this condition. T_{PSKill} (shown below in Table 21) is the minimum time delay from the PSKill pin unmating to when the power pins unmate. The power supply must discharge its output inductor within this time from the unmating of the PSKill pin. When the PSKill signal is not pulled down or left opened (power supply is extracting from the system), the power supply should shut down regardless of the condition of the PSON# signal. The mating pin of this signal in the system should be tied to ground. Internal to the power supply, the PSKill pin should be connected to a standby voltage through a pull-up resistor. Upon receiving a LOW state at the PSKill pin, the power supply will be allowed to turn on via the PSON# signal. A logic LOW on this pin by itself should not turn on the power outputs.

Table 21: PSKill Signal Characteristics

Signal Type (Input Signal to Supply)	Accepts a ground input from the system. Pull-up to VSB located in the power supply.	
PSKILL = Low, PSON# = Low	ON	
PSKILL = Open, PSON# = Low or Open	OFF	
PSKILL = Low, PSON# = Open	OFF	
	MIN	**MAX**
Logic level low (power supply ON)	0 V	1.0 V
Logic level high (power supply OFF)	2.0 V	5.25 V
Source current, VOSKill = low		4 mA
Delay from PSKill = High to power supply turned off (T_{PSKill})[1]		100 µs

1. T_{PSKill} is the time from the PSKill signal deasserting HIGH to the power supply's output inductor discharging.

9.3 AC Input Range Setting (ACRange)

STATUS
Optional

ACRange allows the power supply to meeting the AC Brownout requirement over the 200-240 VAC input voltage range. Refer to Table 22. It communicates the AC input voltage range the power supply is operating at by setting the trip point for the ACOK# signal. If the signal is open, the power supply defaults to the 100-240 VAC input range. If the signal is pulled low, the range is set to 200-240 VAC.

Table 22: ACRange Signal Characteristic

Signal Type	Accepts an open collector/drain input from the system. Pull-up to VSB located in the system.	
ACRange = Low	200-240 VAC	
ACRange = Open (Default)	100-240 VAC	
	MIN	**MAX**
Logic level low voltage (200-240 VAC)	0 V	1.0 V
Logic level high (100-240 VAC)	2.0 V	5.25 V
Source current, Vacrange = low		4 mA

9.4 ACOK# Signal

STATUS
Optional

ACOK# allows the power supply to meet the AC Brownout requirement with multiple power supplies in parallel. Refer to Table 23. This signal is pulled LOW when the AC input voltage has reached the minimum level defined by the ACRange signal. The characteristic of the ACOK# signal is shown in Table 23. Refer to Figure 11 for timing diagram.

The purpose of this signal is to synchronize the power on timing of multiple power supplies within the system. The system will monitor the ACOK# signals. When enough ACOK# signals are active to allow the system to be powered on, the system will activate the PSON# signals to all power supplies.

Table 23: ACOK# Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located in system.	
ACOK# = Low	AC OK	
ACOK# = High	AC Low	
	MIN	**MAX**
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isink=50 mA		5.25 V
Sink current, ACOK# = low		4 mA
Sink current, ACOK# = high		50 µA
ACOK# trip point for 200-240 VAC		175 VAC
ACOK# trip point for 100-240 VAC		85 VAC
ACOK# Delay: T_{acok_delay}	20 ms	
ACOK# rise and fall time		100 µs

9.5 PWOK (Power Good)

STATUS
Required

PWOK is a power good signal and will be pulled HIGH by the power supply to indicate that all the outputs are above the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be deasserted to a LOW state. See Figure 11 for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall be inhibited as long as any power supply's 48 VDC output is in current limit or the 12 VSB output is below the regulation limit.

Table 24: PWOK Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located power supply.	
PWOK = High	Power Good	
PWOK = Low	Power Not Good	
	MIN	**MAX**
Logic level low voltage, Isink = 4 mA	0 V	0.4 V
Logic level high voltage, Isource = 2 mA	2.4 V	5.25 V
Sink current, PWOK = low		4 mA
Source current, PWOK = high		2 mA
PWOK delay: T_{pwok_on}	100 ms	1000 ms
PWOK rise and fall time		100 µs
Power down delay: T_{pwok_off}	1 ms	200 ms

9.6 Predictive Failure Signal (PRFL)

STATUS
Optional

This signal indicates that the power supply (or power supply fan) is reaching its end of life. The signal indicates a predictive failure when the power supply allows this signal to go HIGH.

Table 25: PRFL Signal Characteristics

Signal Type (Active Low)	Open collector/drain output from power supply. Pull-up to VSB located in system.	
PRFL = High	Failing	
PRFL = Low	OK	
	MIN	**MAX**
Logic level low voltage, Isink = 4 mA	0 V	0.4 V
Logic level high voltage, Isink=50 mA		5.25 V
Sink current, FAIL = low		4 mA
Sink current, FAIL = high		50 µA
PRFL rise and fall time		100 µs

9.7 Power Supply Failure (FAIL)

STATUS
Required

In the event of a power supply failure (OVP at any output, UV at any output, Fan Failure, or other failure), this signal is allowed to go HIGH by the power supply.

Table 26: FAIL Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located system.	
FAIL = High	Failed	
FAIL = Low	OK	
	MIN	**MAX**
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isink=50 mA		5.25 V
Sink current, FAIL = low		4 mA
Sink current, FAIL = high		50 µA
FAIL rise and fall time		100 µs

9.8 Power Supply Present Indicator (PRESENT#)

STATUS
Required

The PRESENT# signal is used to sense the number of power supplies in the system (operational or not). This signal is connected to the power supply's output ground.

Table 27: PRESENT# Signal Characteristics

Signal Type	Output from power supply that is connected to ground. Pull-up to VSB located in system.	
PRESENT# = Low	Present	
PRESENT# = High	Not Present	
	MIN	**MAX**
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isink=50 mA		5.25 V
Sink current, PRESENT# = low		4 mA
Sink current, PRESENT# = high		50 µA

9.9 Fan Control (FANC)

STATUS
Required

The requirements for the FANC signal are identical to that of the ATX specification. The FANC signal is a fan speed and shutdown control signal. The fan speed and shut down are controlled by a variable voltage on this pin. This signal allows the system to request control of the power supply fan. The control circuit in the system supplies voltage to this pin from 12 VDC to 0 VDC for the fan control request. If the FANC signal is left open, the fan control defaults to High speed.

Table 28: FANC Signal Characteristics

Signal Type	Accepts an input voltage from the system. Pull-up to 12 V inside the power supply.	
FANC < 1 V	Fan in SLEEP mode[1,2,4]	
2 V < FANC < 3V	Fan in LOW speed[1,4]	
3 V < FANC < 10.5 V	Fan ramps from LOW to HIGH speed[1,4]	
FANC > 10.5 V	Fan in HIGH speed	
	MIN	**MAX**
Source current		2 mA
Fan OFF output power[2]		50 W
Fan LOW speed ambient temperature[3]		35 °C

1. This is a request from the system to the power supply to operate the fan at this condition. The power supply can over ride this request and increase the fan speed if the power supply requires more cooling. Refer to Section 5.6 for LOW speed requirements. Refer to note 2 for fan SLEEP mode requirements.
2. When the power supply fan is in SLEEP mode the fan must be operating at its minimum RPM, which is slow enough to not output any noticeable audible levels. The power supply must be able to supply 0 W to 50 W of output power at 50 °C ambient (on the 48 VDC output) in the power supply fan SLEEP mode condition without the power supply over riding and turning the fan to LOW or HIGH speed.
3. This is the ambient temperature the power supply must be able to supply maximum load at LOW fan speed. Refer to Section 5.4 for a description of requirements for operating at LOW fan speed.
4. When the power supply overrides the FANC signal to control the fan, it shall do so without the fan oscillating between different speeds for any operating ambient temperature.

9.10 Fan Power Input (FANP)

STATUS
Required

The FANP signal is an input power pin to the power supply. It is used to provide power to the power supply fan in the case of a power supply failure or loss of AC power to the power supply. A failure inside the power supply shall not cause any disturbance on the power connected to FANP. The fan inside the power supply shall turn off if the power supply is disabled with the PSON# signal. The FANC signal shall still be able to control the fan speed when the power supply fan is being powered from FANP.

Table 29: FANP Signal Characteristics

Signal Type	Accepts input power from the system to operate the power supply fan when supply has failed or loss of AC.	
FANP = 11.4 V to 13.0 V **PSON# = Low** **Power Supply = ON**	Fan(s) operating. No current draw from FANP. Fan powered internally.	
FANP = 11.4V to 13.0 V **PSON# = High** **Power Supply = OFF or Failed or No AC**	Fan(s) not operating. No current draw from FANP.	
FANP = 11.4 V to 13.0 V **PSON# = Low** **Power Supply = Failed or No AC**	Fan(s) operating, powered from FANP.	
FANP = Open **PSON# = Low** **Power Supply = ON**	Fan(s) operating. Fan powered internally.	
FANP = Open **PSON# = High** **Power Supply = OFF or Failed or No AC**	Fan(s) not operating.	
FANP = Open **PSON# = Low** **Power Supply = Failed or No AC**	Fan(s) not operating.	
	MIN	**MAX**
FANP Voltage	11.4 V	13.0 V
FANP Peak Sink current; @ Power On, FANP = 12.5 V (600 ms max duration)		1.0 A
FANP Continuous Sink current; FANP = 12.5 V		600 mA

9.11 PSAlert#

STATUS
Optional

This signal indicates that the power supply is experiencing a problem that the user should investigate. The signal shall activate in the case of over temperature, general failure, over current, over voltage, and under voltage. This signal may also indicate the power supply is reaching it end of life or is operating in an environment exceeding the specified limits.

Table 30: Alert# Signal Characteristics

Signal Type (Active Low)	Open collector/drain output from power supply. Pull-up to VSB located in system.	
Alert# = High	OK	
Alert# = Low	Power Alert to system	
	MIN	**MAX**
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isink=50 mA		5.25 V
Sink current, Alert# = low		4 mA
Sink current, Alert# = high		50 µA
Alert# rise and fall time		100 µs

9.12 Power Supply Management (PSM) Interface

STATUS
Optional

The power supply shall provide information over a server management bus (PSM Bus) to the system. Two pins have been reserved on the connector to provide this information. One pin is the Serial Clock (PSM Clock). The second pin is used for Serial Data (PSM Data). Both pins are bi-directional and are used to form a serial bus. The device in the power supply shall be located at an address shown in Table 31. The PSM circuits inside the power supply shall be powered from an internal 5 V bias voltage derived from the 12 VSB output on the system side of the or'ing device. The PSM circuits should be referenced to 12 VSB Return. No pull-up resistors shall be on SCL or SDA inside the power supply. These pull-up resistors should be located external to the power supply. The EEPROM for FRU data in the power supply shall be hard wired to allow writing data to the device.

Table 31: FRU Addressing

A2	A1	A0	Address	A2	A1	A0	Address
Low	Low	Low	0xA0	High	Low	Low	0xA8
Low	Low	High	0xA2	High	Low	High	0xAA
Low	High	Low	0xA4	High	High	Low	0xAC
Low	High	High	0xA6	High	High	High	0xAE[1]

1. This is the default EEPROM address if A0, A1, and A2 are left open.

NOTE

These PSM requirements (excluding the hours in operation clock) may be accomplished using an Analog Devices power supply monitoring ASIC (ADI part number ADM1040) inside the power supply.

The PSM Interface shall provide current, output voltage, fan speed, and temperature measurement information. It shall also provide system control of the power supply fan. The PSM Interface may optionally provide input voltage measurement and a power supply hours in operation clock. The PSM Interface also shall provide the FRU data communication as describe in IPMI.

The PSM device inside the power supply shall provide a number of internal registers. These include:

Register:	Function:
Sensor Registers:	The monitoring results for voltage, current, fan speed, and temperature are contained in these registers.
Limit Registers:	The limits or threshold values that will cause the Alert signal to assert and the Alert register to assert when a Sensor register exceeds its associated Limit register.
EEPROM:	Write protectable non-volatile memory for storing the power

9.12.1 Monitoring Cycle Time

STATUS
Optional

When the power supply is powered on, the PSM device shall cycle through each voltage, current, fan period, and temperature measurement in sequence, and continuously loop through this sequence. It shall take no more than 200 ms to cycle once through all measurements and update their respective registers. The measured values shall be stored in Sensor Registers.

Each Sensor Register value shall be compared to values stored in the Limit Registers. When the Sensor Register value exceeds its associated Limit Register, the PSM device inside the power supply shall assert the PSAlert# signal and the PSM Alert bit. The Alert bit shall be located at Bit 7 of register 0Eh.

Some averaging shall be performed on each measurement input. Refer to sensor details for averaging method. This averaging time is included in the 200 ms maximum cycle time.

9.12.2 Current Monitoring

STATUS
Optional

The PSM device inside the power supply shall measure the 48 V and 12 VSB output currents. The register Sensor Register locations are reserve for storing these current measurements. They shall be updated every measurement cycle. The values in the Sensor Registers shall be compared to their associated Limit Registers. If the value in the Sensor Register exceeds the Limit Register, then the PSAlert# signal and PSAlert Bit shall be asserted.

There are also Sensor Register locations for storing and saving the maximum current measured in each of the current Sensor Registers. If a current Sensor Register exceeds the value of the associated maximum current Sensor Register, then the value in the current Sensor Register shall be saved into the maximum current Sensor Register. The Maximum Current Sensor Register shall be reset to 00 when the power supply powered down with PSON# or loss of AC. The system shall also be able to reset the Maximum Current Sensor Register by writing a 00 to the register.

Description	MIN	NOM	MAX
Sensor Register Location; 48 V current [1]		1Dh	
Sensor Register Location; 12 VSB current [1]		1Ch	
Register value range; 48 V current[3]	0 A = 00h		Max Amps = C0h
Register value range; 12 VSB current[3]	0 A = 00h		Max Amps = C0h
Sensor Register Location; 48 V max current [4]		20h	
Sensor Register Location; 12 VSB max current [4]		1Fh	
Averaging period [2]	8 ms	14 ms	20 ms
Limit Register Location; 48 V current [1]		6Ch	
Limit Register Location; 12 VSB current [1]		6Bh	
Limit Register Value; 48 V current	100% of max output current		110% of max output current
Limit Register Value; 12 VSB current	100% of max output current		110% of max output current

1. Each Sensor Register uses bits 0-7 for the current measurement value or limit value.
2. The measured current shall be averaged over this period to eliminate high frequency elements.
3. The Sensor Register value shall be linear from 0A (register value = 00h) to maximum output current (register value = C0h). The maximum output current corresponds to 75% of the maximum register value (register value = FFh). The 25% left at the high end of the register value allows for peak current measurements, which shall continue to ramp linearly from maximum output current value C0h.
4. The maximum current Sensor Register shall store the highest value seen in its associated current Sensor Register. This register can be reset to 00h to start a new series of maximum current measurements.

9.12.3 Output Voltage Monitoring

STATUS
Optional

The PSM device inside the power supply shall measure the 48 V and 12 VSB output voltages on the anode of the output or'ing device. Two register locations (Sensor Registers) are reserve for storing these voltage measurements. They shall be updated every measurement cycle. The values in the Sensor Registers storing the voltage information shall be compared to their associated Limit Registers. If the value in the Sensor Register exceeds the Limit Register than the Alert# signal and Alert Bit shall be asserted.

Description	MIN	NOM	MAX
Sensor Register Location; 48 V voltage [1]		15h	
Sensor Register Location; 12 VSB voltage [1]		14h	
Register value range; 48 V voltage	0 V = 00h	48.0 V = 96h	81.92 V = FFh
Register value range; 12 VSB voltage	0 V = 00h	12.0 V = 96h	20.48 V = FFh
Averaging period [2]	8 ms	14 ms	20 ms
Limit Register Locations; 48 V voltage [1]	67h		62h
Limit Register Location; 12 VSB voltage [1]	66h		61h
Limit Register Value; 48 V voltage	43.20 V = 87h		52.80 V = A5h
Limit Register Value; 12 V voltage	11.16 V = 8Bh		12.84 V = A1h

1. Each Sensor Register uses bits 0-7 for the current measurement value or limit value.
2. The measured voltage shall be averaged over this period to eliminate high frequency elements.
3. The Sensor Register value shall be linear from 0 V (register value = 00h) to max voltage (register value = FFh).

9.12.4 Temperature Monitoring

STATUS
Optional

A "hotspot" within the power supply shall be measured and the temperature stored within the PSM device. The data shall be stored in 8-bit twos-complement format. The temperature Sensor Register shall be compared against the Limit Registers for temperature. If the Limit Register value is exceeded the PSAlert# signal and the PSAlert bit shall be asserted.

Description	MIN	NOM	MAX
Sensor Register Location; Temp [1]		11h	
Register Value Range; Temp [2]	-55 °C = C9h		+125 °C = 7Dh
Limit Register Location; Temp [1]	75h		74h
Limit Register Value; Temp	Determined by Manufacturer [3]		Determined by Manufacturer [3]

1. The Sensor Register uses bits 0-7 for the temperature measurement value or limit value.
2. The data is stored in 8 bit two-complement format. See table below for description.

3. The High Limit Register value shall set 10 to 5 °C lower than the shutdown temperature of the power supply.

Temperature (°C)	Binary (O/P)	Hex (O/P)
-55	1100 1001	C9
-25	1110 0111	E7
-1	1111 1111	FF
0	0000 0000	00
+1	0000 0001	01
+25	0001 1001	19
+125	0111 1101	7D

9.12.5 Fan Speed Measurement

STATUS
Optional

Both fans in the power supply shall be measured via the PSM device. When either Sensor Register exceeds its associated Limit Register the PSAlert# signal and PSAlert bit shall be asserted. The Sensor Registers store the period of the fan revolutions. The higher the value in the register the slower the fan is operating. To accommodate fans of different speeds or pulses/revolution a divisor of 1, 2, 4, or 8 shall be set before the measurement. The divisors are located in register 6Eh.

Description	MIN	NOM	MAX
Sensor Register Location; Fan1 [1]		18h	
Sensor Register Location; Fan2 [1]		19h	
Register Value Range; 6Eh = 00	5280 RPM = FFh	8800 RPM = 99h	
Register Value Range; 6Eh = 01	2640 RPM = FFh	4400 RPM = 99h	
Register Value Range; 6Eh = 10	1320 RPM = FFh	2200 RPM = 99h	
Register Value Range; 6Eh = 11	660 RPM = FFh	1100 RPM = 99h	
Limit Register Location; Fan1 [1]	6Fh		
Limit Register Location; Fan2 [1]	70h		
Limit Register Value; Fan1,Fan2 [2]	70% of nominal fan speed.		
Fan Divisor Location; Fan1		6Eh (bit 1-0)	
Fan Divisor Location; Fan2		6Eh (bit 3-2)	

1. The Sensor Register uses bits 0-7 for the fan period counter.
2. The High Limit Register value shall set 70% lower than the nominal low fan speed. The power supply manufacturer shall determine this limit. The power supply shall not shutdown before the limit register is exceeded.
3. The fan period counter, which reflects the fan RPM, shall be linear from nominal to minimum periods.

9.12.6 Fan Speed Control

STATUS
Optional

The power supply shall have variable speed fans. The PSM interface shall be able to request a different fan speed. If the power supply requires a higher fan speed for cooling, the fan shall be set to the higher fan speed.

Description	MIN	NOM	MAX
Sensor Register Location		78h	
Register Value Range	00h = Fan Off	BFh = low fan speed	FFh = high fan speed

9.12.7 Hours in Operation Clock

STATUS
Optional

The PSM device in the power supply shall have three 8 bit registers to count the hours the power supply has been operating with PSON# asserted. The hours of operation shall be stored in non-volatile memory when AC is removed from the power supply. The accuracy of the counter shall not gain or loose more than 15 days over a 300-day period. The data saved in the registers and the non-volatile memory shall be write protected.

Description	MIN	NOM	MAX
Sensor Register Location		TBD	
Register Value Range	00h = 0 hours		FFFFFh = 2^{24} hours

9.12.8 Input Voltage Monitoring

STATUS
Optional

The PSM device inside the power supply shall measure the AC input voltage. One register location (Sensor Register) is reserve for storing this voltage measurement. It shall be updated every measurement cycle. The value in the Sensor Register shall be compared to its Limit Register. If the value in the Sensor Register exceeds the Limit Register than the PSAlert# signal and PSAlert Bit shall be asserted.

Description	MIN	NOM	MAX
Sensor Register Location; AC input voltage [1]		17h	
Register value range; AC input voltage[3]	0 V = 00h	110 VAC = 37h 220 VAC = 6Eh	512 V = FFh
Accuracy; THD = 0%	+/-5%	5.0 V = 7Ch	10.24 V = FFh
Accuracy; THD = 10%	+/-10%	12.0 V = 96h	20.48 V = FFh
Averaging period [2]	200 ms	350 ms	500 ms
Limit Register Locations; AC input voltage [1]	69h		64h
Limit Register Values; AC input voltage	70 VAC = 23h		300 VAC = 96h

1. The Sensor Register uses bits 0-7 for the voltage measurement value or limit value.
2. The measured voltage shall be averaged over this period to eliminate high frequency elements.
3. The Sensor Register value shall be linear from 0 V (register value = 00h) to max voltage (register value = FFh).

9.12.9 PSM Interface

STATUS
Optional

Refer to www.smbus.org under the High Power Version of the SMBus Specification for details regarding protocol, timing, and other requirements for the PSM interface.

The PSM interface of the power supply must not load down the system PSM interface if no power is applied to the power supply. This requirement allows a Power supply to be disconnected from the AC supply while still installed in a system.

9.12.10PSM Protocols

STATUS
Optional

The SMbus specification defines several protocols for different types of read and write operations. The ones used in the PSM device are discussed below. The following abbreviations are used in the diagrams:

S - START
P - STOP
R - READ

W - WRITE
A - ACKNOWLEDGE
/A - NO ACKNOWLEDGE

9.12.11PSM Write Operations

STATUS
Optional

The PSM interface uses the following transactions.

Send Byte
In this operation the master device in the system sends a single command byte to a slave device in the power supply, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a STOP condition on SDA and the transaction ends.

In the PSM device, the SMBus send byte protocol is used to write a register address to the SMBus interface for a subsequent single byte read from the same address or block read or write starting at that address. This is illustrated below:

1	2		3	4	5	6
S	Slave Address	W	A	Reg Address (00h to 7Fh)	A	P

If it is required to read data from the PSM device immediately after setting up the address, the master can assert a repeat start condition immediately after the final ACK and carry out a single byte read, block read or block write operation, without asserting an intermediate stop condition.

Write Byte/Word
In this operation the master device in the system sends a command byte and one or two data bytes to the slave device in the power supply, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master sends a data byte (or may assert STOP at this point).
9. The slave asserts ACK on SDA.
10. The master asserts a STOP condition on SDA to end the transaction.

In the PSM device, the write byte/word protocol is used for three purposes. The PSM device knows how to respond by the value of the command byte.

Write a single byte of data to a Register. In this case the command byte is the Register address from 00h to 0x7Fh and the (only) data byte is the actual data. This is illustrated below:

1	2		3	4	5	6	7	8
S	Slave Address	W	A	Reg Address (00h to 7Fh)	A	Data Byte	A	P

9.12.12PSM Read Operations

STATUS
Optional

The PSM device uses the following SMBus read protocols.

Receive Byte
In this operation the master device receives a single byte from a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a STOP condition on SDA and the transaction ends.

In the PSM device, the receive byte protocol is used to read a single byte of data from a Register or an EEPROM location, whose address has previously been set by a send byte or write byte/word operation. The packet format is illustrated below.

1	2		3	4	5	6
S	Slave Address	R	A	Data Byte	/A	S

Bit 2 of the register 04h should be set prior to sending the SMBUS packet illustrated above.

Block Read

In this operation the master device reads a block of data from a slave device. The start address for a block read must previously have been set. This is done by a Send Byte operation to set a RAM address or a Write Byte/Word operation to set an EEPROM address. The block read operation itself consists of a Send Byte operation that sends a block read command to the slave, immediately followed by a repeat start and a read operation that reads out multiple data bytes, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code that tells the slave device to expect a block read. The PSM device command code for a block read is A1h (10100001).
5. The slave asserts ACK on SDA.
6. The master asserts a repeat start condition on SDA.
7. The master sends the 7-bit slave address followed by the read bit (high).
8. The slave asserts ACK on SDA.
9. The master receives a byte count data byte that tells it how many data bytes will be received. The SMBus specification allows a maximum of 32 data bytes to be received in a block read.
10. The master asserts ACK on SDA.
11. The master receives N data bytes.
12. The master asserts ACK on SDA after each data byte.
13. The slave does not acknowledge after the Nth data byte.
14. The master asserts a STOP condition on SDA to end the transaction.

S	Slave Address	W	A	Command A1h (Block Read)	A	S	Slave Address	R	A	Byte Count	A	Data Byte 1	A	

		13	14
	Data Byte N	/A	P

Bit 2 of the register 04h should be set prior to sending the SMBUS packet illustrated above.

9.12.13Reset

STATUS
Optional

The values for the limit registers shall be stored in non-volatile memory and automatically loaded into the limit register location at power on. Bit 1 of register 04h is set to 1 when the limit registers have completed loading from the non-volatile memory. The PSM device shall be able to do a soft reset by writing to bit 0 of the Reset Register (05h). This bit shall automatically clear itself after being set. A soft reset performs a similar reset to the Power On Reset, except that the limit registers are not reset, also the limit registers are not updated from the EEPROM. A soft reset could be viewed as an internal reset of the state machine and gives the ability to see if conversions are still occurring as the value registers will be updated from a zero value. Registers that are reset by each type of reset are shown below:

Reg Address	Reg Name	Soft Reset	Power On Reset
0Eh, 0Fh	Alert Interrupt Status Registers	X	X

10h-21h	Sensor Registers	X	X
60h-6Ch	Limit Registers		X

9.12.14Interrupt Status Registers

STATUS
Optional

The power supply PSM device shall contain a pair of Alert interrupt status registers and one Shutdown interrupt status register. These registers are used to reflect the state of all of the possible error conditions that the power supply monitors. When an error occurs during the conversion cycle, its corresponding bit is set in its respective interrupt status register. The status register bits are updated continuously through each monitoring cycle. Reading a status register does not clear its contents.

Reg Address	Reg Name	Description	Value = 1	Value = 0
0Eh (bit 0)	Reserved			
0Eh (bit 1)	Fan1 Fail	Fan1 in the power supply is operating less than 70% of the low fan speed.	Fan Operating Slow	OK
0Eh (bit 2)	Reserved			
0Eh (bit 3)	Reserved			
0Eh (bit 4)	Fan2 Fail	Fan2 in the power supply is operating less than 70% of the low fan speed.	Fan Operating Slow	OK
0Eh (bit 5)	Fail	The power supply has failed.	Fail	OK
0Eh (bit 6)	Reserved			
0Eh (bit 7)	PSAlert	Combined indicator of all the interrupt bits.	Alert	OK
0Fh (bit 0)	Reserved			
0Fh (bit 1)	Reserved			
0Fh (bit 2)	Reserved			
0Fh (bit 3)	12 V Fail	The voltage measured on 12 V has exceeded one of its limit registers.	Fail	OK
0Fh (bit 4)	5 V Fail	The voltage measured on 5 V has exceeded one of its limit registers.	Fail	OK
0Fh (bit 5)	3.3 V Fail	The voltage measured on 3.3 V has exceeded one of its limit registers.	Fail	OK
0Fh (bit 6)	5 VSB Fail	The voltage measured on 5 VSB has exceeded one of its limit registers.	Fail	OK
0Fh (bit 7)	AC Input Fail	The voltage measured on the AC input has exceeded one of its limit registers.	Fail	OK

10 Field Replacement Unit (FRU) Signals

STATUS
Required

Two pins will be allocated for the FRU information on the power supply connector. One pin is the Serial Clock (SCL). The second pin is used for Serial Data (SDA). Both pins are bi-directional and are used to form a serial bus. The FRU circuits inside the power supply must be powered off of 5 VSB output and grounded to ReturnS (remote sense return). The Write Control (or Write protect) pin should be tied to ReturnS inside the power supply so that information can be written to the EEPROM.

10.1 FRU Data

STATUS
Required

FRU data shall be stored starting in address location 8000h through 80FFh. The FRU data format shall be compliant with the IPMI specifications. The current version of these specifications are available at http:\\developer.intel.com\design\servers\ipmi\spec.htm.

10.2 FRU Data Format

STATUS
Required

The information to be contained in the FRU device is shown in the following table.

Area Type	Description
Common Header	As defined by the FRU document
Internal Use Area	Not required, do not reserve
Chassis Info Area	Not applicable, do not reserve
Board Info Area	Not applicable, do not reserve
Product Info Area	As defined by the IPMI FRU document.

Product information shall be defined as follows:

Field Name	Field Description
Manufacturer Name	{Formal name of manufacturer}
Product Name	{Manufacturer's model number}
Product part/model number	Customer part number
Product Version	Customer current revision
Product Serial Number	{Defined at time of manufacture}

Asset Tag	{Not used, code is zero length byte}
FRU File ID	{Not required}
PAD Bytes	{Added as necessary to allow for 8-byte offset to next area}
MultiRecord Area	As defined by the IPMI FRU document. The following record types shall be used on this power supply: Power Supply Information (Record Type 0x00) DC Output (Record Type 0x01) No other record types are required for the power supply.

MultiRecord information shall be defined as follows:

Field Name (PS Info)	Field Information Definition
Overall Capacity (W)	1200 {replace with other power levels if different}
Peak VA	1450 {replace with other power levels if different}
Inrush current (A)	35
Inrush interval (ms)	5
Low end input voltage range 1	90
High end input voltage range 1	140
Low end input voltage range 2	180
High end input voltage range 2	264
A/C dropout tol. (msec)	20
Binary flags	Set for: Hot Swap support, Autoswitch, and PFC
Peak Wattage	Set for: 10 s, 1320 W {replace with other power levels if different}
Combined wattage	No combine wattage. 00h value
Predictive fail tach support	Lower fan revolutions per second threshold to indicate a predictive failure. 01h to FFh value.
Field Name (Output)	Field Description: Two outputs are to be defined from #1 to #2, as follows: +48 V and +12 VSB.
Output Information	Set for: Standby on +12 VSB, No Standby on all others.
All other output fields	Format per IPMI specification, using parameters in the DPS specification.

10.3 LED Indicators

STATUS	
PWR, FAIL	**Required**
PFAIL	**Optional**

A green POWER LED (PWR) is required to indicate that AC is applied to the PSU and standby voltages are available when blinking. This same LED should go solid to indicate that all the power outputs are available. An amber Power Supply Fail LED (FAIL) is required to indicate that the Power Supply has failed therefore a replacement of the unit is necessary. An amber Predictive Fail LED (PFAIL) is recommended to indicate that the power supply is about to fail in the near future due to a poorly performing fan. This LED should be blinking to indicate the predictive failure condition and should be latched into blinking state once the condition has occurred. This latch can be cleared by toggling the PSON signal or by an AC power interruption of greater than 1 second. Refer to Table 32 for conditions of the LED's.

Table 32: LED Indicators

	Power Supply LED's		
Power Supply Condition	**PWR (Required) (green)**	**PFAIL (Recommended) (AMBER)**	**FAIL (Required) (AMBER)**
No AC power to all PSU	OFF	OFF	OFF
No AC power to this PSU only	OFF	OFF	ON
AC present / Standby Output On	Blinking	OFF	OFF
Power supply DC outputs ON and OK	ON	OFF	OFF
Power supply failure	OFF	OFF	ON
Current limit on 48 VDC output	ON	OFF	Blinking
Predictive failure	ON	Blinking/Latched	OFF

The LED's shall be visible on the power supply surface that is opposite to the docking end. The LED location shall meet ESD requirements. LED's shall be securely mounted in such a way that incidental pressure on the LED will not cause it to become displaced.

11 Markings and Labels

11.1 LED Labeling

STATUS
Recommended

The Power LED (green), the Predictive Failure LED (amber), and the Power Supply Failure LED (amber) shall be marked or labeled near the LED's with the following markings.

Power

Fail

Predictive Failure

12 MTBF

The power supply shall have a minimum MTBF at continuous operation of 1) 100,000 hours at 100% load and 50 °C, as calculated by Bellcore RPP, or 2) 200,000 hours demonstrated at 100% load and 50 °C.

13 Agency Requirements

The power supply must comply with all regulatory requirements for its intended geographical market. Depending on the chosen market, regulatory requirements may vary. Although a power supply can be designed for worldwide compliance, there may be cost factors that drive different versions of supplies for different geographically targeted markets. All outputs shall meet SELV requirements.

This specification requires that the power supply meet all regulatory requirements for the intended market at the time of manufacturing. Typically this includes:

- UL
- CSA
- A Nordic CENELEC
- TUV
- VDE
- CISPR Class B
- FCC Class B

The power supply, when installed in the system, shall meet immunity requirements specified in *EN55024*. Specific tests are to be *IEC 801-2, IEC 801-3, IEC 801-4*, and *IEC801-5*, each at level 3. The power supply must maintain normal performance within specified limits. This testing must be completed by the system EMI engineer. Conformance must be designated with the European Union CE Marking.