Peregrine Semiconductor

Advance Information

PE43702

50 Ω RF Digital Attenuator
7-bit, 31.75 dB, DC-4.0 GHz

Product Description

The PE43702 is a HaRP™-enhanced, high linearity, 7-bit RF Digital Step Attenuator (DSA) covering a 31.75 dB attenuation range in 0.25 dB steps. This Peregrine 50Ω RF DSA provides both a serial and parallel CMOS control interface. It maintains high attenuation accuracy over frequency and temperature and exhibits very low insertion loss and low power consumption. This next generation Peregrine DSA is available in a 4x4 mm 24 lead QFN footprint.

The PE43702 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- HaRP™-enhanced UltraCMOS™ device
- Fast switch settling time
- High Linearity: Typical +57 dBm IP3
  - Excellent low-frequency performance
- 3.3 V or 5.0 V Power Supply Voltage
- Best in class 2000 V HBM ESD tolerance
- Attenuation: 0.25 dB steps to 31.75-dB
- Programming Modes:
  - Direct Parallel
  - Latched Parallel
  - Serial
- CMOS Compatible
- No DC blocking capacitors required
- High-α state @ power-up (PUP)
- Packaged in a 24-lead 4x4x0.85 mm QFN

Figure 1. Package Photo
24-lead 4x4x0.85 mm QFN Package

Figure 2. Functional Schematic Diagram

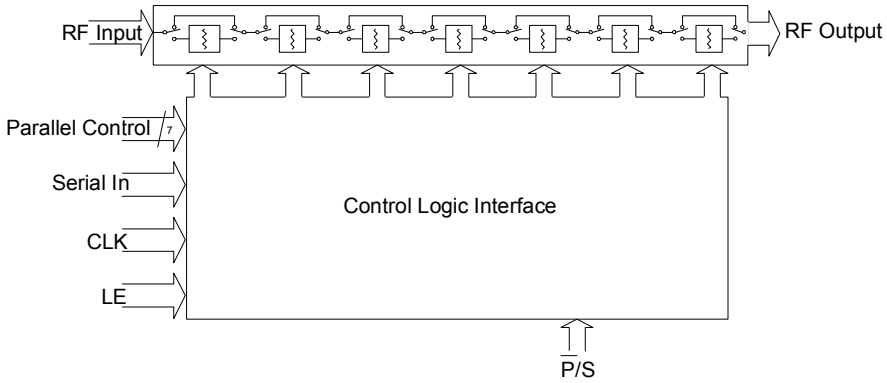

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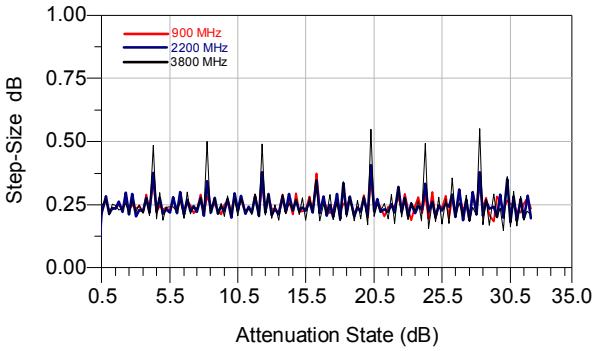
Table 1. Electrical Specifications @ +25°C, V_{DD} = 3.3 V or 5.0 V

Parameter	Test Conditions	Frequency	Typical	Units
Frequency Range			DC – 4000	MHz
Attenuation Range	0.25-dB Step	DC – 4000 MHz	0 – 31.75	dB
Insertion Loss		DC - 4000 MHz	1.7	dB
Attenuation Error	Any bit or bit combination	DC - 4000 MHz	≤ ±(0.2+2% of Att. Setting)	dB
Return Loss		DC -4000 MHz	18	dB
Relative Phase	All States	DC - 4000 MHz	< 55	deg
P1dB		20 MHz to 4000 MHz	+28	dBm
IIP3		20 MHz to 4000 MHz	+57	dBm
Switching Speed	10%-90%		650	ns
Idd			60	µA
Video Feed Through			10	mV
Settling Time	50% CTRL		10	µs

Performance Plots

Figure 3. Step-Size*



*Monotonicity is held so long as step size does not fall below on LSB

Figure 4. Attenuation

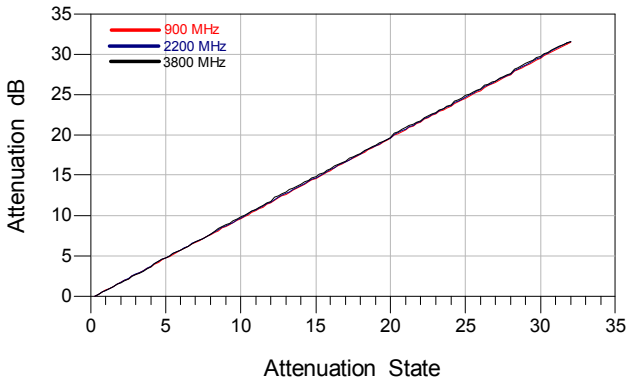


Figure 5. Major State Bit Error

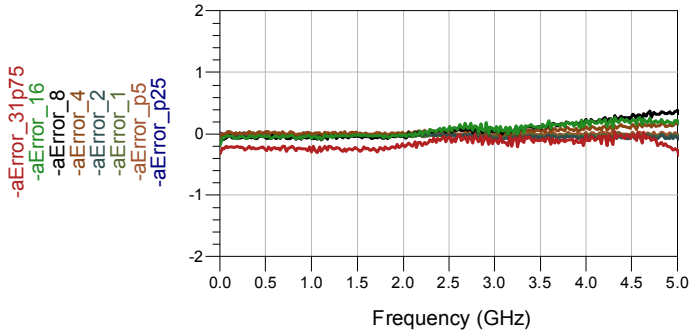
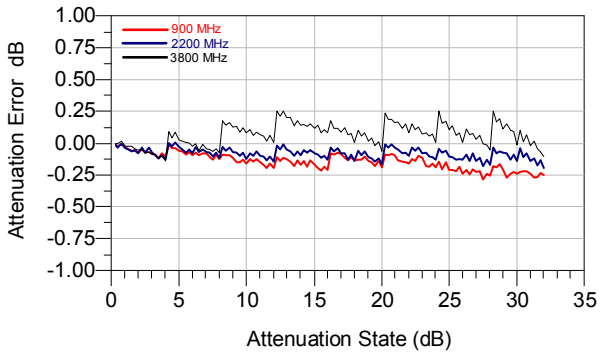


Figure 6. Attenuation Error



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Performance Plots

Figure 7. Return Loss: RF1, RF2

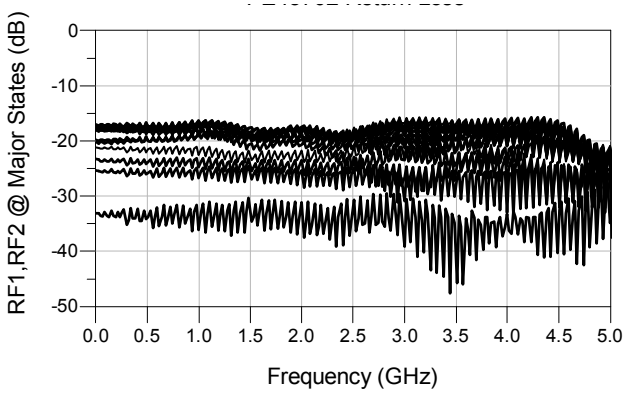

Figure 8. Relative Phase

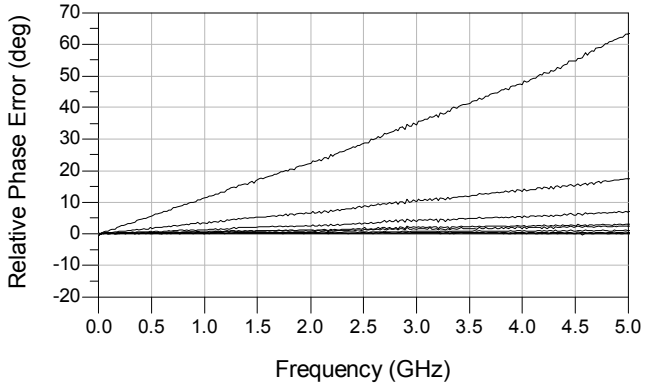

Figure 9. Insertion Loss

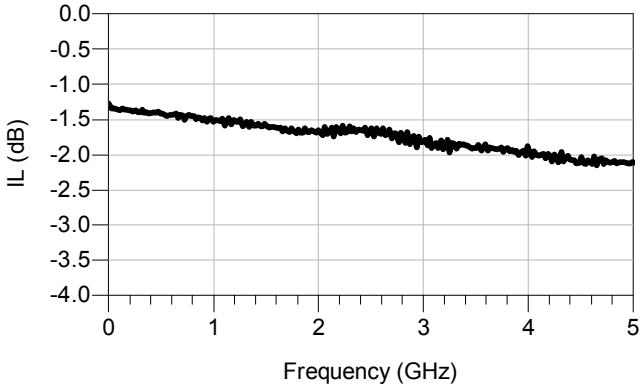

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Figure 10. Pin Configuration (Top View)

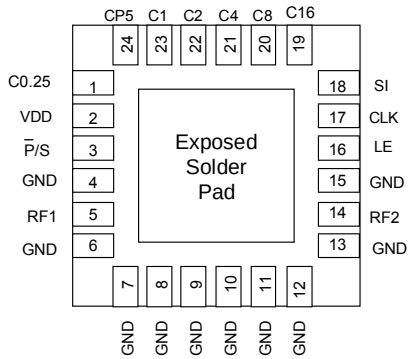

Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	C0.25	Attenuation control bit, 0.25 dB
2	V_{DD}	Power supply pin
3	$\overline{P}$/S	Serial/Parallel mode select
4	GND	Ground
5	RF1	RF1 port
6 - 13	GND	Ground
14	RF2	RF2 port
15	GND	Ground
16	LE	Latch Enable input
17	CLK	Serial interface clock input
18	SI	Serial Interface input
19	C16	Attenuation control bit, 16 dB
20	C8	Attenuation control bit, 8 dB
21	C4	Attenuation control bit, 4 dB
22	C2	Attenuation control bit, 2 dB
23	C1	Attenuation control bit, 1 dB
24	C0.5	Attenuation control bit, 0.5 dB
Paddle	GND	Ground for proper operation

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	3.0	3.3/5.0	5.5	V
I_{DD} Power Supply Current			100	µA
Digital Input High	2.6		5.5	V
P_{IN} Input power (50Ω)			+22	dBm
T_{OP} Operating temperature range	-40	25	85	°C
Digital Input Low	0		1	V
Digital Input Leakage			15	µA

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	6.0	V
V_I	Voltage on any Digital input	-0.3	5.8	V
T_{ST}	Storage temperature range	-65	150	°C
P_{IN}	Input power (50Ω)		+28	dBm
V_{ESD}	ESD voltage (Human Body Model)		2000	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Switching Frequency

The PE43702 has a maximum 25 kHz switching rate.

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Table 5. Control Voltage

State	Bias Condition
Low	0 to +1.0 Vdc at 2 μA (typ)
High	+2.6 to +5 Vdc at 10 μA (typ)

Table 6. Latch and Clock Specifications

Latch Enable	Shift Clock	Function
X	↑	Shift Register Clocked
↑	X	Contents of shift register transferred to attenuator core

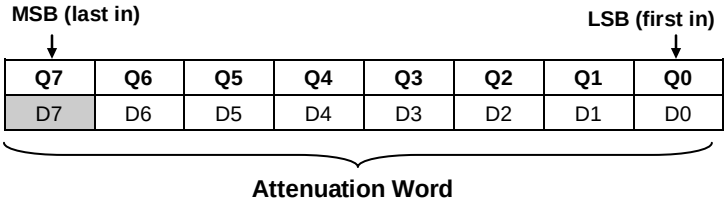
Table 7. Parallel Truth Table

Parallel Control Setting							Attenuation Setting RF1-RF2
D6	D5	D4	D3	D2	D1	D0	
L	L	L	L	L	L	L	Reference I.L.
L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	H	L	0.5 dB
L	L	L	L	H	L	L	1 dB
L	L	L	H	L	L	L	2 dB
L	L	H	L	L	L	L	4 dB
L	H	L	L	L	L	L	8 dB
H	L	L	L	L	L	L	16 dB
H	H	H	H	H	H	H	31.75 dB

Table 8. Serial Attenuation Word Truth Table

Attenuation Word								Attenuation Setting RF1-RF2
D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	
X	L	L	L	L	L	L	L	Reference I.L.
X	L	L	L	L	L	L	H	0.25 dB
X	L	L	L	L	L	H	L	0.5 dB
X	L	L	L	L	H	L	L	1 dB
X	L	L	L	H	L	L	L	2 dB
X	L	L	H	L	L	L	L	4 dB
X	L	H	L	L	L	L	L	8 dB
X	H	L	L	L	L	L	L	16 dB
X	H	H	H	H	H	H	H	31.75 dB

Table 9. Serial Register Map



Bits can either be set to logic high or logic low

Attenuation Word is derived directly from the attenuation value. For example, to program the 12.5 dB state:

Attenuation Word: Multiply by 4 and convert to binary → 4 * 12.5 dB → 50 → X0110010
Serial Input: X0110010

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Programming Options

Parallel/Serial Selection

Either a parallel or serial interface can be used to control the PE43702. The $\overline{P}$/S bit provides this selection, with $\overline{P}$/S=LOW selecting the parallel interface and $\overline{P}$/S=HIGH selecting the serial interface.

Parallel Mode Interface

The parallel interface consists of seven CMOS-compatible control lines that select the desired attenuation state, as shown in *Table 7*.

The parallel interface timing requirements are defined by *Fig. 12* (Parallel Interface Timing Diagram), *Table 11* (Parallel Interface AC Characteristics), and switching speed (*Table 1*).

For *latched*-parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (*per Fig. 12*) to latch new attenuation state into device.

For *direct* parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct Mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Serial Interface

The serial interface is a 8-bit serial-in, parallel-out shift register buffered by a transparent latch. The 8-bits make up the Attenuation Word that controls the DSA. *Fig. 11* illustrates a example timing diagram for programming a state.

The serial-interface is controlled using three CMOS-compatible signals: Serial-In (SI), Clock (CLK), and Latch Enable (LE). The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. Attenuation Word truth table is listed in *Table 8*. A programming example of the serial register is illustrated in *Table 9.* The serial timing diagram is illustrated in *Fig. 11.*

Power-up Control Settings

The PE43702 will always initialize to the maximum attenuation setting (31.75-dB) on power-up for both the serial and latched-parallel modes of operation and will remain in this setting until the user latches in the next programming word. In direct-parallel mode, the DSA can be preset to any state within the 31.75-dB range by pre-setting the parallel control pins prior to power-up. In this mode, there is a 400-µs delay between the time the DSA is powered-up to the time the desired state is set. During this power-up delay, the device attenuates to the maximum attenuation setting (31.75-dB) before defaulting to the user defined state. If the control pins are left floating in this mode during power-up, the device will default to the minimum attenuation setting (insertion loss state).

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Figure 11. Serial Timing Diagram

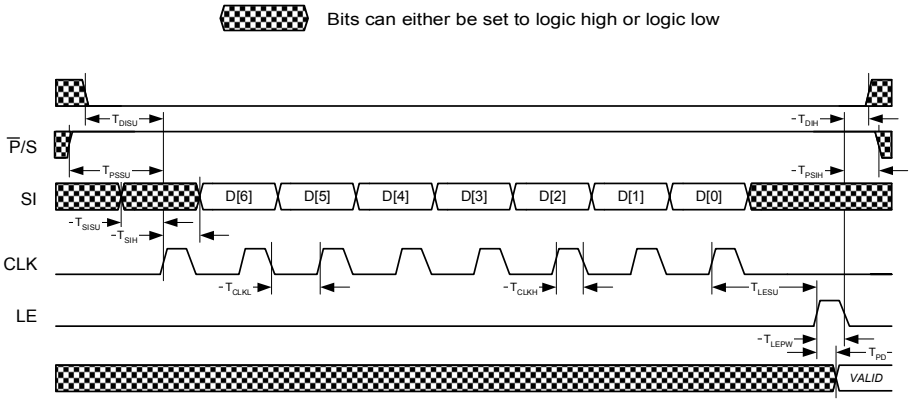

Figure 12. Latched-Parallel/Direct-Parallel Timing Diagram

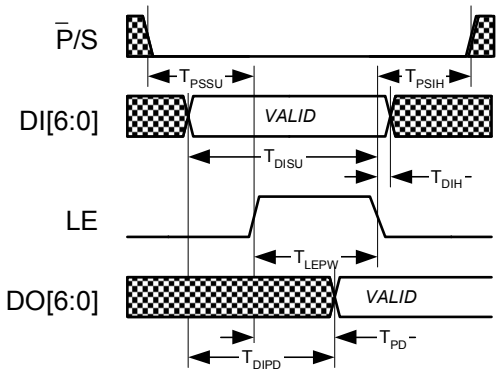

Table 10. Serial Interface AC Characteristics

V_{DD} = 3.3 or 5.0 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Min.	Max.	Unit
F_{CLK}	Serial clock frequency	-	10	MHz
T_{CLKH}	Serial clock HIGH time	30	-	ns
T_{CLKL}	Serial clock LOW time	30	-	ns
T_{LESU}	Last serial clock rising edge setup time to Latch Enable rising edge	10	-	ns
T_{LEPW}	Latch Enable minimum pulse width	30	-	ns
T_{SISU}	Serial data setup time	10	-	ns
T_{SIH}	Serial data hold time	10	-	ns
T_{DISU}	Parallel data setup time	100	-	ns
T_{DIH}	Parallel data hold time	100	-	ns
T_{ASU}	Address setup time	100	-	ns
T_{AIH}	Address hold time	100	-	ns
T_{PSSU}	Parallel/Serial setup time	100	-	ns
T_{PSIH}	Parallel/Serial hold time	100	-	ns
T_{PD}	Digital register delay (internal)	-	10	ns

Note: f_{Clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify fclk specification.

Table 11. Parallel and Direct Interface AC Characteristics

V_{DD} = 3.3 or 5.0 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
T_{LEPW}	Latch Enable minimum pulse width	30	-	ns
T_{DISU}	Parallel data setup time	100	-	ns
T_{DIH}	Parallel data hold time	100	-	ns
T_{PSSU}	Parallel/Serial setup time	100	-	ns
T_{PSIH}	Parallel/Serial hold time	100	-	ns
T_{PD}	Digital register delay (internal)	-	10	ns
T_{DIPD}	Digital register delay (internal, direct mode only)	-	5	ns

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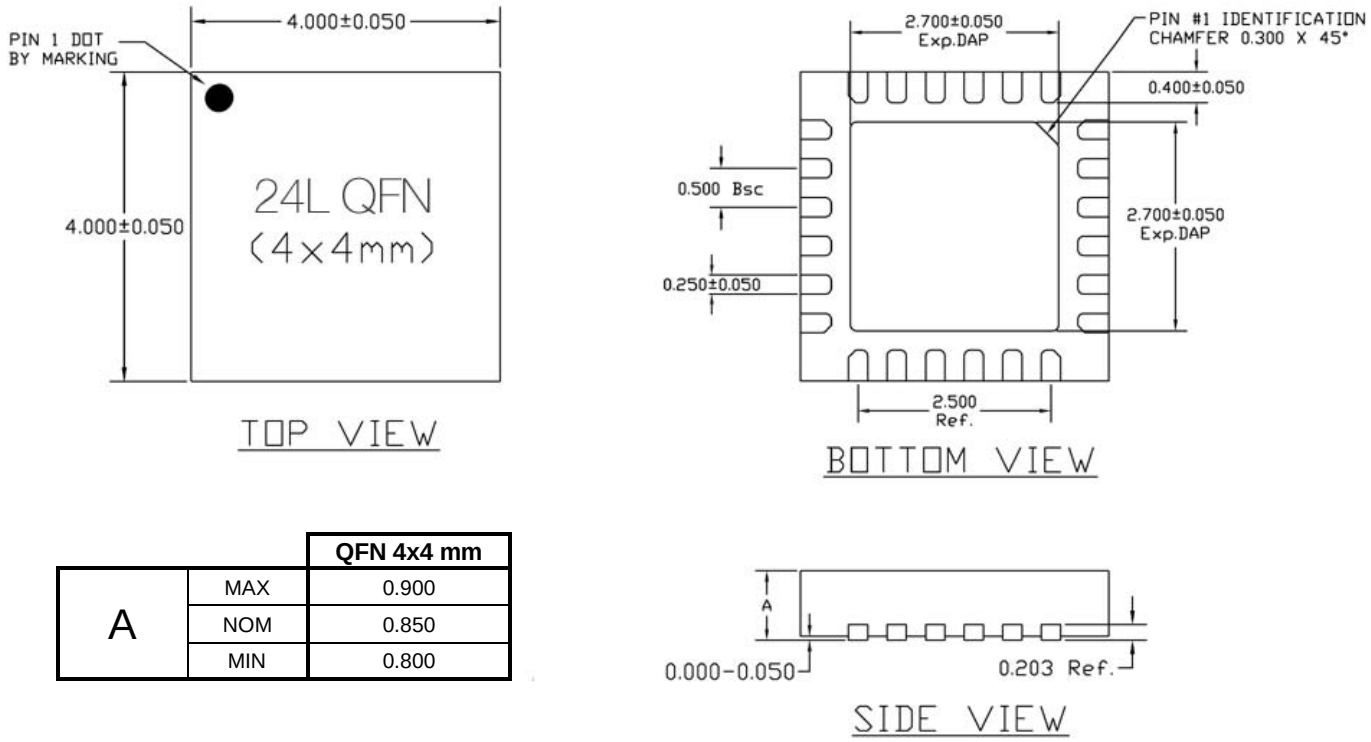
Figure 13. Package Drawing



		QFN 4x4 mm
A	MAX	0.900
	NOM	0.850
	MIN	0.800

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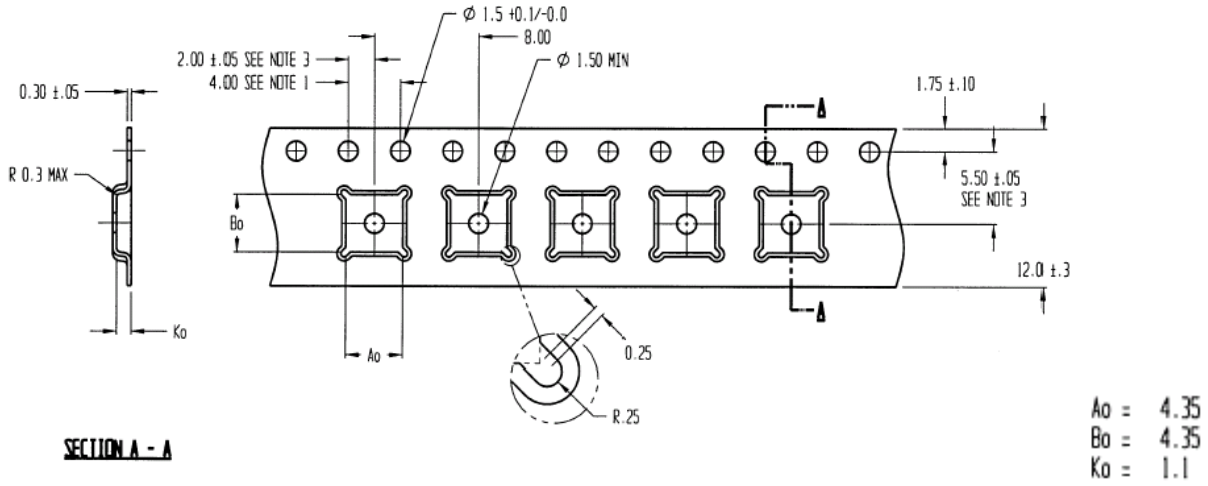
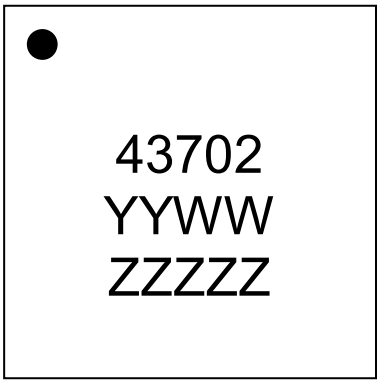
Figure 14. Tape and Reel Drawing



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Figure 15. Marking Specifications



YYWW = Date Code
ZZZZZ = Last five digits of Lot Number

Table 12. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
EK-43702-01	PE43702 -EK	PE43702-24QFN 4x4mm-EK	Evaluation Kit	1 / Box
PE43702 MLI	43702	PE43702G-24QFN 4x4mm-75A	Green 24-lead 4x4mm QFN	75 units / Tube
PE43702 MLI-Z	43702	PE43702G-24QFN 4x4mm-3000C	Green 24-lead 4x4mm QFN	3000 units / T&R

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Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

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