

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4041B **buffers** Quadruple true/complement buffer

Product specification
File under Integrated Circuits, IC04

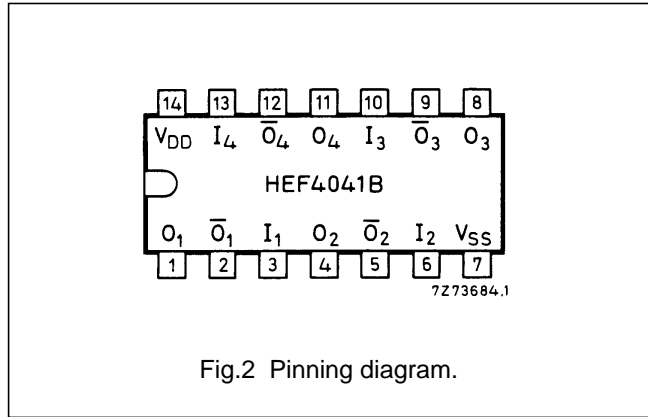
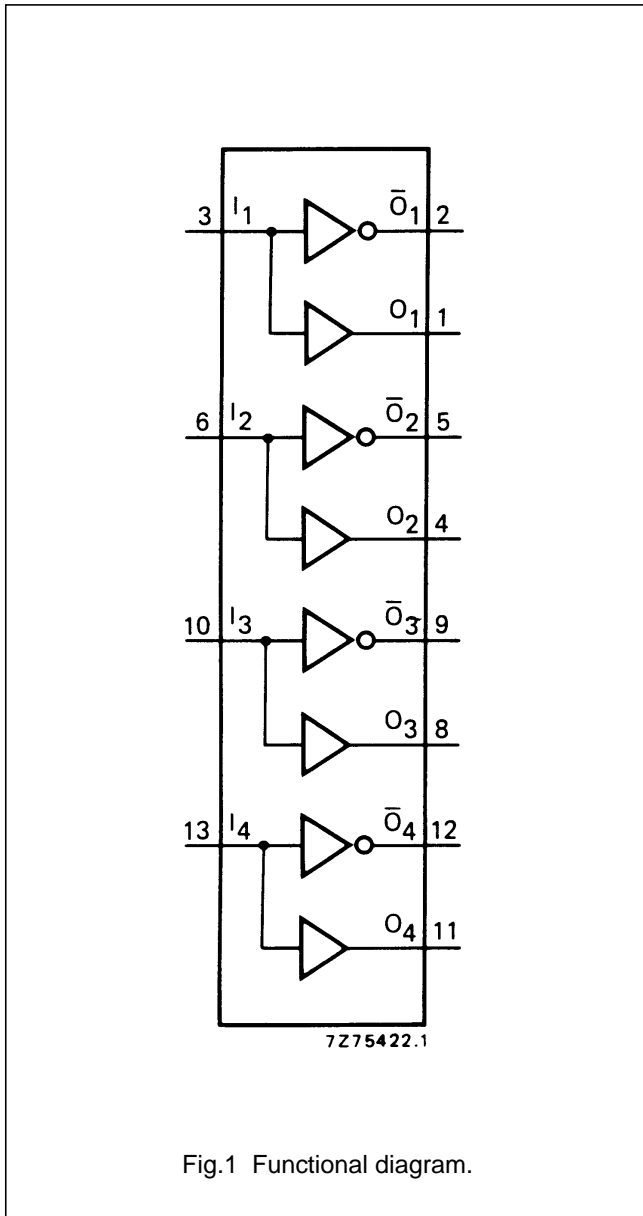
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Quadruple true/complement buffer

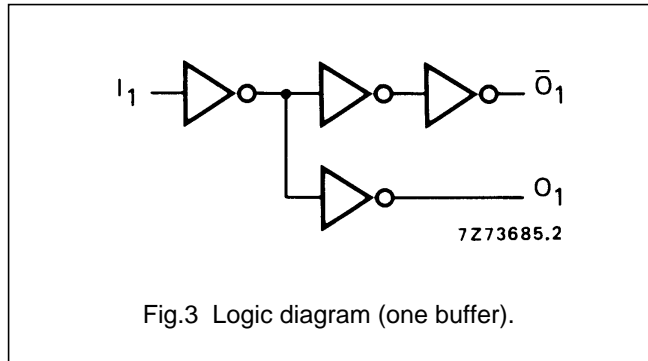
HEF4041B buffers

DESCRIPTION

The HEF4041B is a quadruple true/complement buffer which provides both an inverted active LOW output (\bar{O}) and a non-inverted active HIGH output (O) for each input (I). The buffers exhibit high current output capability suitable for driving TTL or high capacitive loads.



- HEF4041BP(N): 14-lead DIL; plastic (SOT27-1)
 - HEF4041BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
 - HEF4041BT(D): 14-lead SO; plastic (SOT108-1)
- (): Package Designator North America



APPLICATION INFORMATION

- Some examples of applications for the HEF4041B are:
- LOCMOS to DTL/TTL converter
 - High current sink and source driver

FAMILY DATA, I_{DD} LIMITS category BUFFERS

See Family Specifications

Quadruple true/complement buffer

HEF4041B buffers

DC CHARACTERISTICS

 $V_{SS} = 0\text{ V}; V_I = V_{SS}\text{ or }V_{DD}$

	V_{DD} V	V_{OH} V	V_{OL} V	SYMBOL	T_{amb} (°C)					
					-40		+25		+85	
					MIN.	MAX.	MIN.	TYP.	MIN.	MAX.
Output (source) current HIGH	5	4,6		$-I_{OH}$	1,6		1,3	2,6	1,0	mA
	10	9,5			4,5		3,6	7,0	2,7	mA
	15	13,5			16,0		14,0	30,0	10,0	mA
HIGH	5	2,5		$-I_{OH}$	5,0		4,0	8,0	3,0	mA
Output (sink) current LOW	4,75		0,4	I_{OL}	2,0		1,7	4,0	1,35	mA
	10		0,5		7,5		6,0	12,0	4,5	mA
	15		1,5		23,0		20,0	35,0	15,0	mA

AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}; T_{amb} = 25\text{ °C}; C_L = 50\text{ pF};$ input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA		
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}		30	65	ns	17 ns + (0,27 ns/pF) C_L	
	10		20	40	ns	14 ns + (0,11 ns/pF) C_L		
	15		15	30	ns	12 ns + (0,08 ns/pF) C_L		
	LOW to HIGH	5	t_{PLH}		30	55	ns	17 ns + (0,27 ns/pF) C_L
		10		15	30	ns	9 ns + (0,11 ns/pF) C_L	
		15		10	20	ns	7 ns + (0,08 ns/pF) C_L	
$I_n \rightarrow \bar{O}_n$ HIGH to LOW	5	t_{PHL}		35	75	ns	22 ns + (0,27 ns/pF) C_L	
	10		20	40	ns	14 ns + (0,11 ns/pF) C_L		
	15		15	30	ns	12 ns + (0,08 ns/pF) C_L		
	LOW to HIGH	5	t_{PLH}		35	75	ns	22 ns + (0,27 ns/pF) C_L
		10		20	40	ns	14 ns + (0,11 ns/pF) C_L	
		15		15	30	ns	12 ns + (0,08 ns/pF) C_L	
Output transition times $O_n \rightarrow \bar{O}_n$ HIGH to LOW	5	t_{THL}		25	50	ns	5 ns + (0,40 ns/pF) C_L	
	10		12	25	ns	2 ns + (0,21 ns/pF) C_L		
	15		8	20	ns	1 ns + (0,14 ns/pF) C_L		
	LOW to HIGH	5	t_{TLH}		25	45	ns	5 ns + (0,40 ns/pF) C_L
		10		12	25	ns	2 ns + (0,21 ns/pF) C_L	
		15		8	20	ns	1 ns + (0,14 ns/pF) C_L	

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	V_{DD} V	TYPICAL FORMULA FOR P (μ W)	
Dynamic power dissipation per package (P)	5 10 15	$3100 f_i + \sum(f_o C_L) \times V_{DD}^2$ $12\ 700 f_i + \sum(f_o C_L) \times V_{DD}^2$ $33\ 800 f_i + \sum(f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)

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