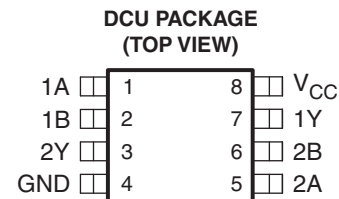


LOW-POWER DUAL 2-INPUT POSITIVE-NAND GATE

Check for Samples: [SN74AUP2G00-Q1](#)

FEATURES

- Qualified for Automotive Applications
- Low Static-Power Consumption ($I_{CC} = 1.7 \mu\text{A}$ Maximum)
- Low Dynamic-Power Consumption ($C_{pd} = 4.3 \text{ pF}$ Typ at 3.3 V)
- Low Input Capacitance ($C_i = 1.5 \text{ pF}$ Typical)
- Low Noise – Overshoot and Undershoot <math><10\%</math> of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 5.9 \text{ ns}$ Maximum at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see [Figure 1](#)). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in [Figure 2](#)).

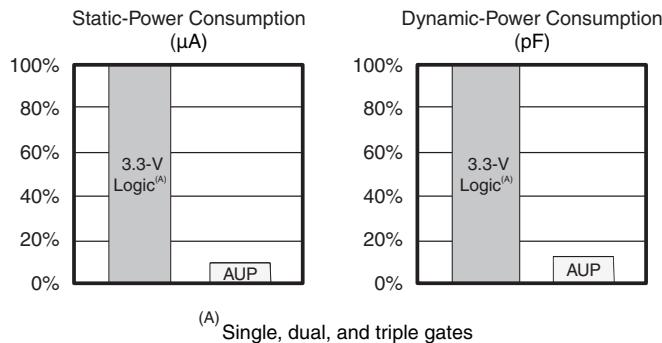
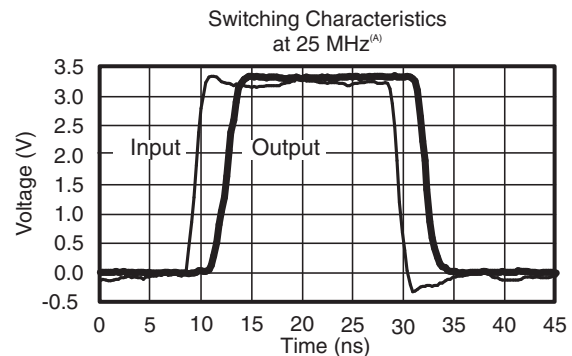

Figure 1. AUP – The Lowest-Power Family

^(A) SN74AUP2Gxx data at $C_L = 15 \text{ pF}$.

Figure 2. Excellent Signal Integrity

The SN74AUP2G00 performs the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

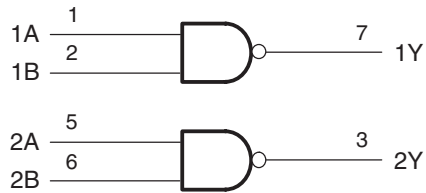
T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	VSSOP – DCU	Reel of 3000	SN74AUP2G00QDCURQ1	SBTQ

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE

INPUTS		OUTPUT Y
A	B	
L	L	H
L	X	H
X	L	H
H	H	L

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin number shown are for DCU and DQE packages.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V_{CC}	Supply voltage range	-0.5	4.6	V	
V_I	Input voltage range ⁽²⁾	-0.5	4.6	V	
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	4.6	V	
V_O	Output voltage range in the high or low state ⁽²⁾	-0.5	$V_{CC} + 0.5$	V	
I_{IK}	Input clamp current	$V_I < 0$	-50	mA	
I_{OK}	Output clamp current	$V_O < 0$	-50	mA	
I_O	Continuous output current		±20	mA	
	Continuous current through V_{CC} or GND		±50	mA	
θ_{JA}	Package thermal impedance, junction to free air	DCU package ⁽³⁾	220	°C/W	
T_{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

ESD PROTECTION

		MAX	UNIT	
ESD	Electrostatic discharge rating	Human-Body Model (HBM)	1000	V

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	0.8	3.6	V	
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}	V	
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	1.6		
		V _{CC} = 3 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0	V	
		V _{CC} = 1.1 V to 1.95 V	0.35 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 3 V to 3.6 V	0.9		
V _I	Input voltage	0	3.6	V	
V _O	Output voltage	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 0.8 V	–20	mA	
		V _{CC} = 1.1 V	–1.1		
		V _{CC} = 1.4 V	–1.7		
		V _{CC} = 1.65 V	–1.9		
		V _{CC} = 2.3 V	–3.1		
		V _{CC} = 3 V	–4		
I _{OL}	Low-level output current	V _{CC} = 0.8 V	20	mA	
		V _{CC} = 1.1 V	1.1		
		V _{CC} = 1.4 V	1.7		
		V _{CC} = 1.65 V	1.9		
		V _{CC} = 2.3 V	3.1		
		V _{CC} = 3 V	4		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 0.8 V to 3.6 V		200	ns/V
T _A	Operating free-air temperature	–40	125	°C	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = –20 μA	0.8 V to 3.6 V	V _{CC} – 0.1			V _{CC} – 0.1		V
	I _{OH} = –1.1 mA	1.1 V	0.75 × V _{CC}			0.7 × V _{CC}		
	I _{OH} = –1.7 mA	1.4 V	1.11			1.03		
	I _{OH} = –1.9 mA	1.65 V	1.32			1.3		
	I _{OH} = –2.3 mA	2.3 V	2.05			1.97		
	I _{OH} = –3.1 mA		1.9			1.85		
	I _{OH} = –2.7 mA	3 V	2.72			2.67		
	I _{OH} = –4 mA		2.6			2.55		
V _{OL}	I _{OL} = 20 μA	0.8 V to 3.6 V				0.1		V
	I _{OL} = 1.1 mA	1.1 V	0.3 × V _{CC}			0.3 × V _{CC}		
	I _{OL} = 1.7 mA	1.4 V	0.31			0.37		
	I _{OL} = 1.9 mA	1.65 V	0.31			0.35		
	I _{OL} = 2.3 mA	2.3 V	0.31			0.33		
	I _{OL} = 3.1 mA		0.44			0.45		
	I _{OL} = 2.7 mA	3 V	0.31			0.33		
	I _{OL} = 4 mA		0.44			0.45		
I _i	A or B input	V _i = GND to 3.6 V	0 V to 3.6 V			0.1	0.5	μA
I _{off}		V _i or V _O = 0 V to 3.6 V	0 V			0.2	1.3	μA
ΔI _{off}		V _i or V _O = 0 V to 3.6 V	0 V to 0.2 V			0.2	2	μA
I _{CC}		V _i = GND or (V _{CC} to 3.6 V), I _O = 0	0.8 V to 3.6 V			0.5	1.7	μA
ΔI _{CC}		V _i = V _{CC} – 0.6 V ⁽¹⁾ , I _O = 0	3.3 V			40	50	μA
C _i		V _i = V _{CC} or GND	0 V			1.5		pF
			3.6 V			1.5		
C _O		V _O = GND	0 V			3		pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND

SWITCHING CHARACTERISTICS⁽¹⁾

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			T _A = –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	Y	0.8 V	19.8					ns
			1.2 V ± 0.1 V	2.6	7.8	18.8	2.1	20.9	
			1.5 V ± 0.1 V	1.4	5.4	11.8	0.9	12.7	
			1.8 V ± 0.15 V	1	4.3	9	0.5	9.5	
			2.5 V ± 0.2 V	1	3	5.9	0.5	6.4	
			3.3 V ± 0.3 V	1	2.4	5.2	0.5	5.7	

(1) Specified by design. Not production tested.

SWITCHING CHARACTERISTICS⁽¹⁾

over recommended operating free-air temperature range, $C_L = 10$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V	23.1					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	1.5	8.9	21.1	1	22.1	
			$1.5\text{ V} \pm 0.1\text{ V}$	1	6.3	13.2	0.5	13.7	
			$1.8\text{ V} \pm 0.15\text{ V}$	1	5	10.1	0.5	10.6	
			$2.5\text{ V} \pm 0.2\text{ V}$	1	3.6	7.4	0.5	7.9	
			$3.3\text{ V} \pm 0.3\text{ V}$	1	2.9	5.5	0.5	6	

(1) Specified by design. Not production tested.

SWITCHING CHARACTERISTICS⁽¹⁾

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V	24.7					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	3.6	9.8	21.7	3.1	24.8	
			$1.5\text{ V} \pm 0.1\text{ V}$	2.3	4.6	14	1.8	15.8	
			$1.8\text{ V} \pm 0.15\text{ V}$	1.6	5.5	10.6	1.1	11.7	
			$2.5\text{ V} \pm 0.2\text{ V}$	1	4	7	0.5	7.5	
			$3.3\text{ V} \pm 0.3\text{ V}$	1	3.3	5.9	0.5	6.4	

(1) Specified by design. Not production tested.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

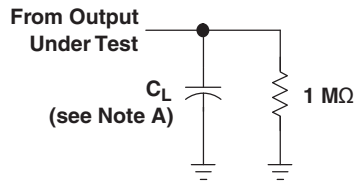
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V	31.8					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	4.9	12.6	26.3	4.4	29	
			$1.5\text{ V} \pm 0.1\text{ V}$	3.4	9	16.6	2.9	20	
			$1.8\text{ V} \pm 0.15\text{ V}$	2.5	7.3	12.9	2	15.7	
			$2.5\text{ V} \pm 0.2\text{ V}$	1.8	5.4	8.8	1.3	11.4	
			$3.3\text{ V} \pm 0.3\text{ V}$	1.5	4.5	7	1	9.5	

OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

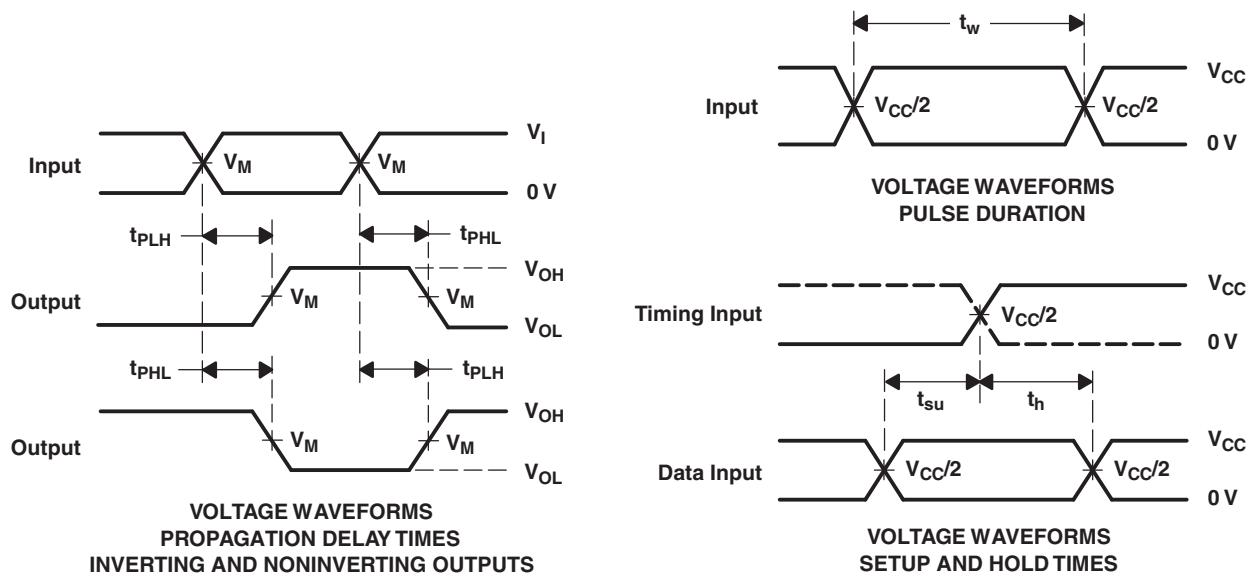
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$	0.8 V	4	pF
			$1.2\text{ V} \pm 0.1\text{ V}$	4	
			$1.5\text{ V} \pm 0.1\text{ V}$	4	
			$1.8\text{ V} \pm 0.15\text{ V}$	4	
			$2.5\text{ V} \pm 0.2\text{ V}$	4.1	
			$3.3\text{ V} \pm 0.3\text{ V}$	4.3	

**PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)**



LOAD CIRCUIT

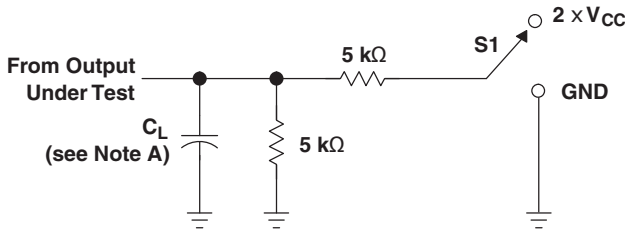
	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V} \pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, for propagation delays $t_r/t_f = 3\text{ ns}$, for setup and hold times and pulse width $t_r/t_f = 1.2\text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLH} and t_{PHL} are the same as t_{pd} .
- F. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)**



TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V} \pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r/t_f = 3\text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PLH} and t_{PHL} are the same as t_{pd} .
- G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP2G00QDCURQ1	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBTQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74AUP2G00-Q1 :

- Catalog: [SN74AUP2G00](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP2G00QDCURQ 1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

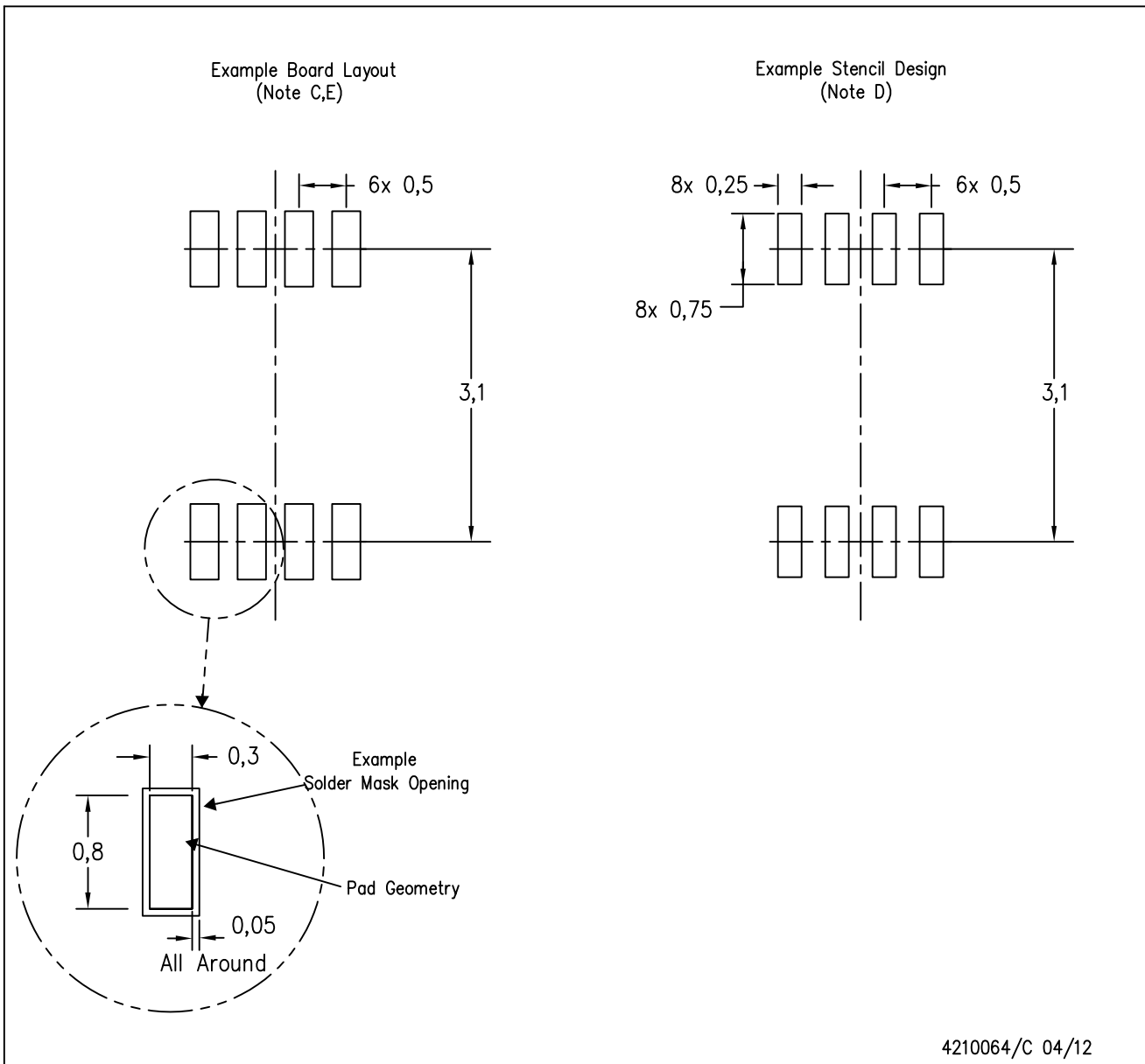


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP2G00QDCURQ1	VSSOP	DCU	8	3000	202.0	201.0	28.0

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



4210064/C 04/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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