Logic Doubling™ Reference designs and White Paper

ISP MANUAL

WinCUPL™ MANUAL

POF2JED APP NOTE

LOGIC DOUBLING™ FILES

Click to link to website to download files.

Logic Doubling tutorial and Design source files
"Logic Doubling™" White paper describes typical CPLD logic usability problems and documents the reference designs which illustrate them, and the main architectural features of Logic Doubling™. The paper describes how the ATF15xx Family products used in the reference designs combined with second generation Atmel fitters address these problems by packing more logic functionality into a same size chip than a typical CPLD. It shows how packing more into the devices, leaves additional logic resources for future revisions, reducing the chance of a PCB re-spin.

http://www.adobe.com/products/acrobat/readstep.html