



N-Channel 2.5-V (G-S) MOSFET

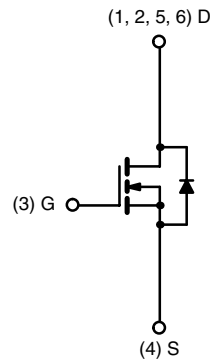
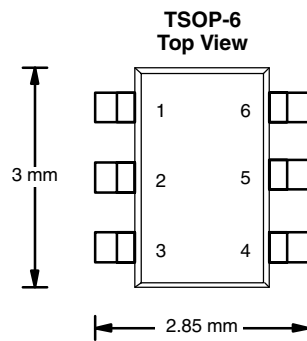
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.045 @ $V_{GS} = 4.5$ V	5.3
	0.065 @ $V_{GS} = 2.5$ V	4.4

FEATURES

- TrenchFET® Power MOSFET
- 100% R_g Tested



RoHS
COMPLIANT



Ordering Information: Si3446DV-T1
Si3446DV-T1-E3 (Lead (Pb)-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	5.3	A
	$T_A = 70^\circ\text{C}$		4.2	
Pulsed Drain Current		I_{DM}	20	
Continuous Source Current (Diode Conduction) ^a		I_S	1.7	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.0	W
	$T_A = 70^\circ\text{C}$		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 5$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

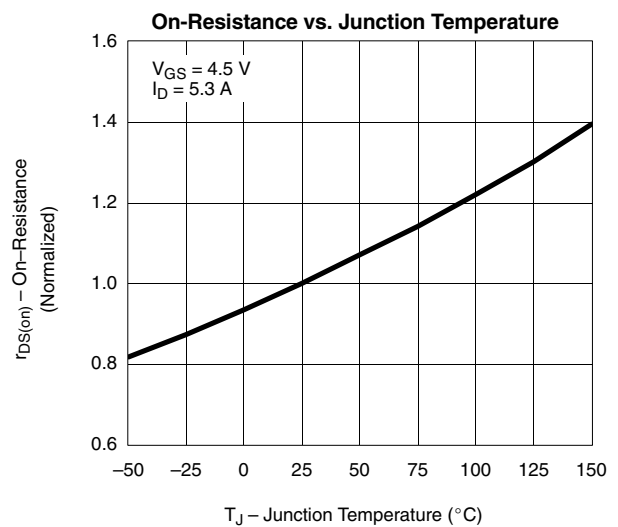
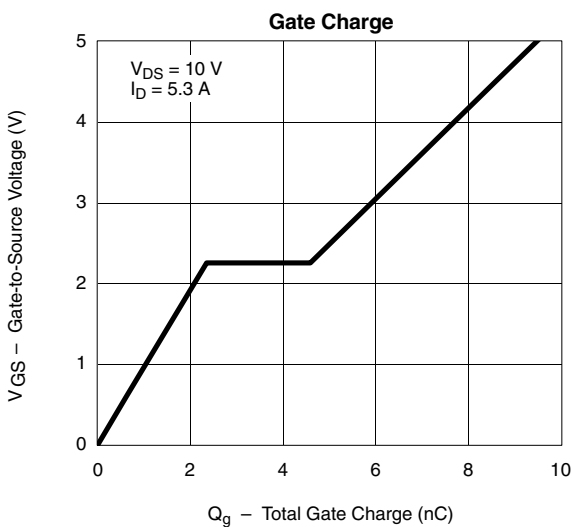
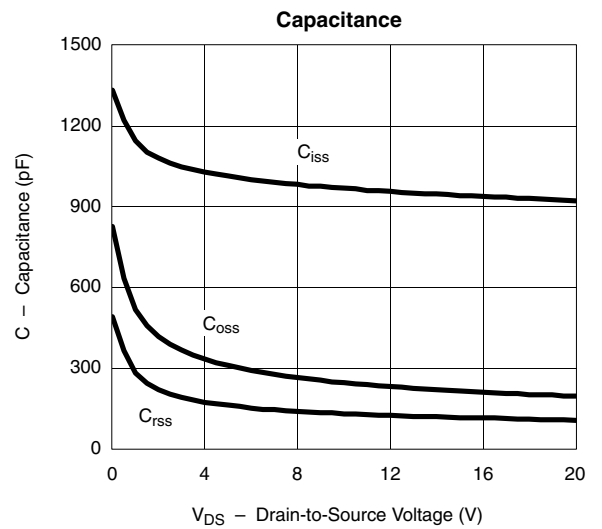
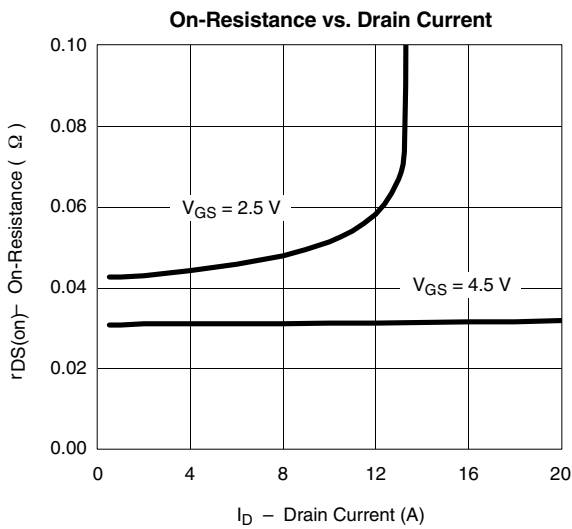
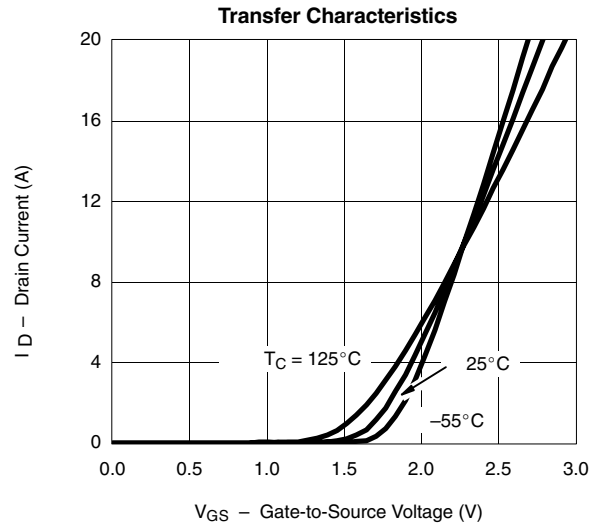
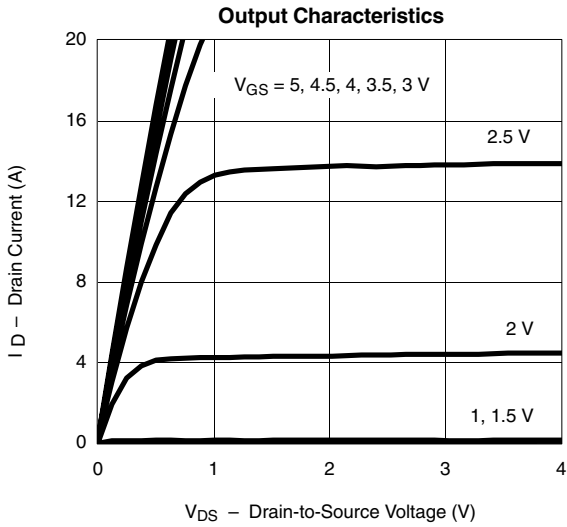
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.6		1.6	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 70 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	10			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 5.3 A		0.032	0.045	Ω
		V _{GS} = 2.5 V, I _D = 4.4 A		0.045	0.065	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 5.3 A		20		S
Diode Forward Voltage ^a	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V			1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 5.3 A		10	20	nC
Gate-Source Charge	Q _{gs}			2.5		
Gate-Drain Charge	Q _{gd}			2.2		
Gate Resistance	R _g		0.5		3.0	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω		30	50	ns
Rise Time	t _r			50	80	
Turn-Off Delay Time	t _{d(off)}			65	100	
Fall Time	t _f			35	60	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 1.7 A, di/dt = 100 A/μs		60	

Notes

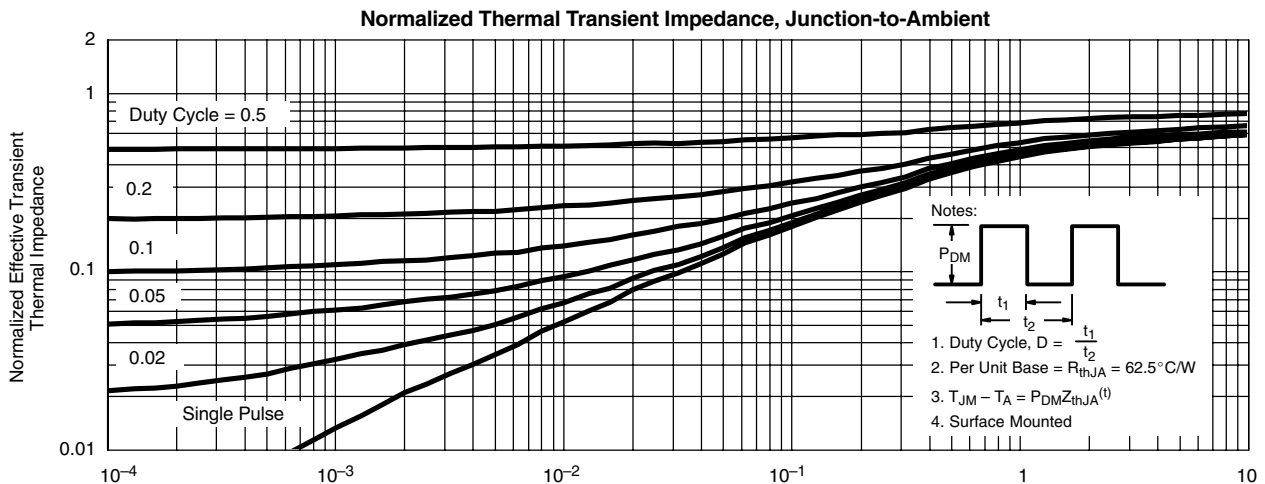
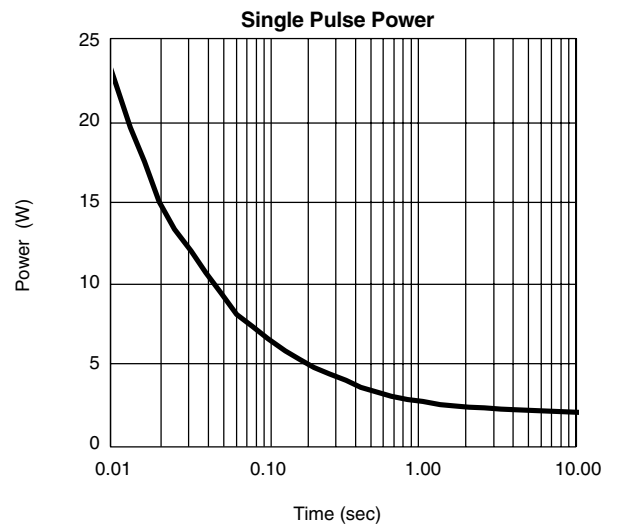
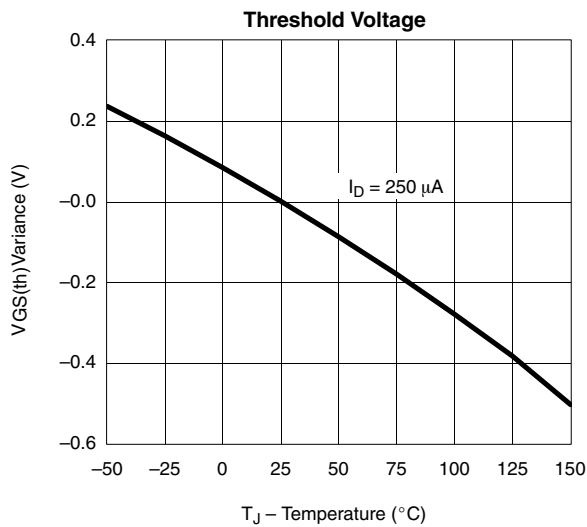
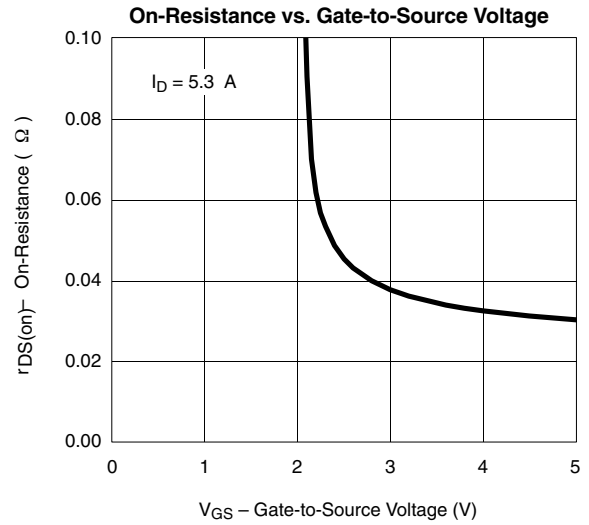
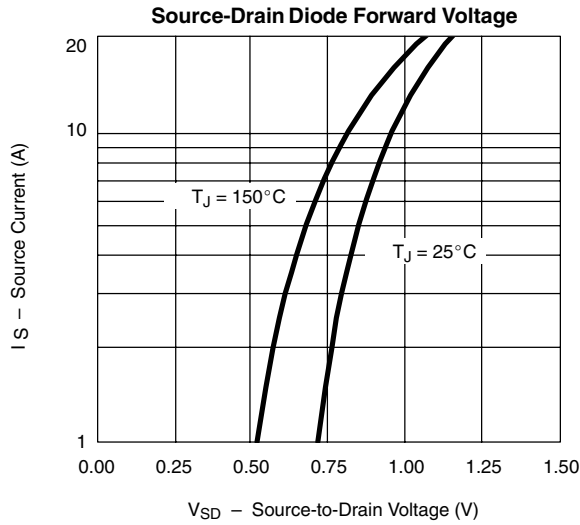
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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