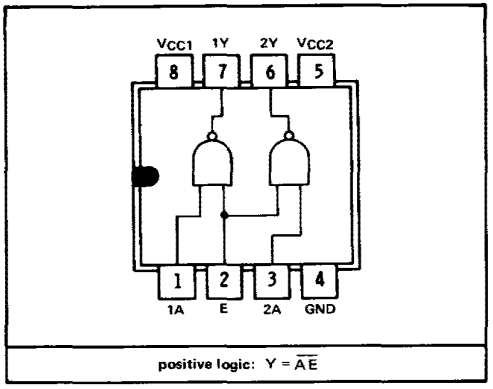
# TYPE SN75361A
# DUAL NAND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712054, SEPTEMBER 1973—REVISED APRIL 1977

## MOS MEMORY INTERFACE

- Dual Positive-Logic NAND TTL-to-MOS Driver
- Versatile Interface Circuit for Use between TTL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs
- $V_{CC2}$ Supply Voltage Variable over Wide Range to 24 Volts Maximum
- TTL and DTL Compatible Diode-Clamped Inputs
- Operates from Standard Bipolar and MOS Supply Voltages
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation
- Low Standby Power Dissipation

JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)




positive logic: $Y = \overline{AE}$

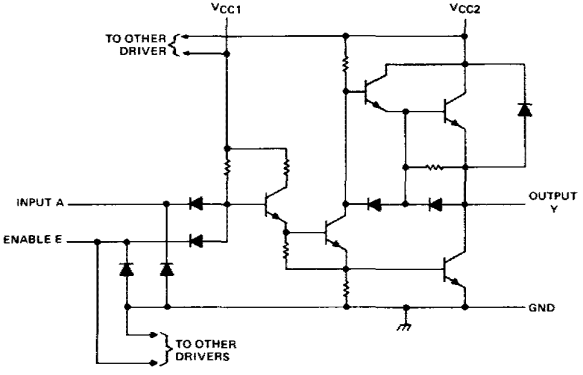
### description

The SN75361A is a monolithic integrated dual TTL-to-MOS driver and interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs including the TMS 1103 and TMS 4062.

The SN75361A operates from the TTL 5-volt supply and the MOS $V_{SS}$ supply in many applications. This device has been optimized for operation with $V_{CC2}$ supply voltage from 16 volts to 20 volts; however, it is designed so as to be useable over a much wider range of $V_{CC2}$.

The SN75361A is characterized for operation from 0°C to 70°C.

### schematic (each driver)






TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|---|
| Supply voltage range of $V_{CC1}$ (see Note 1) | −0.5 V to 7 V |
| Supply voltage range of $V_{CC2}$ | −0.5 V to 25 V |
| Input voltage | 5.5 V |
| Inter-input voltage (see Note 2) | 5.5 V |
| Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3): | |
| JG package | 825 mW |
| P package | 1000 mW |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | −65°C to 150°C |
| Lead temperature 1/16 inch from case for 60 seconds: JG package | 300°C |
| Lead temperature 1/16 inch from case for 10 seconds: P package | 260°C |

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between the A input of either driver and the common E input.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the JG package, SN75361A chips are glass-mounted.

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC1}$ | 4.75 | 5 | 5.25 | V |
| Supply voltage, $V_{CC2}$ | 4.75 | 20 | 24 | V |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

5

## electrical characteristics over recommended ranges of $V_{CC1}$, $V_{CC2}$, and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $I_I = -12$ mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{IL} = 0.8$ V, | $I_{OH} = -50$ μA | $V_{CC2}-1$ | $V_{CC2}-0.7$ | | V |
| | | $V_{IL} = 0.8$ V, | $I_{OH} = -10$ mA | $V_{CC2}-2.3$ | $V_{CC2}-1.8$ | | |
| $V_{OL}$ | Low-level output voltage | $V_{IH} = 2$ V, | $I_{OL} = 10$ mA | | 0.15 | 0.3 | V |
| | | $V_{CC2} = 15$ V to 24 V, $V_{IH} = 2$ V, $I_{OL} = 40$ mA | | | 0.25 | 0.5 | V |
| $V_{OK}$ | Output clamp voltage | $V_I = 0$ V, | $I_{OH} = 20$ mA | | | $V_{CC2}+1.5$ | V |
| $I_I$ | Input current at maximum input voltage | $V_I = 5.5$ V | | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_I = 2.4$ V | A inputs | | | 40 | μA |
| | | | E input | | | 80 | |
| $I_{IL}$ | Low-level input current | $V_I = 0.4$ V | A inputs | | −1 | −1.6 | mA |
| | | | E input | | −2 | −3.2 | |
| $I_{CC1(H)}$ | Supply current from $V_{CC1}$, both outputs high | $V_{CC1} = 5.25$ V, | $V_{CC2} = 24$ V, | | 2 | 4 | mA |
| $I_{CC2(H)}$ | Supply current from $V_{CC2}$, both outputs high | All inputs at 0 V, | No load | | | 0.5 | |
| $I_{CC1(L)}$ | Supply current from $V_{CC1}$, both outputs low | $V_{CC1} = 5.25$ V, | $V_{CC2} = 24$ V, | | 16 | 24 | mA |
| $I_{CC2(L)}$ | Supply current from $V_{CC2}$, both outputs low | All inputs at 5 V, | No load | | 7 | 13 | |
| $I_{CC2(S)}$ | Supply current from $V_{CC2}$, standby condition | $V_{CC1} = 0$ V, All inputs at 5 V, | $V_{CC2} = 24$ V, No load | | | 0.5 | mA |

†All typical values are at $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, and $T_A = 25°C$.

5

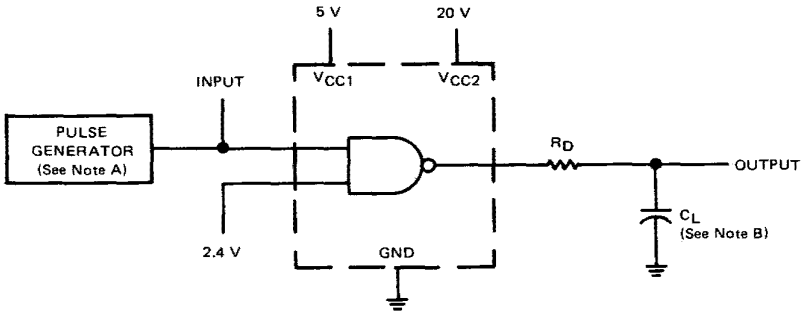
## switching characteristics, $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, $T_A = 25°C$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{DLH}$ | Delay time, low-to-high-level output | $C_L = 390$ pF, $R_D = 10\ \Omega$, See Figure 1 | | 11 | 24 | ns |
| $t_{DHL}$ | Delay time, high-to-low-level output | | | 10 | 20 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 25 | 40 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 21 | 35 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | | 10 | 36 | 55 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | 10 | 31 | 47 | ns |

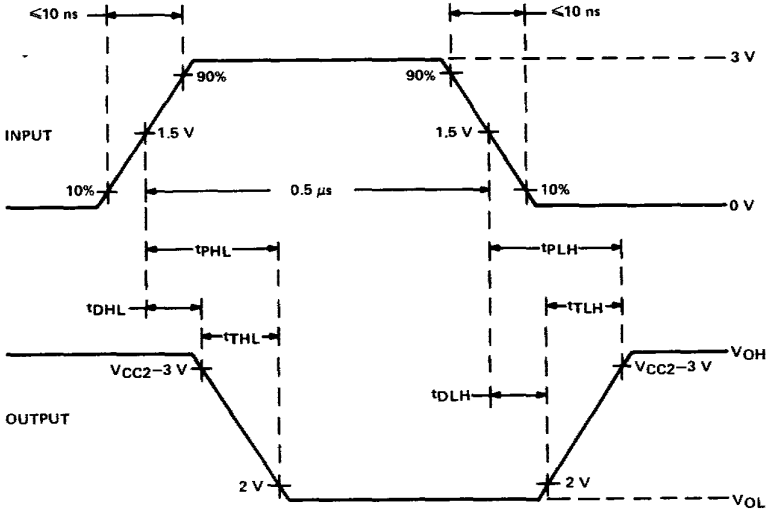


TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. $C_L$ includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

5

## TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

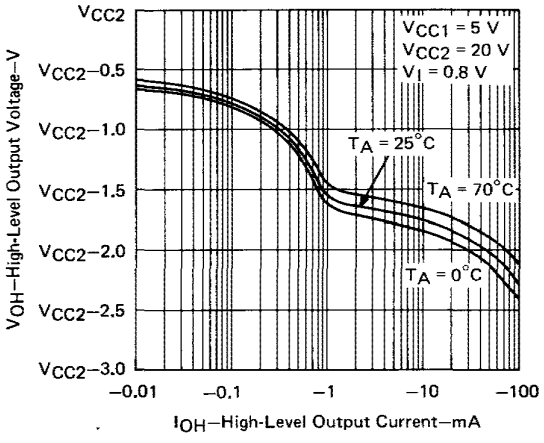



FIGURE 2

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

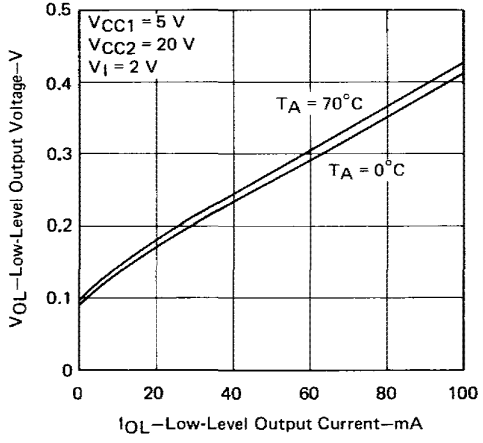



FIGURE 3

VOLTAGE TRANSFER CHARACTERISTICS

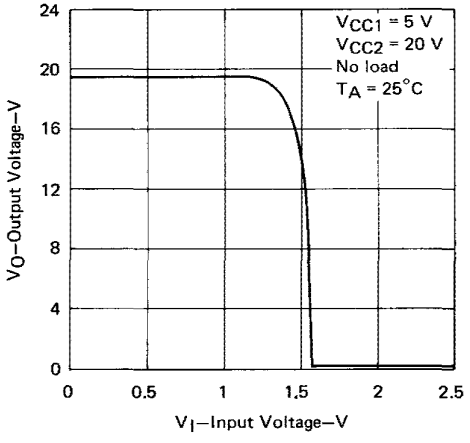



FIGURE 4

TOTAL DISSIPATION
(BOTH DRIVERS)
vs
FREQUENCY

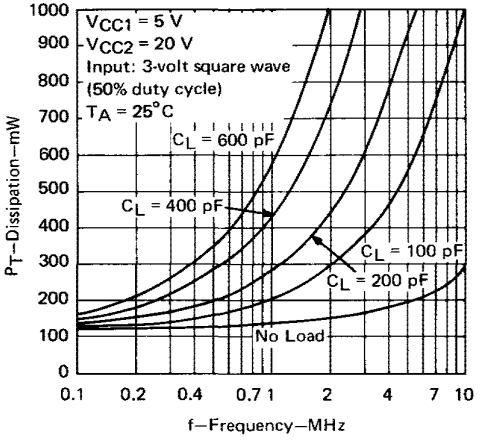



FIGURE 5

5

## TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

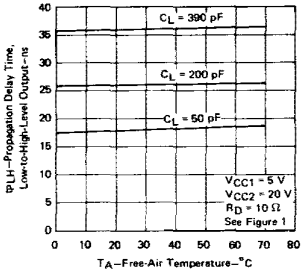



FIGURE 6

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

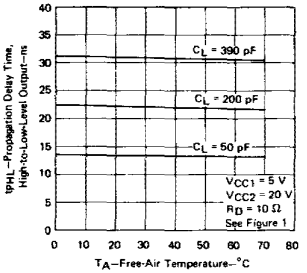



FIGURE 7

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
$V_{CC2}$ SUPPLY VOLTAGE

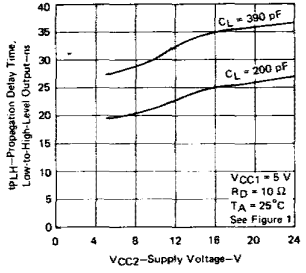



FIGURE 8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
$V_{CC2}$ SUPPLY VOLTAGE

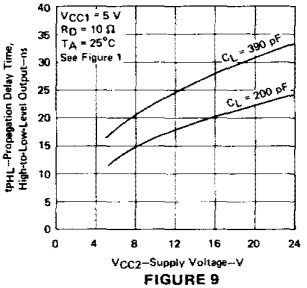



FIGURE 9

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
LOAD CAPACITANCE

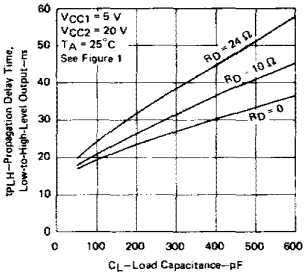



FIGURE 10

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
LOAD CAPACITANCE

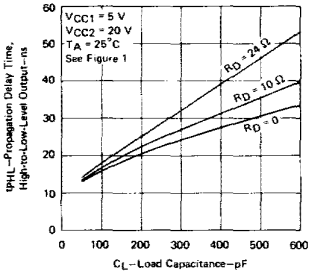



FIGURE 11

5

## TYPICAL APPLICATION DATA

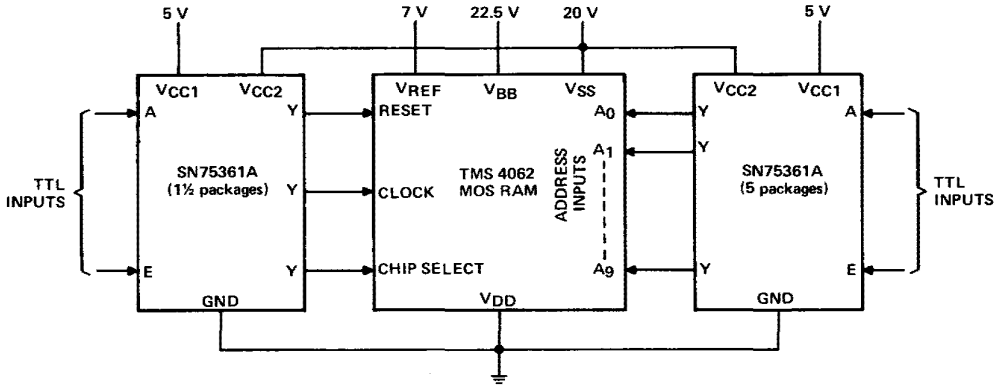



FIGURE 12–INTERCONNECTION OF SN75361A DEVICES WITH TMS4062-TYPE P-CHANNEL MOS RAM

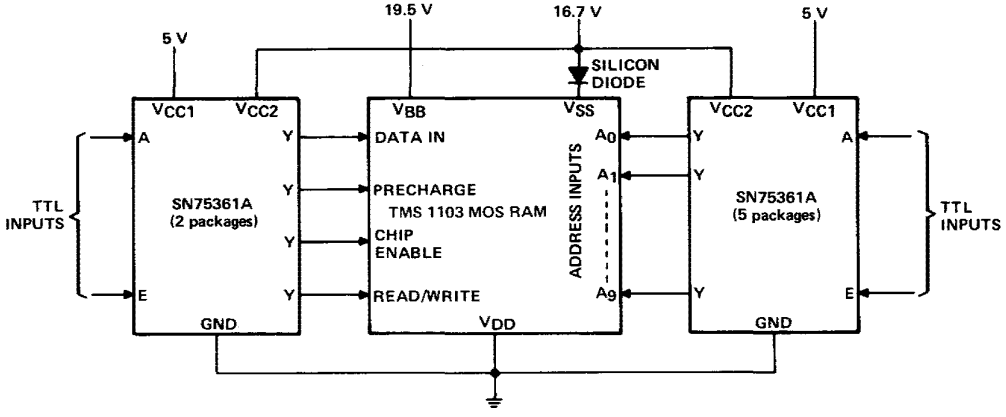



FIGURE 13–INTERCONNECTION OF SN75361A DEVICES WITH '1103-TYPE SILICON-GATE MOS RAM

## TYPICAL APPLICATION DATA

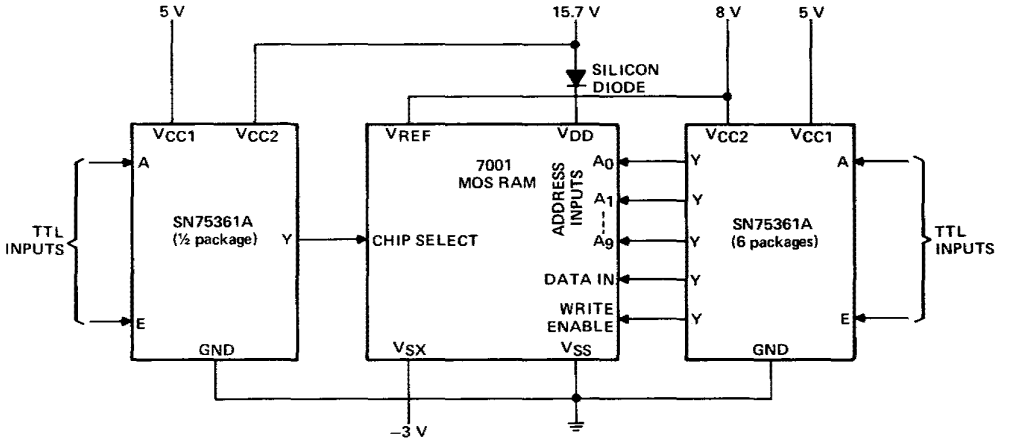
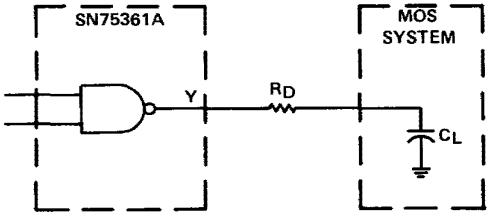



FIGURE 14—INTERCONNECTION OF SN75361A DEVICES WITH 7001-TYPE N-CHANNEL MOS RAM




NOTE: $R_D \approx 10\ \Omega$ to $30\ \Omega$ (optional).

FIGURE 15—USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN SN75361A APPLICATIONS

Applications using SN75361A as interface devices between TTL inputs and the address, control, and timing inputs for three types of MOS RAMs are shown in Figures 12, 13, and 14. A silicon diode is used in Figures 13 and 14 to increase the SN75361A high-level output voltage to obtain the desired high-level input voltage required by these MOS RAMs. An extra power supply could be used in place of the diode.

Figures 12, 13, and 14 show the use of the SN75361A over a wide range of $V_{CC2}$ supply voltages. The device may even be used as a TTL gate, if desired, by connecting $V_{CC2}$ to 5 volts.

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor to use depends on the specific load characteristics and switching speed. A typical value would be between $10\ \Omega$ and $30\ \Omega$. See Figure 15.

5

## THERMAL INFORMATION

### power dissipation precautions

Significant power may be dissipated in the SN75361A driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 5 shows the power dissipated in a typical SN75361A as a function of load capacitance and frequency. Average power dissipated by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{p_L t_L + p_H t_H}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{p_{LH} t_{LH} + p_{HL} t_{HL}}{T}$$

where the times are as defined in Figure 16.

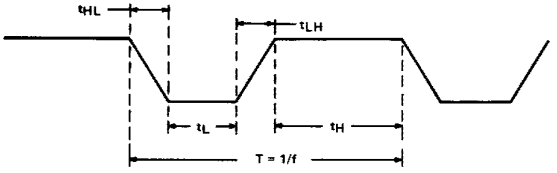



FIGURE 16–OUTPUT VOLTAGE WAVEFORM

$p_L$, $p_H$, $p_{LH}$, and $p_{HL}$ are the respective instantaneous levels of power dissipation and C is load capacitance.

The SN75361A is so designed that $P_S$ is a negligible portion of $P_T$ in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that $P_S$ can be neglected. Figure 5 for no load demonstrates this point. The power dissipation contributions from both channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume both channels are operating identically with C = 200 pF, f = 2 MHz, $V_{CC1}$ = 5 V, $V_{CC2}$ = 20 V, and duty cycle = 60% outputs high ($t_H/T$ = 0.6). Also, assume $V_{OH}$ = 19.3 V, $V_{OL}$ = 0.1 V, $P_S$ is negligible, and that the current from $V_{CC2}$ is negligible when the output is high.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5\text{ V})\left(\frac{2\text{ mA}}{2}\right) + (20\text{ V})\left(\frac{0\text{ mA}}{2}\right)\right](0.6) + \left[(5\text{ V})\left(\frac{16\text{ mA}}{2}\right) + (20\text{ V})\left(\frac{7\text{ mA}}{2}\right)\right](0.4)$$

$P_{DC(AV)}$ = 47 mW per channel

$P_{C(AV)} \approx (200\text{ pF})\ (19.2\text{ V})^2\ (2\text{ MHz})$

$P_{C(AV)} \approx$ 148 mW per channel.

For the total device dissipation of the two channels:

$P_{T(AV)} \approx 2\ (47 + 148)$

$P_{T(AV)} \approx$ 390 mW typical for total package.



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222