C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

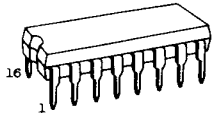
TC40H076P/F
TC40H076AP/AF

TC40H076 DUAL J-K FLIP-FLOP (PULSE TRIGGER TYPE)
TC40H076A DUAL J-K FLIP-FLOP (EDGE TRIGGER TYPE)

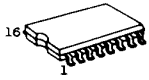
The TC40H076 is a dual J-K flip-flop with a synchronous clear preset function.

J-K mode: When both of $\overline{CLEAR}$ and $\overline{PRESET}$ are set to "H" level, and provided with CLOCK input, the output varies at the CLOCK 1 pulse for the TC40H076 and at the falling edge of $\overline{CLOCK}$ for the TC40H076A, depending on the conditions of J and K.

R-S mode: When $\overline{CLEAR}$ is set to "L" level and $\overline{PRESET}$ to "H" level, Q goes to "H" level and $\overline{Q}$ to "L" level regardless of the other inputs.



DIP16(3D16A-P)

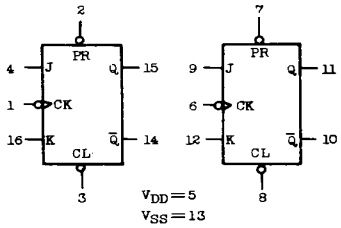


MFP16(F16GC-P)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+10$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

BLOCK DIAGRAM



* ALL INPUTS ARE EQUIPPED WITH PROTECTION CIRCUIT.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	2.0	-	8.0	V
Input Voltage	V_{IN}	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-40	-	85	°C

TRUTH TABLE (TC40H076)

INPUTS					OUTPUTS	
$\overline{PRESET}$	$\overline{CLEAR}$	$\overline{CLOCK}$	J	K	Q	$\overline{Q}$
L	H	*	*	*	H	L
H	L	*	*	*	L	H
L	L	*	*	*	H	H
H	H	⎍	L	L	NO CHANGE	
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

TRUTH TABLE (TC40H076A)

INPUTS					OUTPUTS	
$\overline{PRESET}$	$\overline{CLEAR}$	$\overline{CLOCK}$	J	K	Q	$\overline{Q}$
L	H	*	*	*	H	L
H	L	*	*	*	L	H
L	L	*	*	*	H	H
H	H	⎍	L	L	NO CHANGE	
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	
H	H	⎍	×	×	NO CHANGE	

* Don't Care
⎍ One high-Level Pulse
⎍ Transition from Low to high level.
⎍ Transition from high to Low level.

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TC40H076P/F
TC40H076AP/AF

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0.0	-	V_{DD}	V
Operating Temperature	topr	-	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\lvert I_{OUT}\rvert$<1μA $V_{IN}=V_{SS}, V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\lvert I_{OUT}\rvert$<1μA $V_{IN}=V_{SS}, V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS}, V_{DD}$	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS}, V_{DD}$	5	1.4	-	1.1	-	-	0.8	-	mA
Input Voltage	"H" Level	V_{IH}	$\lvert I_{OUT}\rvert$<1μA V_{OH}=4.5V V_{IL}=0.5V	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level	V_{IL}		5	-	1.0	-	-	1.0	-	1.0	V
Input Current	"H" Level	I_{IH}	V_{IH}=8.0V	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	8	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS}, V_{DD}$	5	-	5.0	-	10^{-2}	5.0	-	25.0	μA

*All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Circuit 1	5	-	24	40	ns
Output Fall Time		tof	Circuit 1	5	-	18	40	ns
Propagation Delay Time	(Low-High)	t_{pLH}	Circuit 1 $\overline{CLOCK}$-Q, $\overline{Q}$	5	-	27	50	ns
	(High-Low)	t_{pHL}			-	37	55	
Propagation Delay Time	(Low-High)	t_{pLH}	Cirucit 1 $\overline{CL}$, $\overline{PR}$-Q, $\overline{Q}$	5	-	40	60	ns
	(High-Low)	t_{pHL}			-	56	85	
Max. Clock Frequency		$f_{MAX\phi}$		5	10	20	-	MHz
Min. Data Setup Time		$t_{set\ up}$	Circuit 3 TC40H076A	5	-	-	25	ns
Min. Data Setup Time		$t_{set\ up}$	Circuit 2 TC40H076	5	-	-	0	ns
Min. Data Hold Time		t_{hold}	Circuit 3 TC40H076A	5	-	-	0	ns
Min. Data Hold Time		t_{hold}	Circuit 2 TC40H076	5	-	-	0	ns
Min. Clear and Preset Pulse Width		t_w	Cirucit 1 $\overline{CLEAR}$, $\overline{PRESET}$	5	-	23	40	ns

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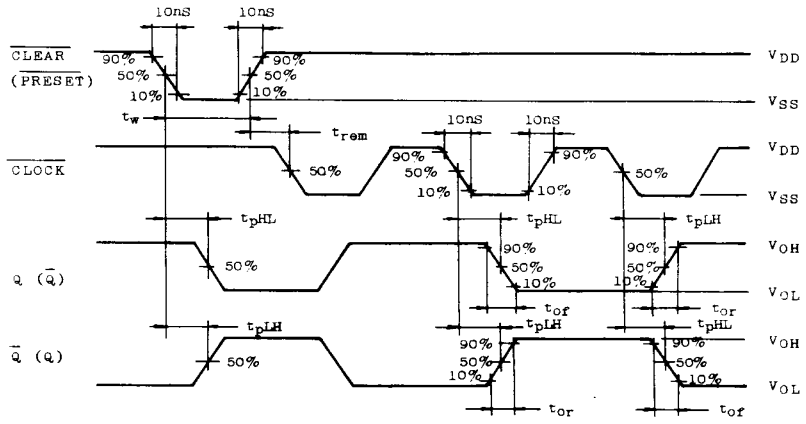
(CONTINUE)

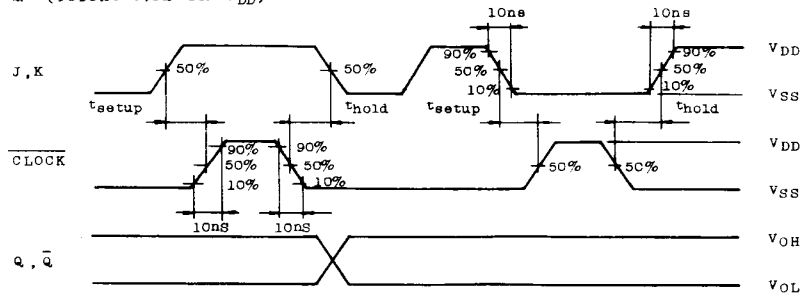
CHARACTERISTIC	SYMBOL	TEST CONSITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Max. Clock Rise Time Max. Clock Fall Time	$t_{r\phi}$ $t_{f\phi}$		5	0.5	-	-	μS
Min. Clear and Preset Removal Time	t_{rem}	CIRCUIT 1	5	-	15	30	ns
Input Capacitance	C_{IN}			-	5	-	pF

SWITCHING TIME TEST WAVEFORM

CIRCUIT 1. ($J=K=V_{DD}$, $\overline{CL}$ or $\overline{PR}=V_{DD}$)



CIRCUIT 2. (TC40H076, $\overline{CL}=\overline{PR}=V_{DD}$)



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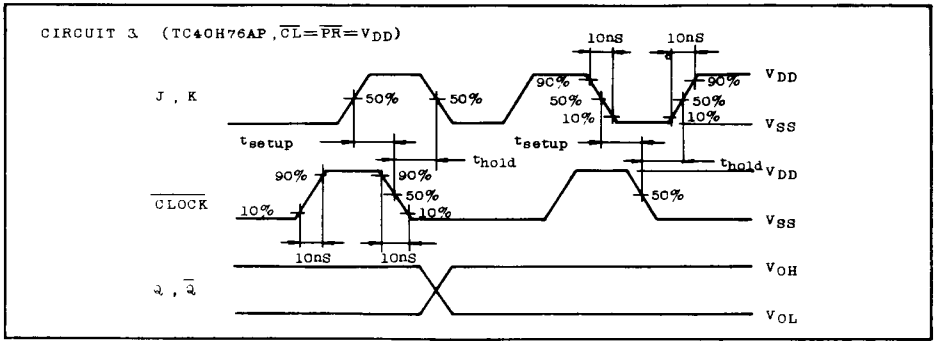
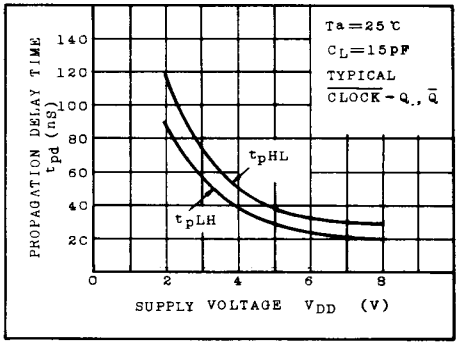
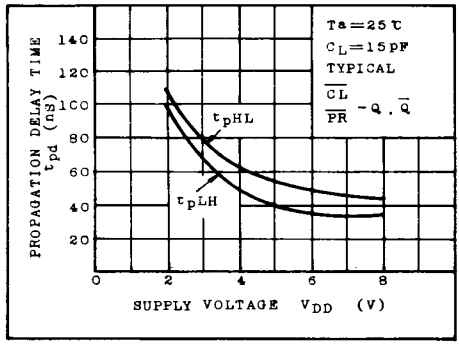
SWITCHING TIME TEST WAVEFORM



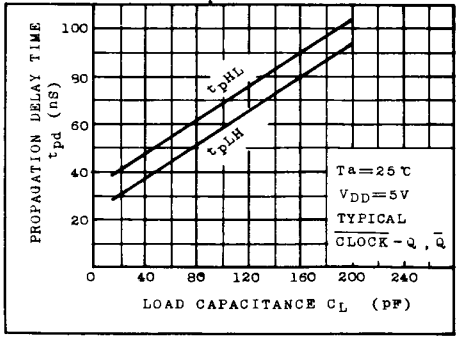
t_{pd} - V_{DD}



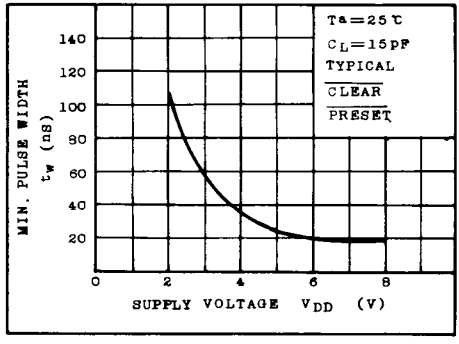
t_{pd} - V_{DD}



t_{pd} - C_L



t_W - V_{DD}



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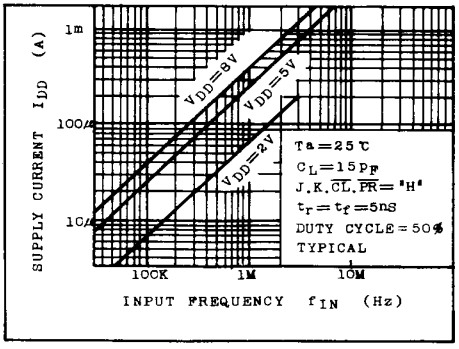
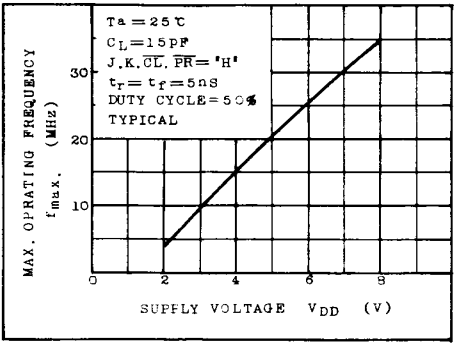
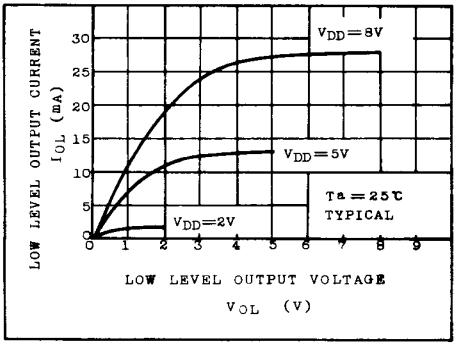
I_{DD} - f_{IN}



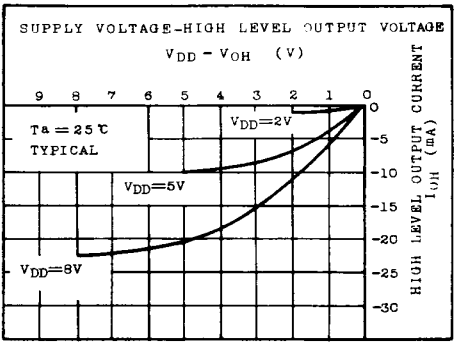
$f_{MAX\phi}$ - V_{DD}



I_{OL} - V_{OL}



I_{OH} - (V_{DD} - V_{OH})



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