1.2A High Efficient Step Down Converter with Snooze Mode

Check for Samples: TPS62080, TPS62080A, TPS62081, TPS62082

FEATURES

- **DCS-Control™ Architecture for Fast Transient Regulation**
- **Snooze Mode for 6.5µA Ultra Low Quiescent Current**
- **2.3V to 6.0V Input Voltage Range**
- **Supports High Output Capacitance up to 100µF**
- **100% Duty Cycle for Lowest Dropout**
- **Power Save Mode for Light Load Efficiency**
- **Output Discharge Function**
- **Short Circuit Protection**
- **Power Good Output**
- **Thermal Shutdown**
- **Available in 2x2mm 8-Pin SON Package and VSSOP Package**

APPLICATIONS

- **Battery Powered Portable Devices**
- **Point of Load Regulators**
- **System Power Rail Voltage Conversion**

DESCRIPTION

The TPS6208x devices are a family of high frequency synchronous step down converters. With an input voltage range of 2.3V to 6.0V, common battery technologies are supported. Alternatively, the device can be used for low voltage system power rails.

The TPS6208x focuses on high efficient step down conversion over a wide output current range. At medium to heavy loads, the converter operates in PWM mode and automatically enters Power Save Mode operation at light load currents to maintain high efficiency over the entire load current range. To maintain high efficiency at very low load or no load currents, a Snooze Mode with an ultra low quiescent current is implemented, that is enabled by the Mode pin. This function increases the run-time of battery driven applications and keeps the standby current at its lowest level to meet green energy standards targeting for a low stand-by current.

To address the requirements of system power rails, the internal compensation circuit allows a large selection of external output capacitor values ranging from 10µF up to 100uF effective capacitance. With its DCS-Control™ architecture excellent load transient performance and output voltage regulation accuracy is achieved. The device is available in 2x2mm SON package and VSSOP package with Thermal PAD.

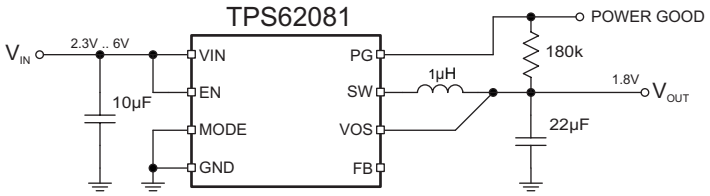


Figure 1. Typical Application of TPS62081 (1.8V Fixed Output)

Table 1. ORDERING INFORMATION

T_A	OUTPUT VOLTAGE(1)	PACKAGE MARKING	PACKAGE	PART NUMBER(2)
–40°C to 85°C	Adjustable	QVR	8-Pin SON	TPS62080DSG
	1.8 V	QVS	8-Pin SON	TPS62081DSG
	3.3 V	QVT	8-Pin SON	TPS62082DSG
	Adjustable	SBN	8-Pin SON	TPS62080ADSG
	Adjustable		8-Pin VSSOP	TPS62080ADGN(3)

(1) Contact the factory to check availability of other fixed output voltage versions.
(2) For detailed ordering information please check the PACKAGE OPTION ADDENDUM section at the end of this datasheet.
(3) Product Preview

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	VALUE	UNIT
Voltage range at VIN, PG, VOS(2)	–0.3 to 7	V
Voltage range at SW(2)(3)	–1 to 7	V
Voltage range at FB(2)	–0.3 to 3.6	V
Voltage range at EN, MODE(2)	–0.3 to (VIN + 0.3V)	V
ESD rating, Human Body Model	2	kV
ESD rating, Charged Device Model	500	V
Continuous total power dissipation	See Dissipation Rating Table	
Operating junction temperature range, T_J	–40 to 150	°C
Operating ambient temperature range, T_A	–40 to 85	°C
Storage temperature range, T_{stg}	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) During operation, device switching

THERMAL INFORMATION

THERMAL METRIC(1)		TPS62080 DSG (8 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	65.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	100.7	
θ_{JB}	Junction-to-board thermal resistance	135.7	
ψ_{JT}	Junction-to-top characterization parameter	2.3	
ψ_{JB}	Junction-to-board characterization parameter	45.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	8.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range, VIN	2.3		6.0	V
V_{OUT}	Output voltage range	0.5		4.0	V
I_{SNOOZE}	Maximum load current in Snooze Mode			2	mA
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

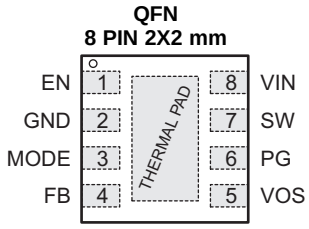
(1) Refer to the APPLICATION INFORMATION section for further information.

ELECTRICAL CHARACTERISTICS

Over recommended free-air temperature range, T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted), V_{IN}=3.6V, MODE = LOW.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.3		6.0	V
I_Q	Quiescent current into VIN	I_{OUT} = 0mA, Device not switching		30		uA
	Quiescent current into VIN (SNOOZE MODE)	I_{OUT} = 0mA, Device not switching, MODE=HIGH		6.5		uA
I_{SD}	Shutdown current into VIN	EN = LOW			1	µA
V_{UVLO}	Under voltage lock out	Input voltage falling		1.8	2.0	V
	Under voltage lock out hysteresis	Rising above V_{UVLO}		120		mV
T_{JSD}	Thermal shut down	Temperature rising		150		°C
	Thermal shutdown hysteresis	Temperature falling below T_{JSD}		20		°C
LOGIC INTERFACE (ENABLE, MODE)						
V_{IH}	High level input voltage	2.3V ≤ V_{IN} ≤ 6.0V	1			V
V_{IL}	Low level input voltage	2.3V ≤ V_{IN} ≤ 6.0V			0.4	V
I_{LKG}	Input leakage current			0.01	0.5	µA
POWER GOOD						
V_{PG}	Power good threshold	V_{OUT} falling referenced to V_{OUT} nominal	–15	–10	–5	%
	Power good hysteresis			5		%
V_{IL}	Low level voltage	I_{sink} = 500 µA			0.3	V
$I_{PG,LKG}$	PG Leakage current	V_{PG} = 5.0 V		0.01	0.1	µA
OUTPUT						
V_{OUT}	Output voltage range TPS62080, TPS62080A		0.5		4.0	V
	Output voltage accuracy TPS62081	I_{OUT} = 0 mA; V_{IN} ≥ 2.3V	–2.5		2.5	%
	Output voltage accuracy TPS62082	I_{OUT} = 0 mA; V_{IN} ≥ 3.6V	–2.5		2.5	%
	Snooze Mode output voltage accuracy	MODE = HIGH; V_{IN} ≥ 2.3V and V_{IN} ≥ V_{OUT} + 1V	–5		5	%
V_{FB}	Feedback regulation voltage TPS62080, TPS62080A	V_{IN} ≥ 2.3V and V_{IN} ≥ V_{OUT} + 1V	0.438	0.45	0.462	V
I_{FB}	Feedback input bias current TPS62080, TPS62080A	V_{FB} = 0.45 V		10	100	nA
R_{DIS}	Output discharge resistor	EN = LOW, V_{OUT} = 1.8 V		1		kΩ
		TPS62080A , EN = LOW, V_{OUT} = 1.2 V,	25	40	65	Ω
	Line Regulation			0		%/V
	Load Regulation	TPS62081, TPS62082		-0.25		%/A
$R_{DS(on)}$	High side FET on-resistance	I_{SW} = 500 mA		120		mΩ
	Low side FET on-resistance	I_{SW} = 500 mA		90		mΩ
I_{LIM}	High side FET switch current limit	Rising inductor current	1.6	2.8	4	A

DEVICE INFORMATION



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	8	PWR	Power Supply Voltage Input.
EN	1	IN	Device Enable Logic Input. Logic HIGH enables the device, logic LOW disables the device and turns it into shutdown.
MODE	3	IN	Snooze Mode Enable Logic Input. Logic HIGH enables the Snooze Mode, logic LOW disables the Snooze Mode
GND	2	PWR	Power and Signal Ground.
VOS	5	IN	Output Voltage Sense Pin for the internal control loop. Must be connected to output.
SW	7	PWR	Switch Pin connected to the internal MOSFET switches and inductor terminal. Connect the inductor of the output filter here.
FB	4	IN	Feedback Pin for the internal control loop. Connect this pin to the external feedback divider for the adjustable output version. For the fixed output voltage versions this pin must be left floating or connected to GND.
PG	6	OUT	Power Good open drain output. This pin is pulled to low if the output voltage is below regulation limits. Can be left floating if not used.
Thermal Pad			Connect it to GND.

FUNCTIONAL BLOCK DIAGRAMS

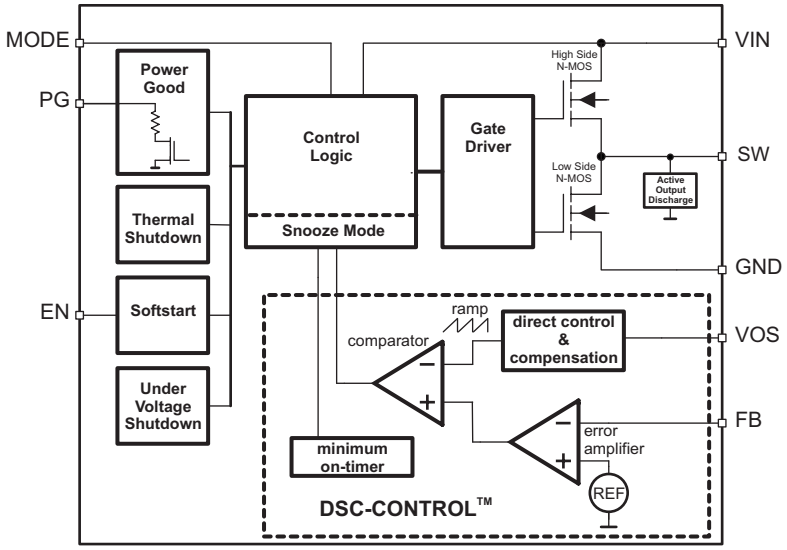


Figure 2. Functional Block Diagram (Adjustable Output Voltage Version)

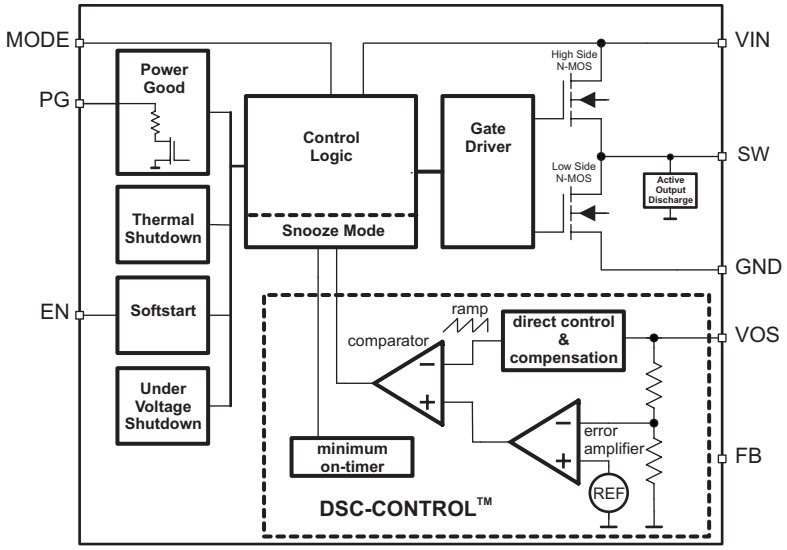


Figure 3. Functional Block Diagram (Fixed Output Voltage Version)

TYPICAL CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION

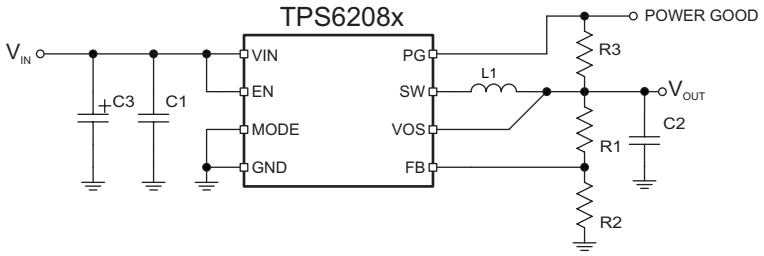


Table 2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10uF, Ceramic Capacitor, 6.3V, X5R, size 0603	Std
C2	22uF, Ceramic Capacitor, 6.3V, X5R, size 0805, GRM21BR60J226ME39L	Murata
C3	47uF, Tantalum Capacitor, 8V, 35mΩ, size 3528, T520B476M008ATE035	Kemet
L1	1.0µH, Power Inductor, 2.2A, size 3x3x1.2mm, XFL3012-102MEB	Coilcraft
R1	Depending on the output voltage of TPS62080, 1%; Not be populated for TPS62081, TPS62082;	
R2	39.2k, Chip Resistor, 1/16W, 1%, size 0603	Std
R3	178k, Chip Resistor, 1/16W, 1%, size 0603	Std

TABLE OF GRAPHS

		Figure
Efficiency	TPS62080, Load Current, V_{OUT} = 0.9V	Figure 4
	TPS62080, Load Current, V_{OUT} = 1.2V	Figure 5
	TPS62080, Load Current, V_{OUT} = 2.5V	Figure 6
	TPS62081, Load Current, V_{OUT} = 1.8V	Figure 7
	TPS62082, Load Current, V_{OUT} = 3.3V	Figure 8
Output Voltage Accuracy	TPS62080, Input Voltage, V_{OUT} = 0.9V	Figure 9
	TPS62080, Input Voltage, V_{OUT} = 2.5V	Figure 10
	TPS62081, Input Voltage, V_{OUT} = 1.8V	Figure 11
	TPS62082, Input Voltage, V_{OUT} = 3.3V	Figure 12
	TPS62080, Load Current, V_{OUT} = 0.9V	Figure 13
	TPS62080, Load Current, V_{OUT} = 2.5V	Figure 14
	TPS62081, Load Current, V_{OUT} = 1.8V	Figure 15
	TPS62082, Load Current, V_{OUT} = 3.3V	Figure 16
Quiescent Current	Input Voltage, Normal Mode	Figure 17
	Input Voltage, Snooze Mode	Figure 18
$R_{DS(on)}$	Input Voltage, High Side FET	Figure 19
	Input Voltage, Low Side FET	Figure 20
Switching Frequency	TPS62080, Load Current, V_{OUT} = 0.9V,	Figure 21
	TPS62080, Load Current, V_{OUT} = 2.5V,	Figure 22
Typical Operation	TPS62080, V_{IN} = 3.3V, V_{OUT} = 1.2V, Load Current = 500mA, PWM Mode	Figure 23
	TPS62080, V_{IN} = 3.3V, V_{OUT} = 1.2V, Load Current = 10mA, PFM Mode	Figure 24
	TPS62080, V_{IN} = 3.3V, V_{OUT} = 1.2V, Load Current = 2mA, Snooze Mode	Figure 25

		Figure
Load Transient	TPS62080, V_{IN} = 3.3V, V_{OUT} = 1.2V, Load Current = 50mA to 1A	Figure 26
Line Transient	TPS62080, V_{IN} = 3.3V to 4.2V, V_{OUT} = 1.2V, Load = 2.2Ω	Figure 27
Startup	TPS62080, V_{IN} = 3.3V, V_{OUT} = 1.2V, Load = 2.2Ω	Figure 28
	TPS62080, V_{IN} = 3.3V, V_{OUT} = 1.2V, No Load	Figure 29
Shutdown with Output Discharge	TPS62080, V_{IN} = 3.3V, V_{OUT} = 1.2V, No Load	Figure 30

EFFICIENCY vs LOAD CURRENT

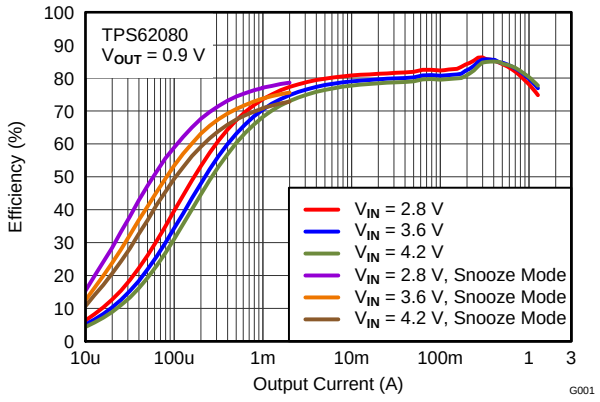


Figure 4.

EFFICIENCY vs LOAD CURRENT

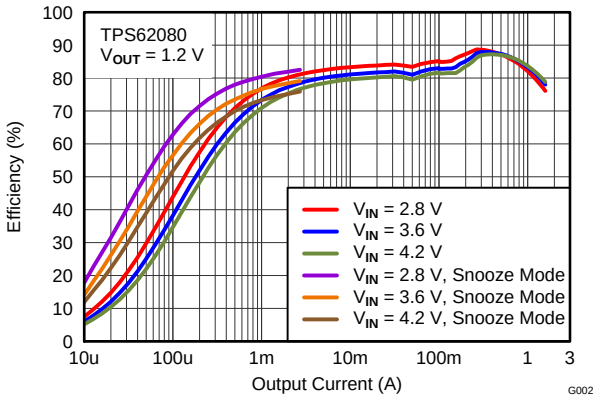


Figure 5.

EFFICIENCY vs LOAD CURRENT

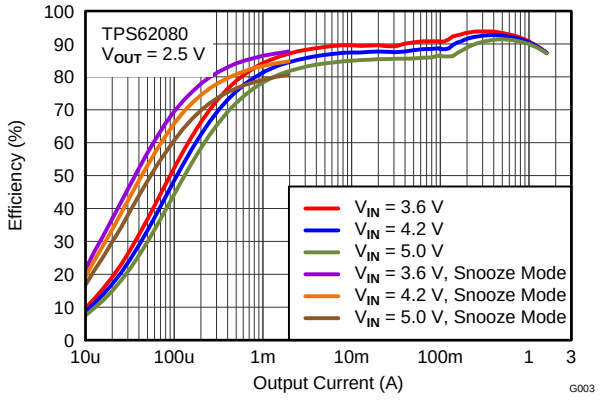


Figure 6.

EFFICIENCY vs LOAD CURRENT

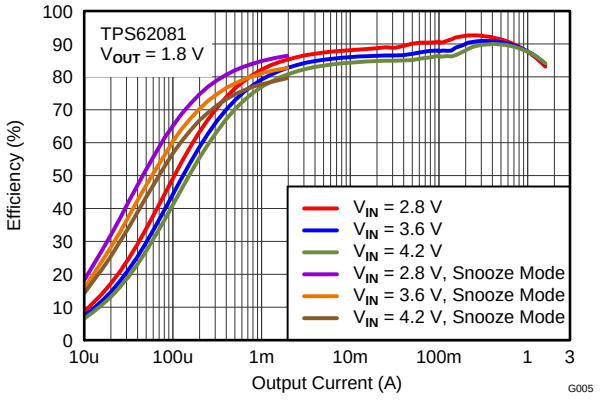


Figure 7.

EFFICIENCY vs LOAD CURRENT

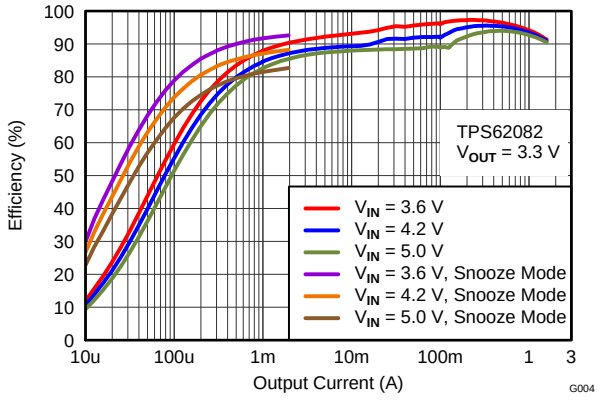


Figure 8.

OUTPUT VOLTAGE vs INPUT VOLTAGE

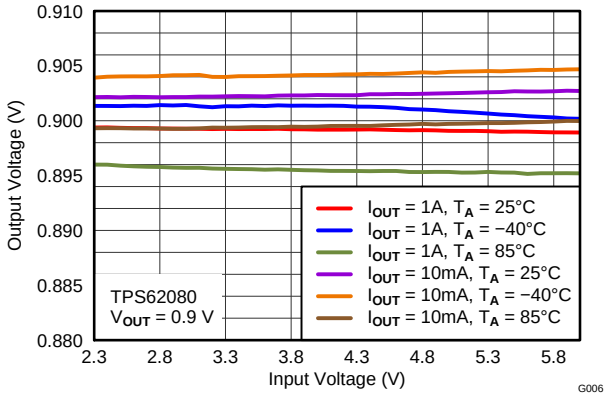


Figure 9.

OUTPUT VOLTAGE vs INPUT VOLTAGE

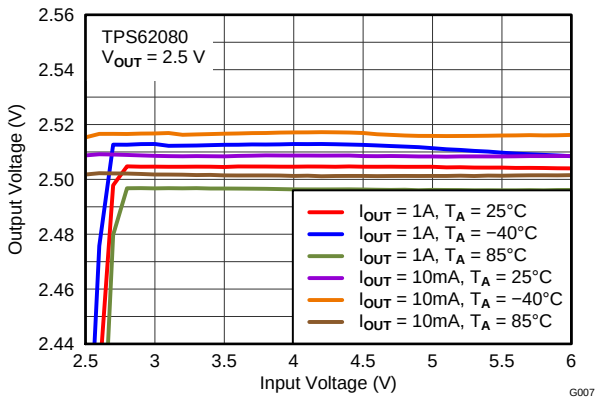


Figure 10.

OUTPUT VOLTAGE vs INPUT VOLTAGE

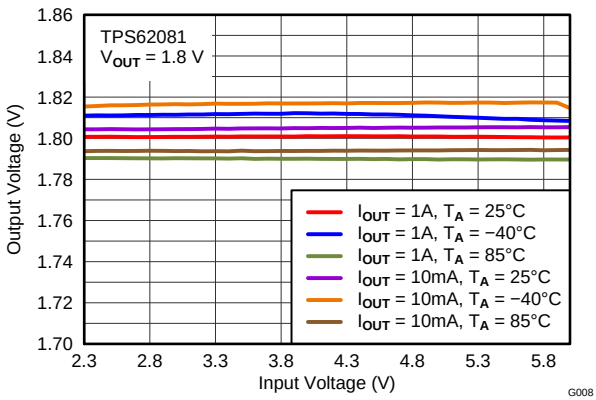


Figure 11.

OUTPUT VOLTAGE vs INPUT VOLTAGE

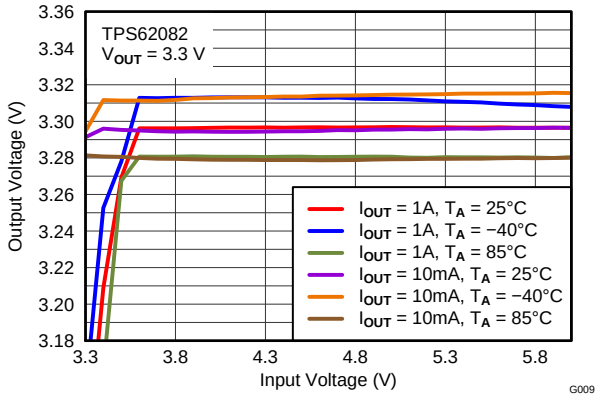


Figure 12.

OUTPUT VOLTAGE vs LOAD CURRENT

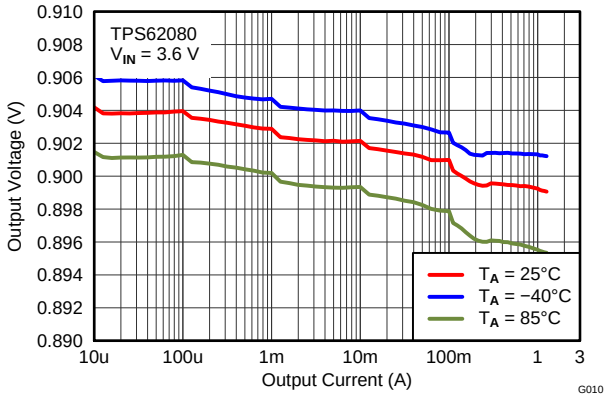


Figure 13.

OUTPUT VOLTAGE vs LOAD CURRENT

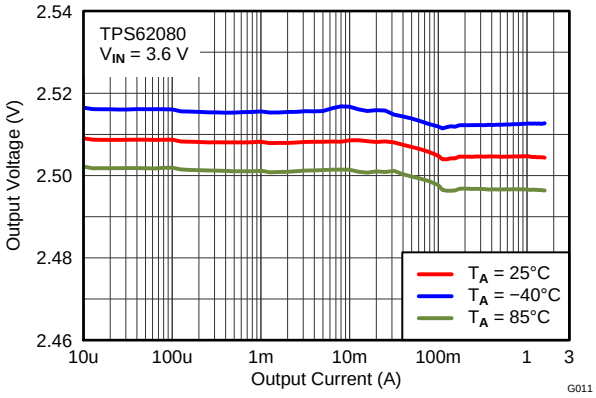


Figure 14.

OUTPUT VOLTAGE vs LOAD CURRENT

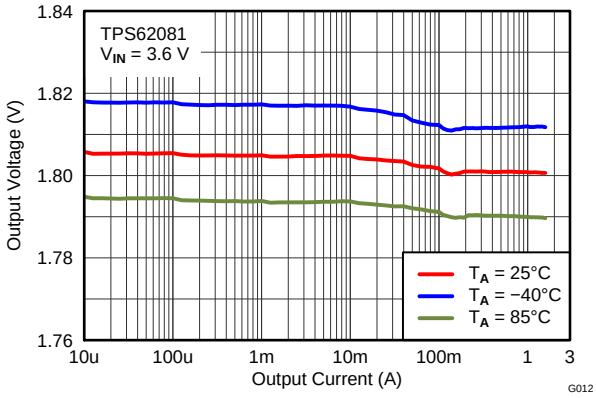


Figure 15.

OUTPUT VOLTAGE vs LOAD CURRENT

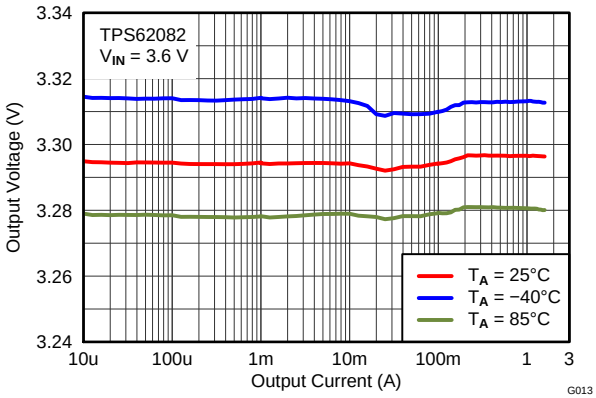


Figure 16.

QUIESCENT CURRENT vs INPUT VOLTAGE

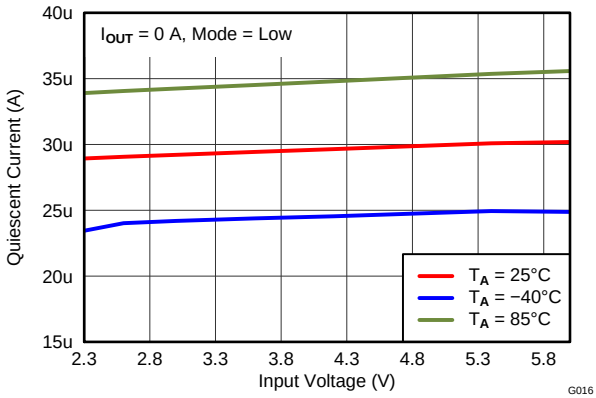


Figure 17.

QUIESCENT CURRENT vs INPUT VOLTAGE

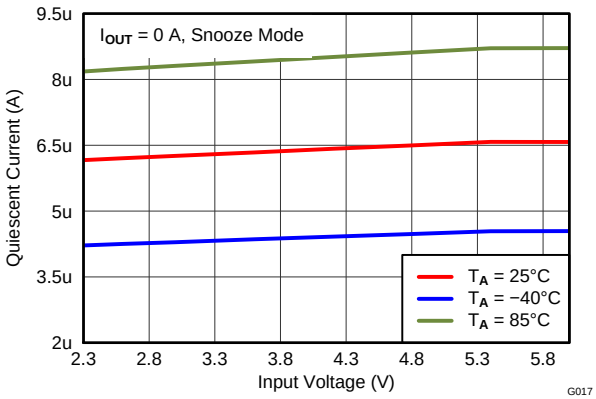


Figure 18.

HIGH SIDE FET $R_{DS(on)}$ vs INPUT VOLTAGE

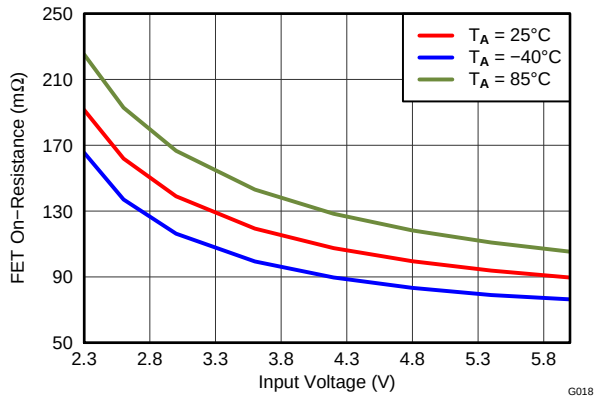


Figure 19.

LOW SIDE FET $R_{DS(on)}$ vs INPUT VOLTAGE

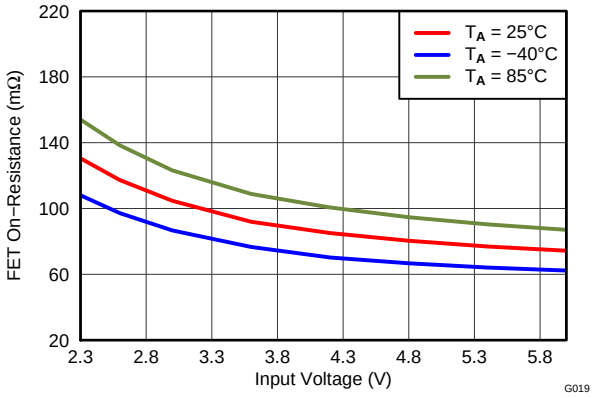


Figure 20.

SWITCHING FREQUENCY vs LOAD CURRENT

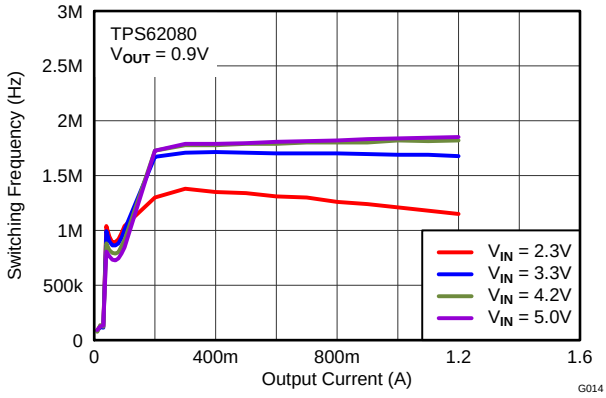


Figure 21.

SWITCHING FREQUENCY vs LOAD CURRENT

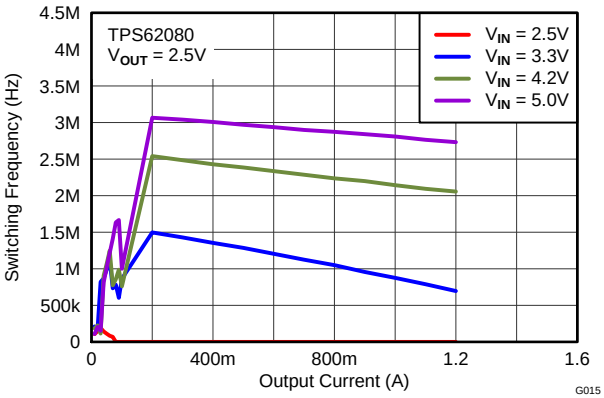


Figure 22.

TYPICAL APPLICATION (PWM MODE)

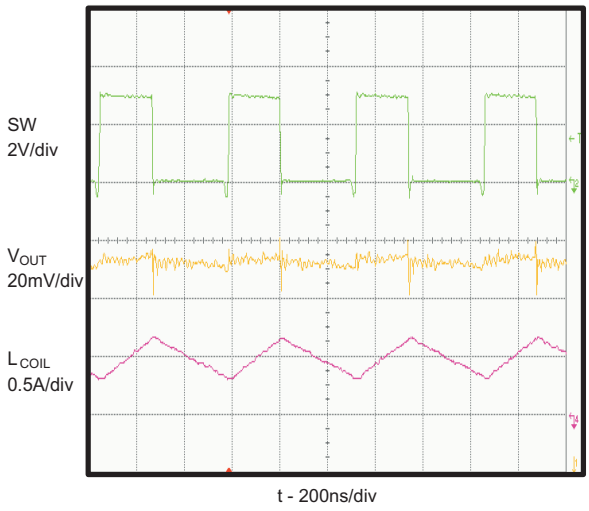


Figure 23.

TYPICAL APPLICATION (PFM MODE)

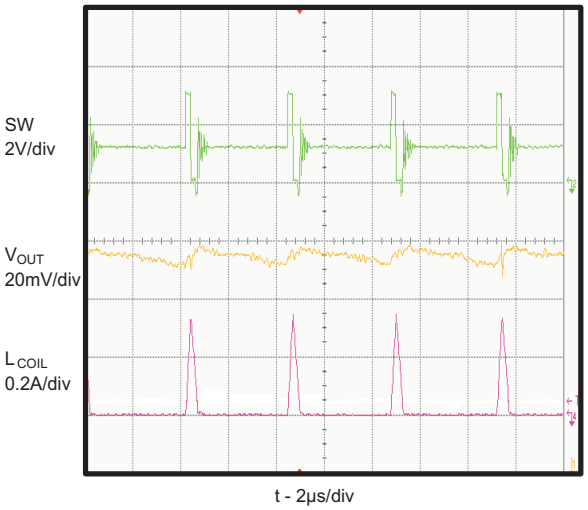


Figure 24.

TYPICAL APPLICATION (SNOOZE MODE)

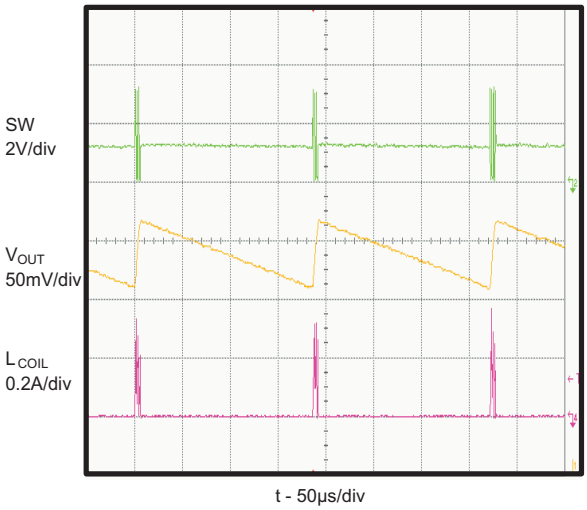


Figure 25.

LOAD TRANSIENT

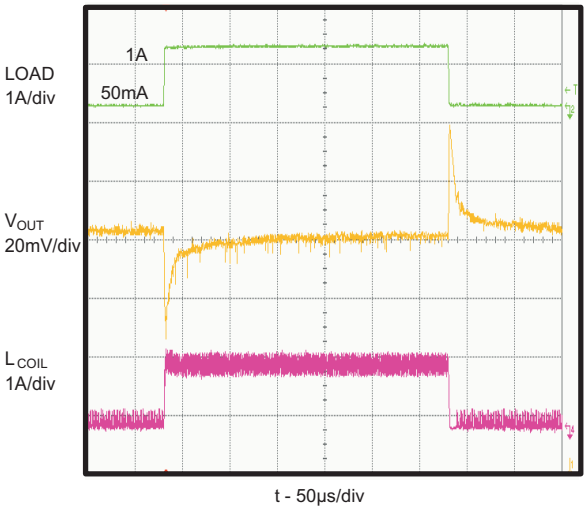


Figure 26.

LINE TRANSIENT

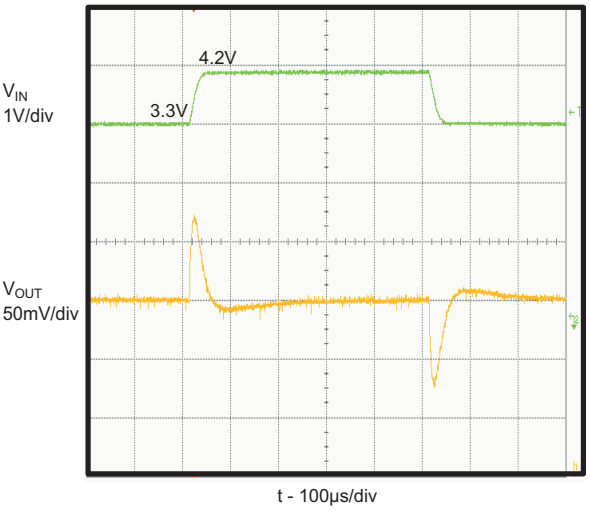


Figure 27.

START UP

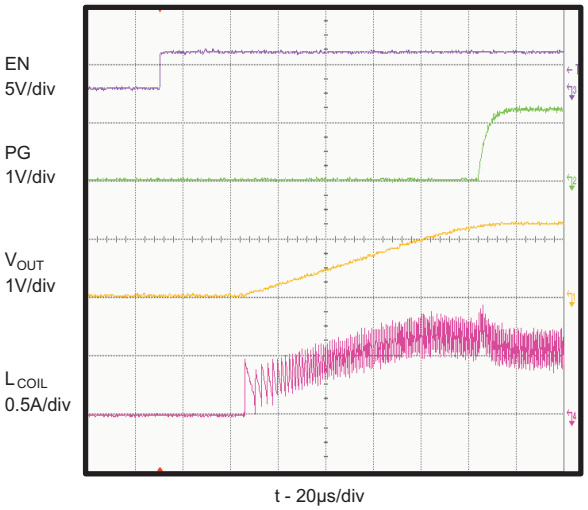


Figure 28.

START UP (WITHOUT LOAD)

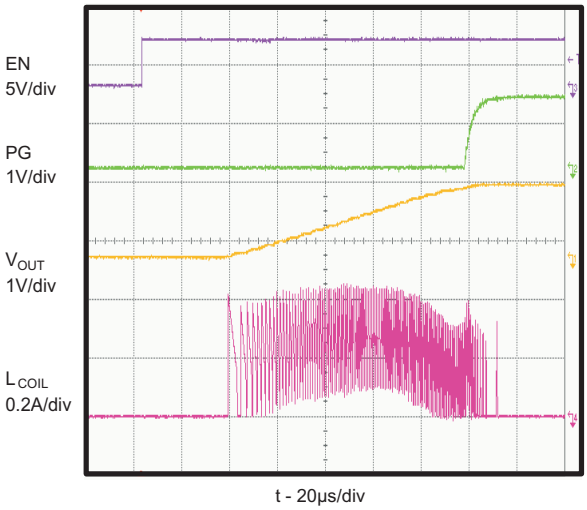


Figure 29.

SHUT DOWN

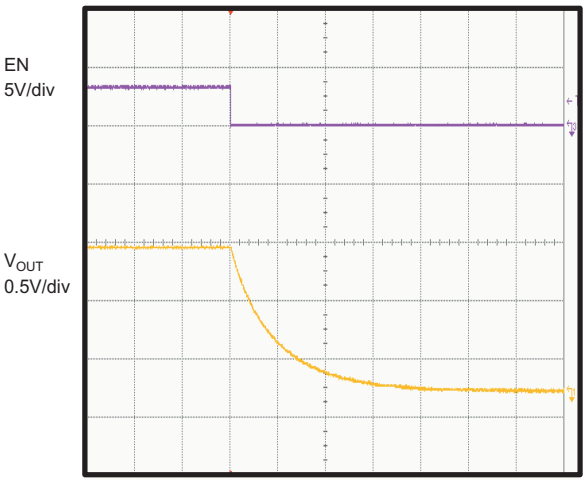


Figure 30.

DETAILED DESCRIPTION

DEVICE OPERATION

The TPS6208x synchronous switched mode converters are based on DCS™ Control (Direct Control with Seamless transition into Power Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control.

The DCS™ Control topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM the converter operates with its nominal switching frequency of 2MHz having a controlled frequency variation over the input voltage range. As the load current decreases the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. DCS™ Control supports both operation modes (PWM and PFM) using a single building block having a seamless transition from PWM to Power Save Mode without effects on the output voltage. Fixed output voltage versions provide smallest solution size combined with lowest quiescent current. The TPS6208x offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

The device is equipped with the Snooze Mode functionality, which is enabled with the Mode pin. The Snooze Mode supports high efficiency conversion at lowest output currents below 2mA. If no load current is drawn, the ultra low quiescent current of 6.5uA is sufficient to maintain the output voltage. This extends battery run time by reducing the quiescent current during lowest or no load conditions in battery driven applications. For mains-operated voltage supplies, the Snooze Mode reduces the system's stand-by energy consumption. During shutdown (EN = LOW), the device reduces energy consumption to less than 1uA.

POWER SAVE MODE

As the load current decreases the TPS6208x will enter the Power Save Mode operation. During Power Save Mode the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current maintaining high efficiency. The power save mode occurs when the inductor current becomes discontinuous. It is based on a fixed on time architecture. The typical on time is given by t_{on}=210ns·(V_{OUT} / V_{IN}). The switching frequency over the whole load current range is shown in Figure 21 and Figure 22.

SNOOZE MODE

The TPS6208x offers a Snooze Mode function. If the Snooze Mode is enabled by an external logic signal setting the MODE pin to HIGH, the device's quiescent current consumption is reduced to typically 6.5µA. As a result, the high efficiency range is extended towards the range of lowest output currents below 2mA, see the typical characteristics efficiency figures.

If the device is operating in Snooze Mode, a dedicated, low power consuming block monitors the output voltage. All other control blocks are snoozing during that time. If the output voltage falls below the programmed output voltage by 3.5% (typ), the control blocks wake up, regulates the output voltage and allow themselves to snooze again until the output voltage drops again. The Snooze Mode operation provides a clear efficiency improvement at lowest output currents. If the load current increases, the advantage of efficiency in Snooze mode will be deprived. Since the dynamic load regulation operates best if the Snooze Mode is disabled, it is recommended to turn off the Snooze Mode by external logic signal if the load current exceeds 2mA, like a micro controller to operate the MODE pin.

100% DUTY CYCLE LOW DROPOUT OPERATION

The device offers low input to output voltage difference by entering 100% duty cycle mode. In this mode the high side MOSFET switch is constantly turned on and the low side MOSFET is switched off. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain switching regulation, depending on the load current and output voltage can be calculated as:

$$V_{IN,MIN} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L) \quad (1)$$

With:

$V_{IN,MIN}$ = Minimum input voltage
$I_{OUT,MAX}$ = Maximum output current

$R_{DS(on)}$ = High side FET on-resistance
R_L = Inductor ohmic resistance

ENABLING / DISABLING THE DEVICE

The device is enabled by setting the EN input to a logic HIGH. Accordingly, a logic LOW disables the device. If the device is enabled, the internal power stage will start switching and regulate the output voltage to the programmed threshold. The EN input must be terminated with a resistance less than 1MΩ pulled to VIN or GND.

OUTPUT DISCHARGE

The output gets discharged by the SW pin with a typical discharge resistor of R_{DIS} whenever the device shuts down. This is the case when the device gets disabled by enable, thermal shutdown trigger, and undervoltage lockout trigger.

SOFT START

After enabling the device, an internal soft-start circuitry monotonically ramps up the output voltage and reaches the nominal output voltage during a soft start time (100µs, typical). This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

If the output voltage is not reached within the soft start time, such as in the case of heavy load, the converter will enter regular operation. Consequently, the inductor current limit will operate as described below. The TPS6208x is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

POWER GOOD

The TPS6208x has a power good output going low when the output voltage is below its nominal value. The power good keeps high impedance once the output is above 95% of the regulated voltage, and is driven to low once the output voltage falls below typically 90% of the regulated voltage. The PG pin is a open drain output and is specified to sink typically up to 0.5mA. The power good output requires a pull up resistor that is recommended connecting to the device output. When the device is off due to disable, UVLO or thermal shutdown, the PG pin is at high impedance.

The PG signal can be used for sequencing of multiple rails by connecting to the EN pin of other converters. Leave the PG pin unconnected when not used.

UNDER VOLTAGE LOCKOUT

To avoid mis-operation of the device at low input voltages, an under voltage lockout is implemented, that shuts down the device at voltages lower than V_{UVLO} with a V_{HYS_UVLO} hysteresis.

THERMAL SHUTDOWN

The device goes into thermal shutdown once the junction temperature exceeds typically T_{JSD}. Once the device temperature falls below the threshold the device returns to normal operation automatically.

INDUCTOR CURRENT LIMIT

The Inductor Current Limit prevents the device from high inductor current and drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted/saturated inductor or a heavy load/shorted output circuit condition.

The incorporated inductor peak current limit measures the current during the high side and low side power MOSFET on-phase in PWM mode. Once the high side switch current limit is tripped, the high side MOSFET is turned off and the low side MOSFET is turned on to reduce the inductor current. Until the inductor current drops down to low side switch current limit, the low side MOSFET is turned off and the high side switch is turned on again. This operation repeats until the inductor current does not reach the high side switch current limit. Due to the internal propagation delay, the real current limit value can exceed the static current limit in the electrical characteristics table.

APPLICATION INFORMATION

Output Filter Design

The inductor and the output capacitor together provide a low pass frequency filter. To simplify this process Table 3 outlines possible inductor and capacitor value combinations for the most application.

Table 3. Matrix of Output Capacitor / Inductor Combinations

L [µH](1)	C_{OUT} [µF](1)				
	10	22	47	100	150
0.47					
1	+	+(2)(3)	+	+	
2.2	+	+	+	+	
4.7					

(1) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by+20% and -50%. Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
(2) Plus mark indicates recommended filter combinations.
(3) Filter combination in typical application.

Inductor Selection

Main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, Equation 4 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (2)$$

Where

$I_{OUT,MAX}$ = Maximum output current
ΔI_L = Inductor current ripple
f_{SW} = Switching frequency
L = Inductor value

It's recommended to choose the saturation current for the inductor 20%~30% higher than the $I_{L,MAX}$, out of Equation 4. A higher inductor value is also useful to lower ripple current, but will increase the transient response time as well. The following inductors are recommended to be used in designs.

Table 4. List of Recommended Inductors

INDUCTANCE [µH]	CURRENT RATING [mA]	DIMENSIONS L x W x H [mm^3]	DC RESISTANCE [mΩ typ]	TYPE	MANUFACTURER
1.0	2500	3 x 3 x 1.2	35	XFL3012-102ME	Coilcraft
1.0	1650	3 x 3 x 1.2	40	LQH3NPN1R0NJ0	Murata
2.2	2500	4 x 3.7 x 1.65	49	LQH44PN2R2MP0	Murata
2.2	1600	3 x 3 x 1.2	81	XFL3012-222ME	Coilcraft

Capacitor Selection

The input capacitor is the low impedance energy source for the converter which helps to provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between VIN and PGND as close as possible to that pins. For most applications 10µF will be sufficient, a larger value reduces input current ripple.

The architecture of the TPS6208X allows to use tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its resistance up to high frequencies and to get narrow capacitance variation with temperature, it's recommended to use X7R or X5R dielectric. The TPS6208x is designed to operate with an output capacitance of 10µF to 100µF, as outlined in Table 3.

Table 5. List of Recommended Capacitors

CAPACITANCE [µF]	TYPE	DIMENSIONS L x W x H [mm^3]	MANUFACTURER
10	GRM188R60J106M	0603: 1.6 x 0.8 x 0.8	Murata
22	GRM188R60G226M	0603: 1.6 x 0.8 x 0.8	Murata
22	GRM21BR60J226M	0805: 2.0 x 1.2 x 1.25	Murata

Setting the Output Voltage

The TPS608x devices are available as fixed and adjustable output voltage versions. The fixed versions are internally programmed to a fixed output voltage, whereas the adjustable output voltage version needs to be programmed via an external voltage divider to set the desired output voltage.

Adjustable output voltage version

For the adjustable output voltage version, an external resistor divider is used. By selecting R_1 and R_2, the output voltage is programmed to the desired value.

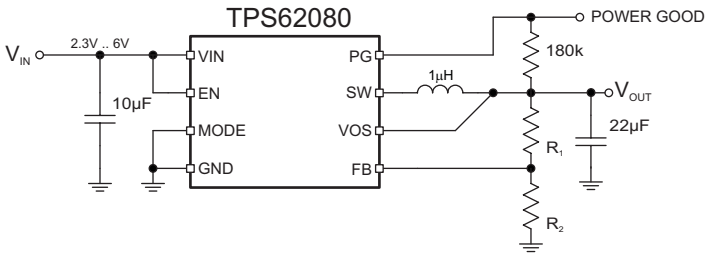


Figure 31. Typical Application Circuit for Adjustable Output Voltage Option

When the output voltage is regulated, the typical voltage at the FB pin is V_{FB} for the adjustable devices. The following equation can be used to calculate R_1 and R_2.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.45V \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

For best accuracy, R2 should be kept smaller than 40kΩ to ensure that the current flowing through R2 is at least 100 times larger than I_{FB}. Changing the sum towards a lower value increases the robustness against noise injection. Changing the sum towards higher values reduces the quiescent current and supports the Snooze Mode function for achieving highest efficiency at low load currents. For lowest quiescent current during the Snooze Mode, it is recommended to use a fixed output voltage version like TPS62081 and TPS62082.

PCB Layout

The PCB layout is an important step to maintain the high performance of the TPS6208x devices.

The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the traces short. Routing these traces direct and wide results in low trace resistance and low parasitic inductance. A common power GND should be used. The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.

The sense traces connected to FB and VOS pins are signal traces. Special care should be taken to avoid noise being induced. By a direct routing, parasitic inductance can be kept small. GND layers might be used for shielding. Keep these traces away from SW nodes.

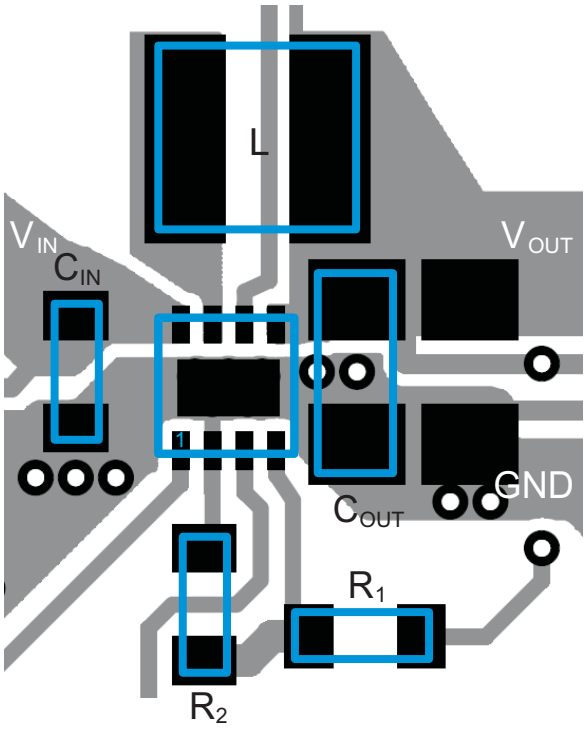


Figure 32. PCB Layout Suggestion

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the ThermalPAD™
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Notes SZZA017 and SPRA953.

APPLICATION EXAMPLES

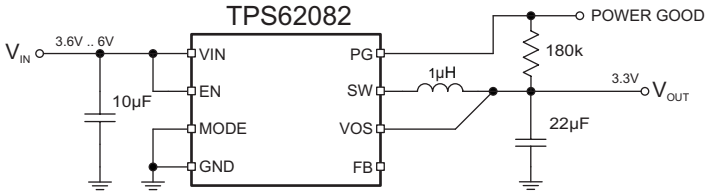


Figure 33. 3.3V Fixed Output Voltage Application (TPS62082)

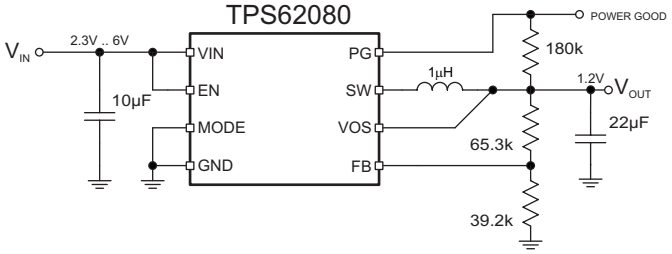


Figure 34. 1.2V Output Voltage Application (TPS62080)

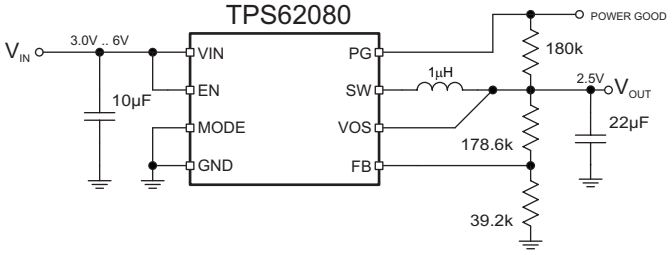


Figure 35. 2.5V Output Voltage Application (TPS62080)

REVISION HISTORY

Changes from Original (September 2011) to Revision A **Page**

- Added TPS62080A device 1
- Added TPS62080ADSG (Product Preview) and TPS62080ADGN (Product Preview) to ORDERING INFORMATION 2
- Added TPS62080A output discharge resistor 3

Changes from Revision A (February 2012) to Revision B **Page**

- Changed TPS62080ADSG from Product Preview to Production Data in ORDERING INFORMATION 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62080DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVR	Samples
TPS62080DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVR	Samples
TPS62081DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVS	Samples
TPS62081DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVS	Samples
TPS62082DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVT	Samples
TPS62082DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

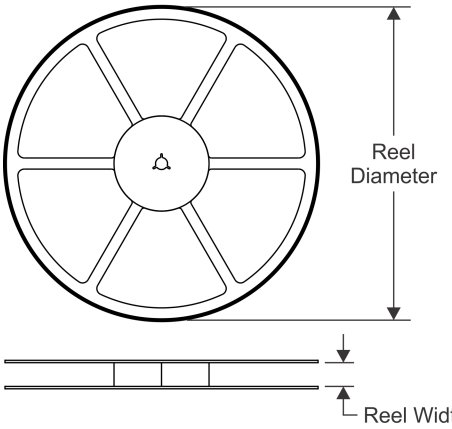
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

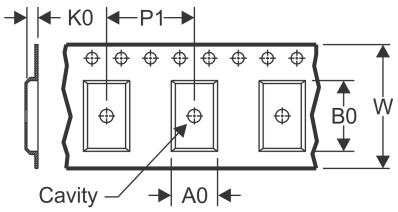
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

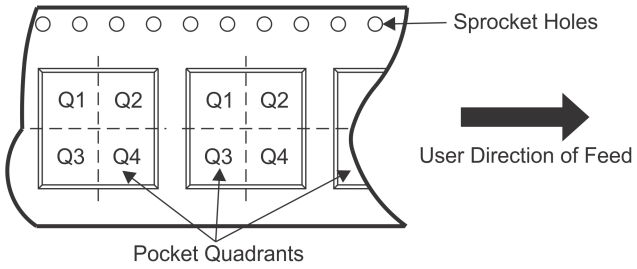


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

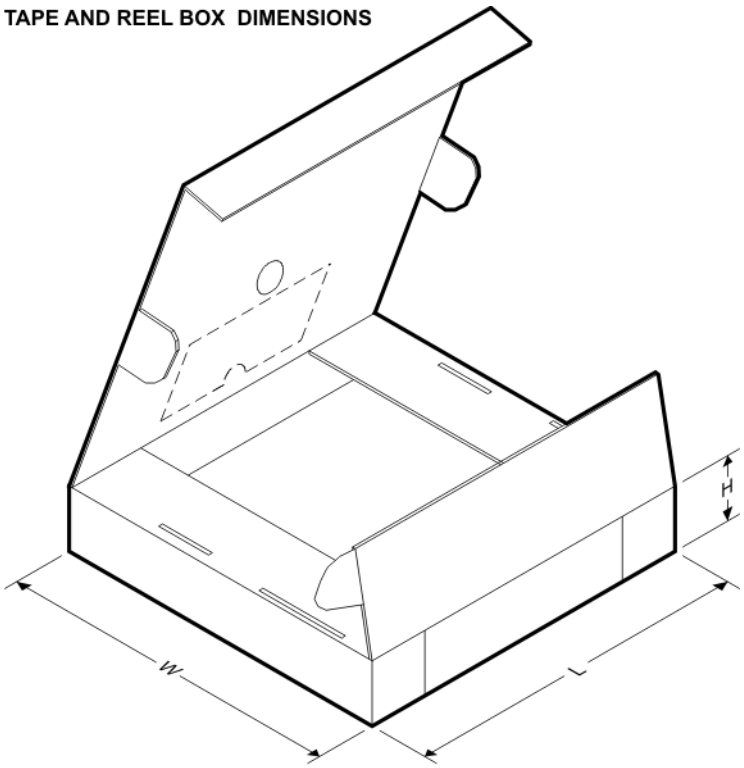
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62080DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62080DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62080DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62080DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62081DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62081DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62082DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62082DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62082DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62082DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

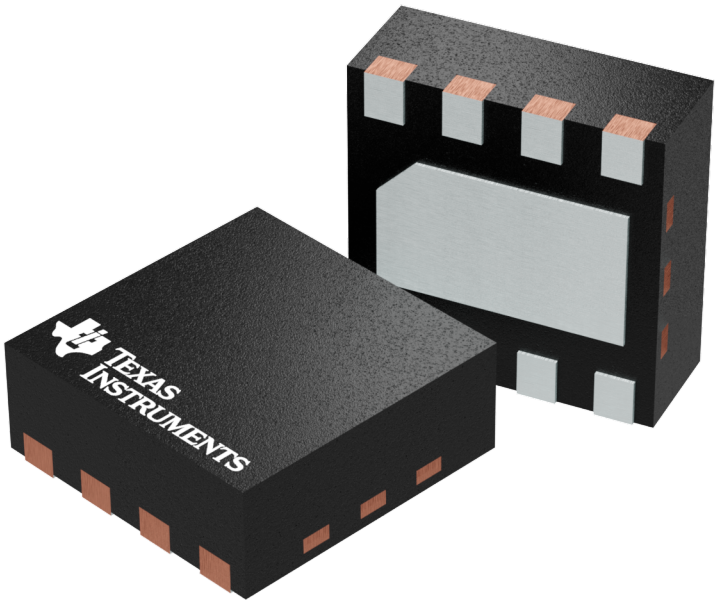


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62080DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
TPS62080DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62080DSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62080DSGT	WSON	DSG	8	250	195.0	200.0	45.0
TPS62081DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62081DSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62082DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
TPS62082DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62082DSGT	WSON	DSG	8	250	195.0	200.0	45.0
TPS62082DSGT	WSON	DSG	8	250	205.0	200.0	33.0

DSG 8 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



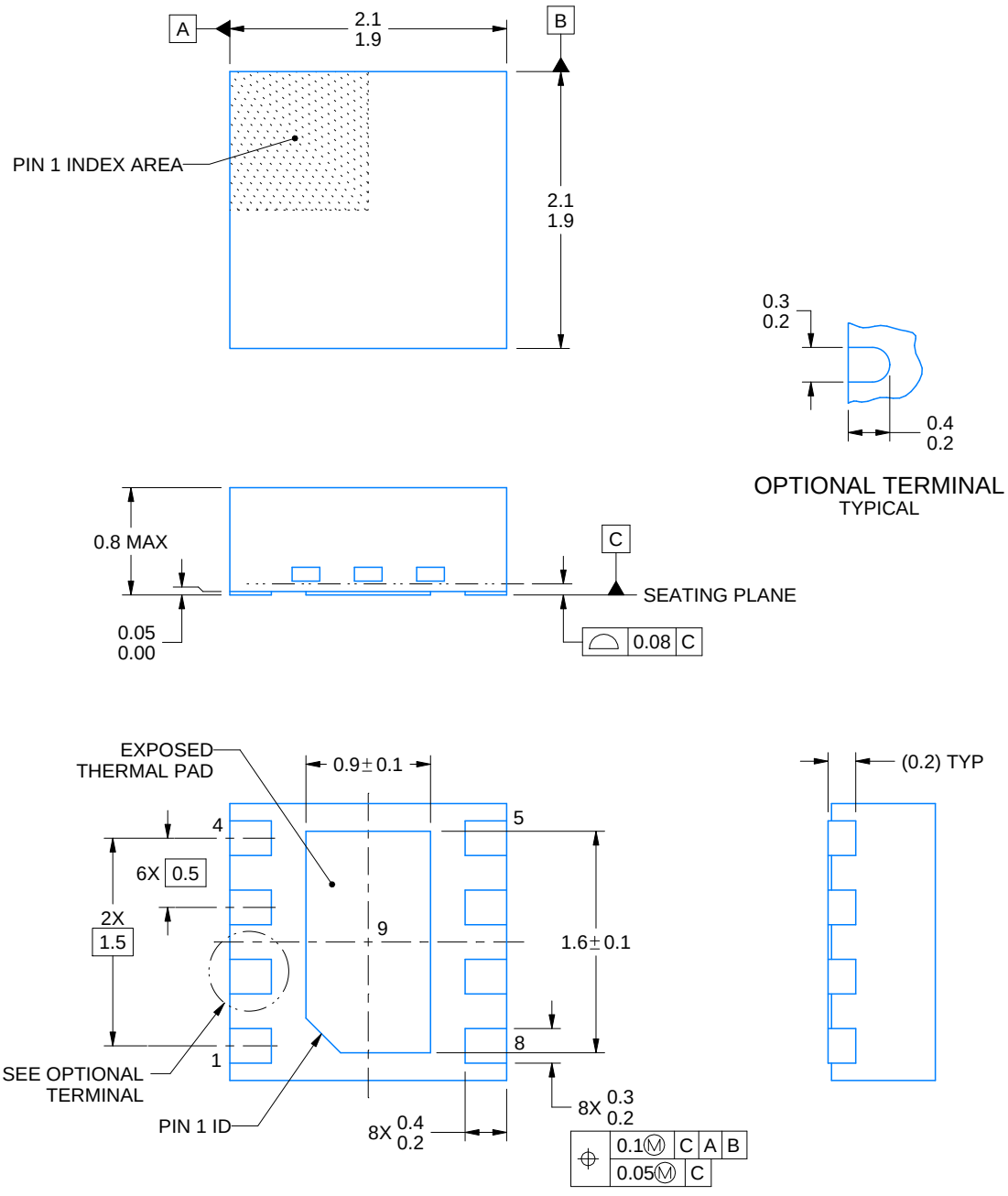
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DSG0008A

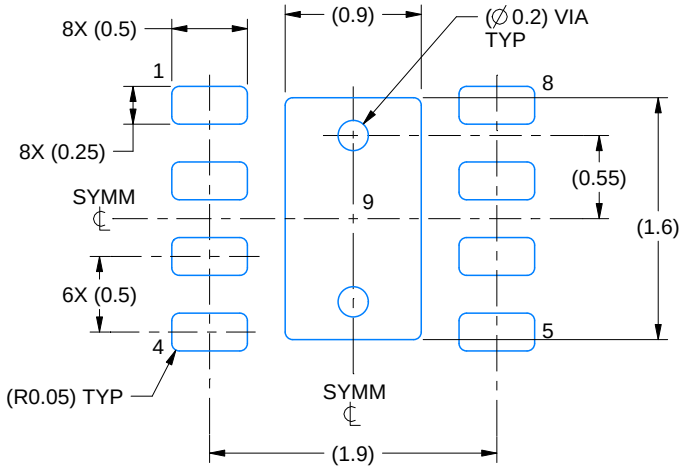
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

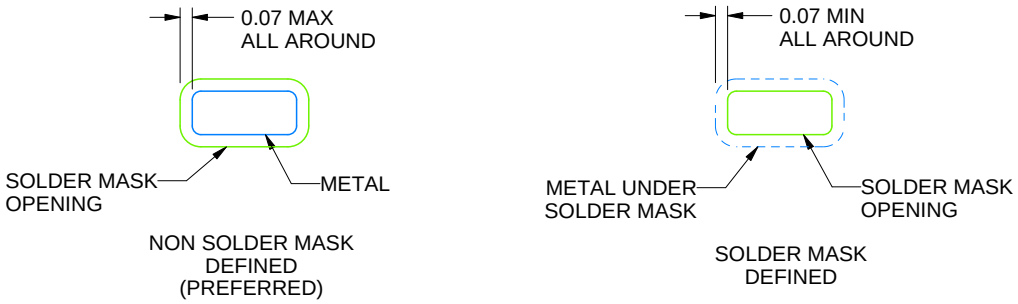


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

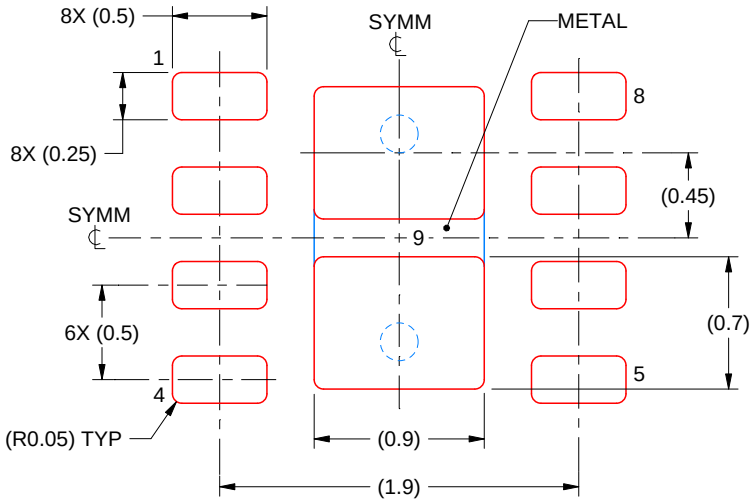


SOLDER MASK DETAILS

4218900/B 09/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/B 09/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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