

# LMR14203 SIMPLE SWITCHER® 42Vin, 0.3A Step-Down Voltage Regulator in SOT-23

Check for Samples: [LMR14203](#)

## FEATURES

- Input Voltage Range of 4.5V to 42V
- Output Voltage Range of 0.765V to 34V
- Output Current up to 0.3A
- 1.25 MHz Switching Frequency
- Low Shutdown Iq, 16  $\mu$ A Typical
- Short Circuit Protected
- Internally Compensated
- Soft-Start Function
- Thin SOT-23-6 Package (2.97 x 1.65 x 1mm)
- Fully Enabled for WEBENCH® Power Designer

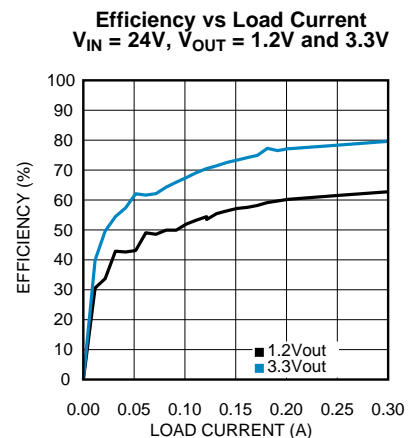
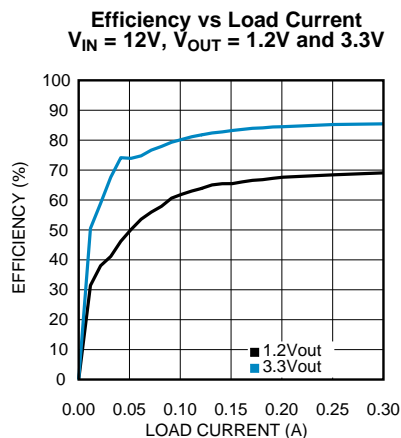
## PERFORMANCE BENEFITS

- Tight Accuracy for Powering Digital ICs
- Extremely Easy to Use
- Tiny Overall Solution Reduces System Cost

## APPLICATIONS

- Point-of-Load Conversions from 5V, 12V, and 24V Rails
- Space Constrained Applications
- Battery Powered Equipment
- Industrial Distributed Power Applications
- Power Meters
- Portable Hand-Held Instruments

## System Performance



## DESCRIPTION

The LMR14203 is a PWM DC/DC buck (step-down) regulator. With a wide input range from 4.5V-42V, it is suitable for a wide range of applications such as power conditioning from unregulated sources. They feature a low  $R_{DS(ON)}$  (0.9 $\Omega$  typical) internal switch for maximum efficiency (85% typical). Operating frequency is fixed at 1.25 MHz allowing the use of small external components while still being able to have low output voltage ripple. Soft-start can be implemented using the shutdown pin with an external RC circuit allowing the user to tailor the soft-start time to a specific application.

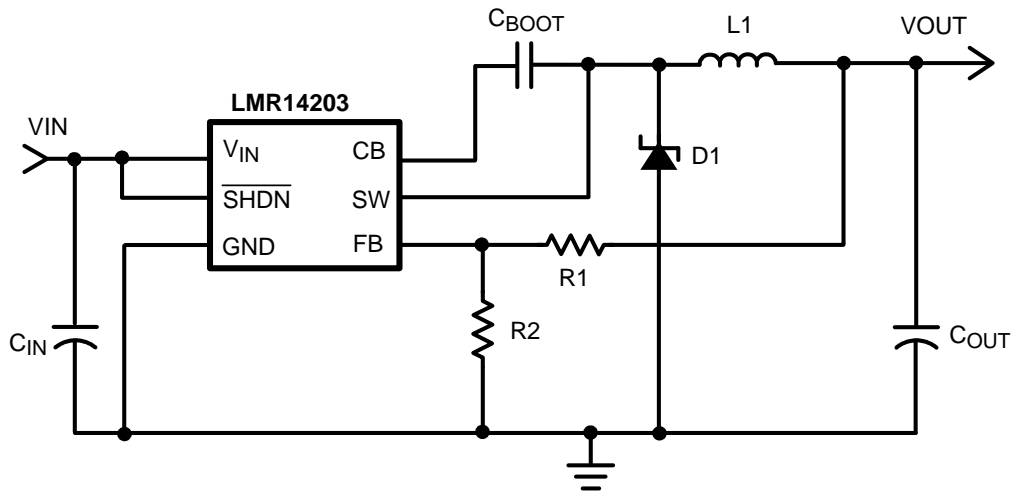
The LMR14203 is optimized for up to 300 mA load current.

Additional features include: thermal shutdown,  $V_{IN}$  under-voltage lockout, and gate drive under-voltage lockout. The LMR14203 is available in a low profile SOT-6L package.



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Connection Diagram

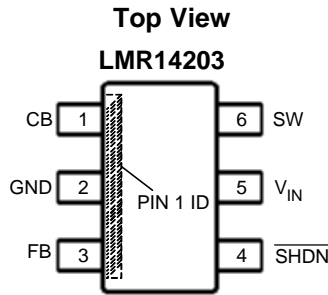


Figure 1. 6 Lead SOT Package  
See Package Number DDC0006A

Pin Descriptions

Pin	Name	Function
1	CB	SW FET gate bias voltage. Connect C <sub>BOOT</sub> cap between CB and SW.
2	GND	Ground connection.
3	FB	Feedback pin: Set feedback voltage divider ratio with $V_{OUT} = V_{FB} (1+(R1/R2))$ . Resistors should be in the 100-10K range to avoid input bias errors.
4	SHDN	Logic level shutdown input. Pull to GND to disable the device and pull high to enable the device. If this function is not used tie to V <sub>IN</sub> or leave open.
5	V <sub>IN</sub>	Power input voltage pin: 4.5V to 42V normal operating range.
6	SW	Power FET output: Connect to inductor, diode, and C <sub>BOOT</sub> cap.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings<sup>(1)(2)</sup>**

$V_{IN}$	-0.3V to +45V
$\overline{SHDN}$	-0.3V to $(V_{IN}+0.3V) < 45V$
SW Voltage	-0.3V to +45V
CB Voltage above SW Voltage	7V
FB Voltage	-0.3V to +5V
Maximum Junction Temperature	150°C
Power Dissipation <sup>(3)</sup>	Internally Limited
For soldering specifications: <a href="http://www.ti.com/lit/SNOA549">http://www.ti.com/lit/SNOA549</a>	
ESD Susceptibility <sup>(4)</sup> Human Body Model	1.5 kV

- (1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For ensured specifications and test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_{J(MAX)}$ , the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation at any ambient temperature is calculated using:  $P_D (MAX) = (T_{J(MAX)} - T_A)/\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at  $T_J=175^\circ\text{C}$  (typ.) and disengages at  $T_J=155^\circ\text{C}$  (typ.).
- (4) Human Body Model, applicable std. JESD22-A114-C.

**Operating Conditions**

Operating Junction Temperature Range <sup>(1)</sup>	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Input Voltage $V_{IN}$	4.5V to 42V
SW Voltage	Up to 42V

- (1) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

## Electrical Characteristics

Specifications in standard type face are for  $T_J = 25^\circ\text{C}$  and those with **boldface type** apply over the full **Operating Temperature Range** ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ). Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = +25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise stated the following conditions apply:  $V_{IN} = 12\text{V}$ .

Parameter		Test Conditions	Min <sup>(1)</sup>	Typ <sup>(2)</sup>	Max <sup>(1)</sup>	Units
$I_Q$	Quiescent current	$\overline{\text{SHDN}} = 0\text{V}$		16	<b>40</b>	$\mu\text{A}$
		Device On, Not Switching		1.30	<b>1.75</b>	mA
		Device On, No Load		1.35	<b>1.85</b>	
$R_{\text{DS(ON)}}$	Switch ON resistance	See <sup>(3)</sup>		0.9	<b>1.6</b>	$\Omega$
$I_{\text{LSW}}$	Switch leakage current	$V_{IN} = 42\text{V}$		0.0	0.5	$\mu\text{A}$
$I_{\text{CL}}$	Switch current limit	See <sup>(4)</sup>		525		mA
$I_{\text{FB}}$	Feedback pin bias current	See <sup>(5)</sup>		0.1	1.0	$\mu\text{A}$
$V_{\text{FB}}$	FB Pin reference voltage		<b>0.747</b>	0.765	<b>0.782</b>	V
$t_{\text{MIN}}$	Minimum ON time			100		ns
$f_{\text{SW}}$	Switching frequency	$V_{\text{FB}} = 0.5\text{V}$	<b>0.95</b>	1.25	<b>1.50</b>	MHz
		$V_{\text{FB}} = 0\text{V}$		0.35		
$D_{\text{MAX}}$	Maximum duty cycle		<b>81</b>	87		%
$V_{\text{UVP}}$	Undervoltage lockout thresholds	On threshold	<b>4.4</b>	3.7		V
		Off threshold		3.5	<b>3.25</b>	
$V_{\text{SHDN}}$	Shutdown threshold	Device on	<b>2.3</b>	1.0		V
		Device off		0.9	<b>0.3</b>	
$I_{\text{SHDN}}$	Shutdown pin input bias current	$V_{\text{SHDN}} = 2.3\text{V}^{(5)}$		0.05	<b>1.5</b>	$\mu\text{A}$
		$V_{\text{SHDN}} = 0\text{V}$		0.02	<b>1.5</b>	
<b>THERMAL SPECIFICATIONS</b>						
$R_{\theta\text{JA}}$	Junction-to-Ambient Thermal Resistance, SOT-6L Package	See <sup>(6)</sup>		121		$^\circ\text{C/W}$

- (1) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
- (2) Typical numbers are at  $25^\circ\text{C}$  and represent the most likely norm.
- (3) Includes the bond wires,  $R_{\text{DS(ON)}}$  from  $V_{IN}$  pin to SW pin.
- (4) Current limit at 0% duty cycle.
- (5) Bias currents flow into pin.
- (6) All numbers apply for packages soldered directly onto a 3" x 3" PC board with 2 oz. copper on 4 layers in still air in accordance to JEDEC standards. Thermal resistance varies greatly with layout, copper thickness, number of layers in PCB, power distribution, number of thermal vias, board size, ambient temperature, and air flow.

### Typical Performance Characteristics

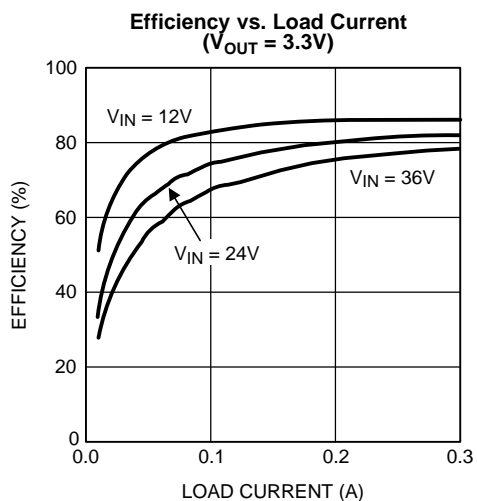


Figure 2.

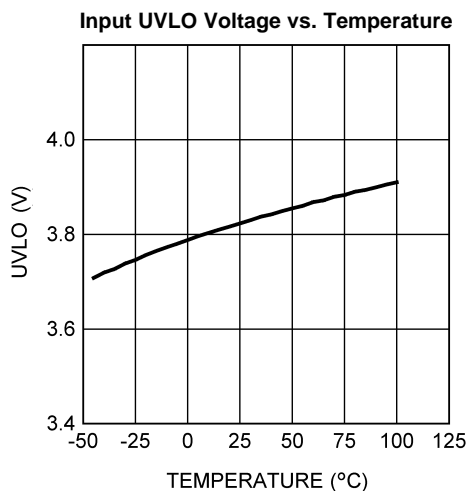


Figure 3.

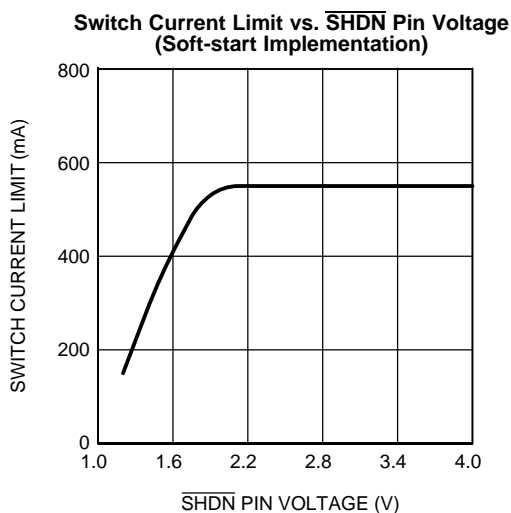


Figure 4.

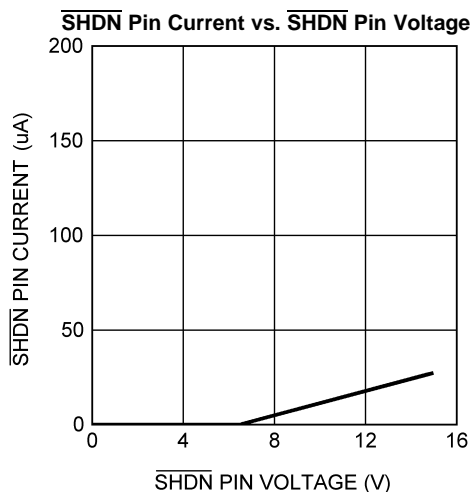
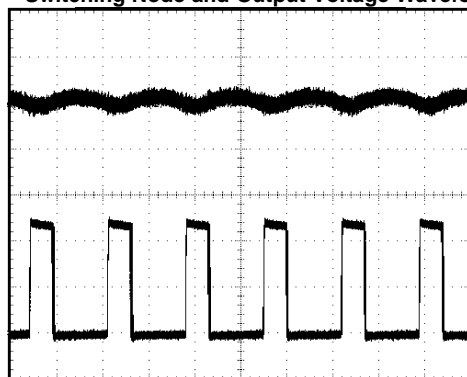


Figure 5.

### Switching Node and Output Voltage Waveforms

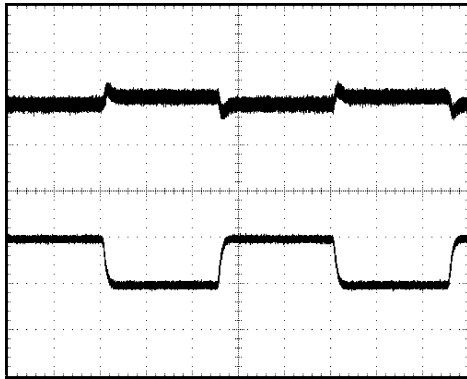


$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $I_{OUT} = 200\text{ mA}$   
 Top trace:  $V_{OUT}$ , 10 mV/div, AC Coupled  
 Bottom trace: SW, 5V/div, DC Coupled  
 T = 1  $\mu\text{s}$ /div

Figure 6.

**Typical Performance Characteristics (continued)**

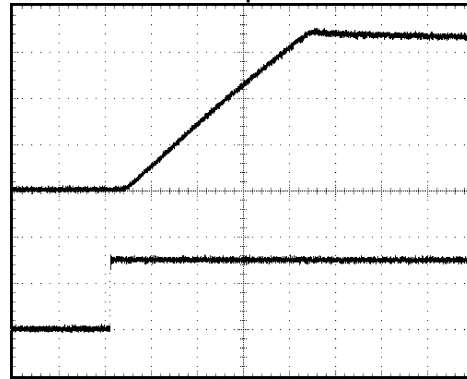
**Load Transient Waveforms**



$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $I_{OUT} = 300\text{ mA}$  to  $200\text{ mA}$  to  $300\text{ mA}$   
 Top trace:  $V_{OUT}$ , 20 mV/div, AC Coupled  
 Bottom trace:  $I_{OUT}$ , 100 mA/div, DC Coupled  
 $T = 200\ \mu\text{s/div}$

**Figure 7.**

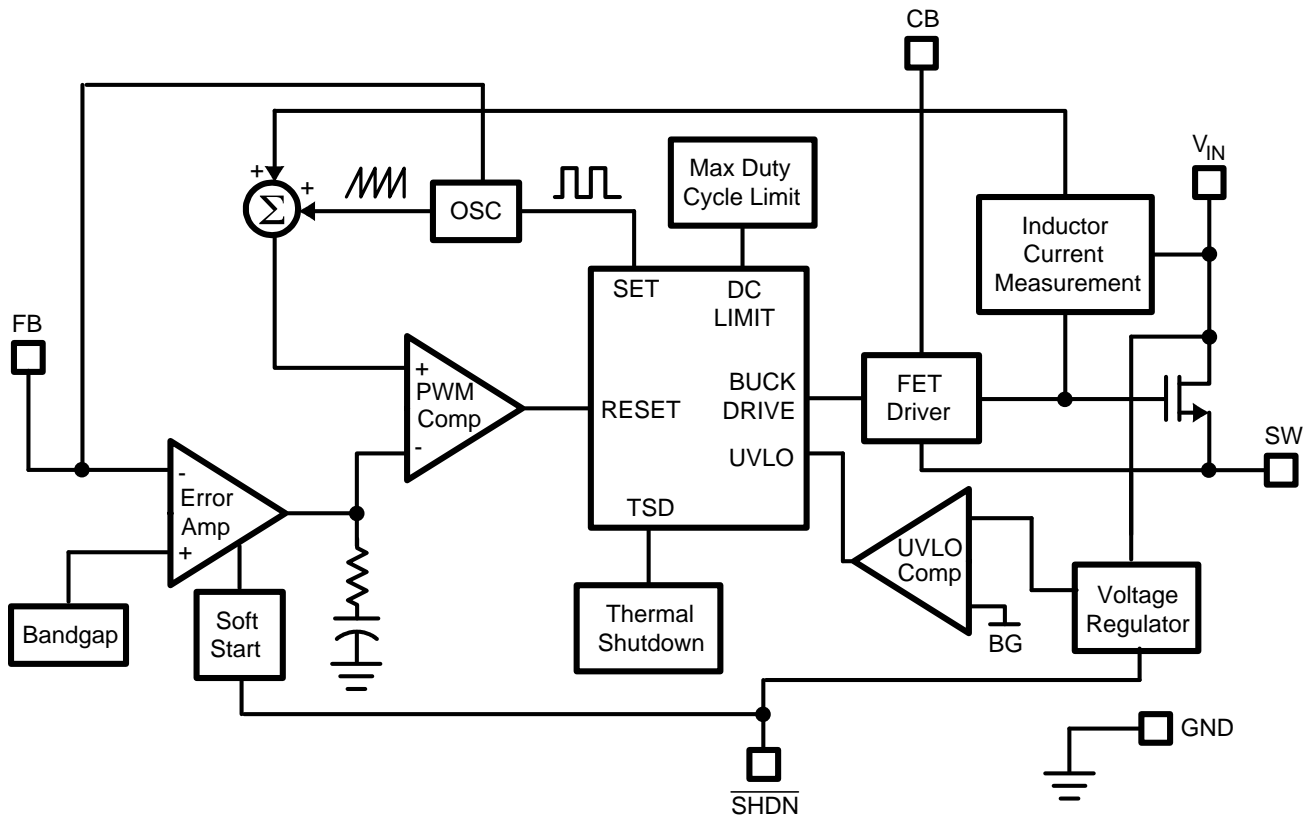
**Start-Up Waveform**



$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $I_{OUT} = 50\text{ mA}$   
 Top trace:  $V_{OUT}$ , 1V/div, DC Coupled  
 Bottom trace:  $SHDN$ , 2V/div, DC Coupled  
 $T = 40\ \mu\text{s/div}$

**Figure 8.**

**Block Diagram**



## APPLICATION INFORMATION

### Protection

The LMR14203 has dedicated protection circuitry running during normal operation to protect the IC. The thermal shutdown circuitry turns off the power device when the die temperature reaches excessive levels. The UVLO comparator protects the power device during supply power startup and shutdown to prevent operation at voltages less than the minimum input voltage. A gate drive (CB) under-voltage lockout is included to ensure that there is enough gate drive voltage to drive the MOSFET before the device tries to start switching. The LMR14203 also features a shutdown mode decreasing the supply current to approximately 16  $\mu$ A.

### Continuous Conduction Mode

The LMR14203 contains a current-mode, PWM buck regulator. A buck regulator steps the input voltage down to a lower output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the buck regulator operates in two cycles. The power switch is connected between  $V_{IN}$  and SW. In the first cycle of operation the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by  $C_{OUT}$  and the rising current through the inductor. During the second cycle the transistor is open and the diode is forward biased due to the fact that the inductor current cannot instantaneously change direction. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as:

$$D = V_{OUT}/V_{IN} \text{ and } D' = (1-D)$$

where

- D is the duty cycle of the switch. (1)

D and D' will be required for design calculations.

### Design Procedure

This section presents guidelines for selecting external components.

#### Setting the Output Voltage

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown on the front page schematic. The feedback pin voltage is 0.765V, so the ratio of the feedback resistors sets the output voltage according to the following equation:

$$V_{OUT} = 0.765V(1 + (R1/R2)) \quad (2)$$

Typically R2 will be given as 100 $\Omega$ -10 k $\Omega$  for a starting value. To solve for R1 given R2 and  $V_{OUT}$  use  $R1 = R2((V_{OUT}/0.765V) - 1)$ .

#### Input Capacitor

A low ESR ceramic capacitor ( $C_{IN}$ ) is needed between the  $V_{IN}$  pin and GND pin. This capacitor prevents large voltage transients from appearing at the input. Use a 2.2  $\mu$ F-10  $\mu$ F value with X5R or X7R dielectric. Depending on construction, a ceramic capacitor's value can decrease up to 50% of its nominal value when rated voltage is applied. Consult with the capacitor manufacturer's data sheet for information on capacitor derating over voltage and temperature.

#### Inductor Selection

The most critical parameters for the inductor are the inductance, peak current, and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input and the output voltages.

$$L = \frac{(V_{IN} - V_{OUT})V_{OUT}}{V_{IN} \times I_{RIPPLE} \times f_{SW}} \quad (3)$$

A higher value of ripple current reduces inductance, but increases the conduction loss, core loss, and current stress for the inductor and switch devices. It also requires a bigger output capacitor for the same output voltage ripple requirement. A reasonable value is setting the ripple current to be 30% of the DC output current. Since the ripple current increases with the input voltage, the maximum input voltage is always used to determine the inductance. The DC resistance of the inductor is a key parameter for the efficiency. Lower DC resistance is

available with a bigger winding area. A good tradeoff between the efficiency and the core size is letting the inductor copper loss equal 2% of the output power. See AN-1197 [SNVA038](#) for more information on selecting inductors. A good starting point for most applications is a 10  $\mu\text{H}$  to 22  $\mu\text{H}$  with a 0.7A or greater current rating for the LMR14203. Using such a rating will enable the LMR14203 to current limit without saturating the inductor. This is preferable to the device going into thermal shutdown mode and the possibility of damaging the inductor if the output is shorted to ground or other longterm overload.

### Output Capacitor

The selection of  $C_{\text{OUT}}$  is driven by the maximum allowable output voltage ripple. The output ripple in the constant frequency, PWM mode is approximated by:

$$V_{\text{RIPPLE}} = I_{\text{RIPPLE}}(\text{ESR} + (1/(8f_{\text{SW}}C_{\text{OUT}}))) \quad (4)$$

The ESR term usually plays the dominant role in determining the voltage ripple. Low ESR ceramic capacitors are recommended. Capacitors in the range of 22  $\mu\text{F}$ -100  $\mu\text{F}$  are a good starting point with an ESR of 0.1 $\Omega$  or less.

### Bootstrap Capacitor

A 0.15  $\mu\text{F}$  ceramic capacitor or larger is recommended for the bootstrap capacitor ( $C_{\text{BOOT}}$ ). For applications where the input voltage is less than twice the output voltage a larger capacitor is recommended, generally 0.15  $\mu\text{F}$  to 1  $\mu\text{F}$  to ensure plenty of gate drive for the internal switches and a consistently low  $R_{\text{DS(ON)}}$ .

### Soft-Start Components

The LMR14203 has circuitry that is used in conjunction with the  $\overline{\text{SHDN}}$  pin to limit the inrush current on start-up of the DC/DC switching regulator. The  $\overline{\text{SHDN}}$  pin in conjunction with a RC filter is used to tailor the soft-start for a specific application. When a voltage applied to the  $\overline{\text{SHDN}}$  pin is between 0V and up to 2.3V it will cause the cycle by cycle current limit in the power stage to be modulated for minimum current limit at 0V up to the rated current limit at 2.3V. Thus controlling the output rise time and inrush current at startup. The resistor value should be selected so the current sourced into the  $\overline{\text{SHDN}}$  pin will be greater than the leakage current of the  $\overline{\text{SHDN}}$  pin (1.5  $\mu\text{A}$ ) when the voltage at  $\overline{\text{SHDN}}$  is equal or greater than 2.3V.

### Shutdown Operation

The  $\overline{\text{SHDN}}$  pin of the LMR14203 is designed so that it may be controlled using 2.3V or higher logic signals. If the shutdown function is not to be used the  $\overline{\text{SHDN}}$  pin may be tied to  $V_{\text{IN}}$ . The maximum voltage to the  $\overline{\text{SHDN}}$  pin should not exceed 42V. If the use of a higher voltage is desired due to system or other constraints it may be used, however a 100 k $\Omega$  or larger resistor is recommended between the applied voltage and the  $\overline{\text{SHDN}}$  pin to protect the device.

### SCHOTTKY Diode

The breakdown voltage rating of the diode (D1) is preferred to be 25% higher than the maximum input voltage. The current rating for the diode should be equal to the maximum output current for best reliability in most applications. In cases where the duty cycle is greater than 50%, the average diode current is lower. In this case it is possible to use a diode with a lower average current rating, approximately  $(1-D)I_{\text{OUT}}$ , however the peak current rating should be higher than the maximum load current. A 0.5A to 1A rated diode is a good starting point.

### Layout Considerations

To reduce problems with conducted noise pick up, the ground side of the feedback network should be connected directly to the GND pin with its own connection. The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor to minimize coupling noise into the feedback pin. The input bypass capacitor  $C_{\text{IN}}$  must be placed close to the  $V_{\text{IN}}$  pin. This will reduce copper trace resistance which effects input voltage ripple of the IC. The inductor L1 should be placed close to the SW pin to reduce EMI and capacitive coupling. The output capacitor,  $C_{\text{OUT}}$  should be placed close to the junction of L1 and the diode D1. The L1, D1, and  $C_{\text{OUT}}$  trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency. The ground connection for the diode,  $C_{\text{IN}}$ , and  $C_{\text{OUT}}$  should be as small as possible and tied to the system ground plane in only one spot (preferably at the  $C_{\text{OUT}}$  ground point) to minimize conducted noise in the system ground plane. For more detail on switching power supply layout considerations see Application Note AN-1149: *Layout Guidelines for Switching Power Supplies* [SNVA021](#).



Typical Applications

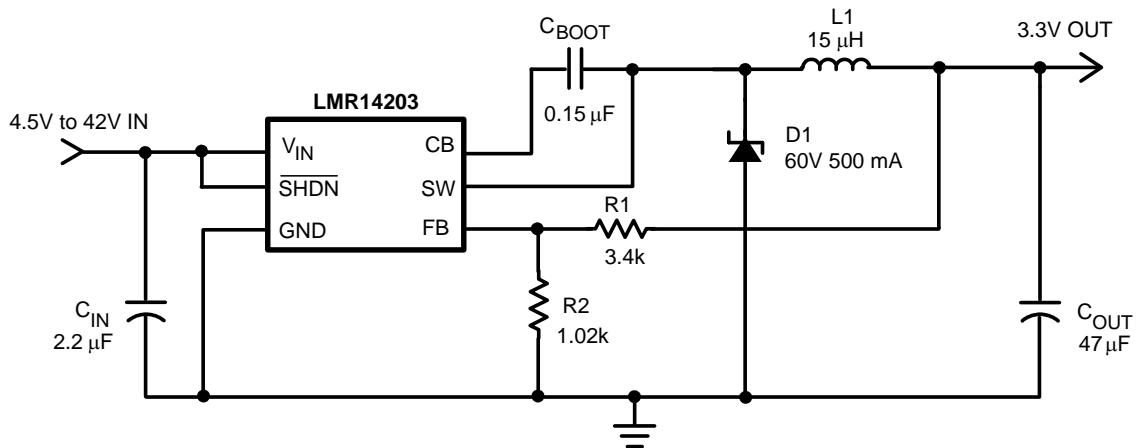


Figure 9. Application Circuit, 3.3V Output

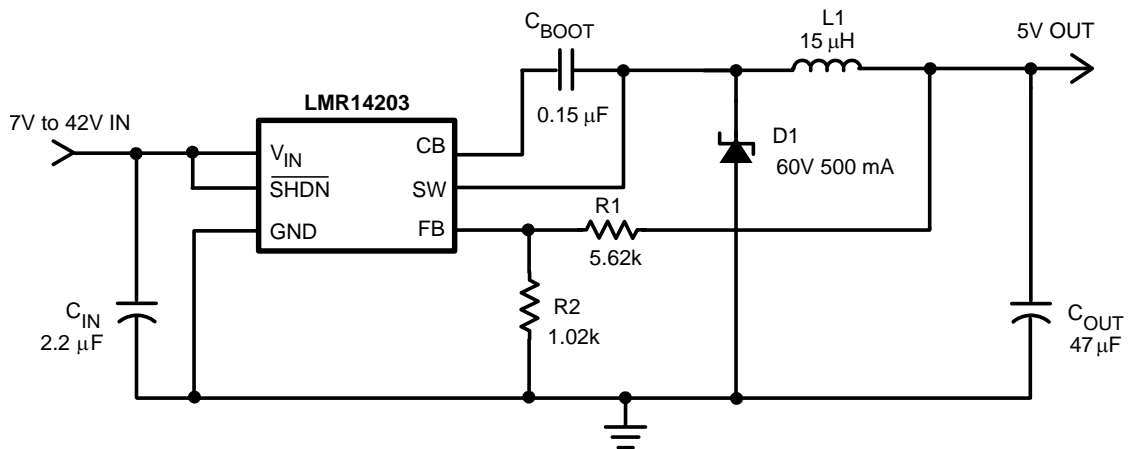


Figure 10. Application Circuit, 5V Output

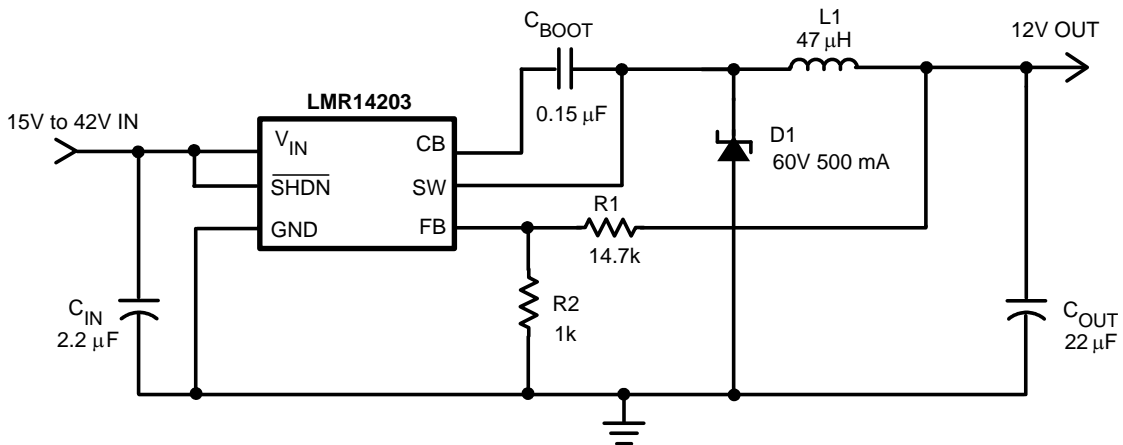


Figure 11. Application Circuit, 12V Output

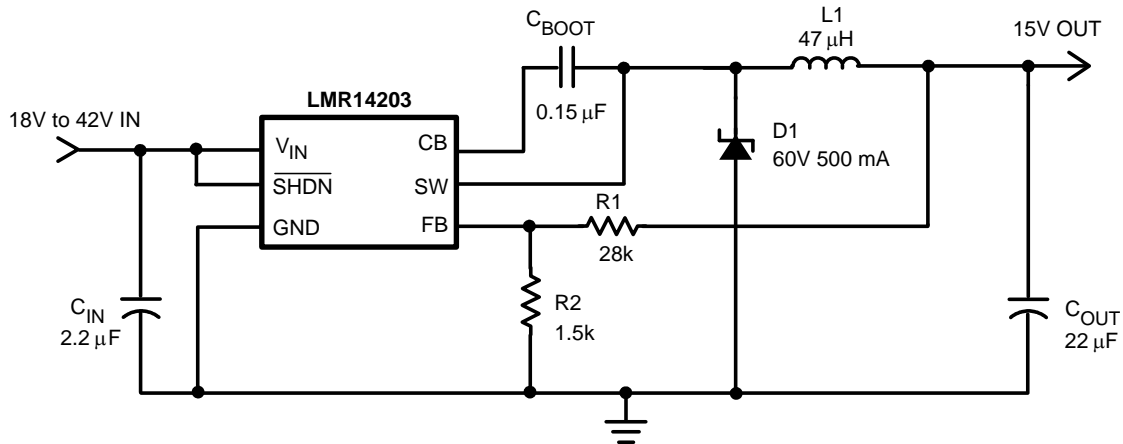


Figure 12. Application Circuit, 15V Output

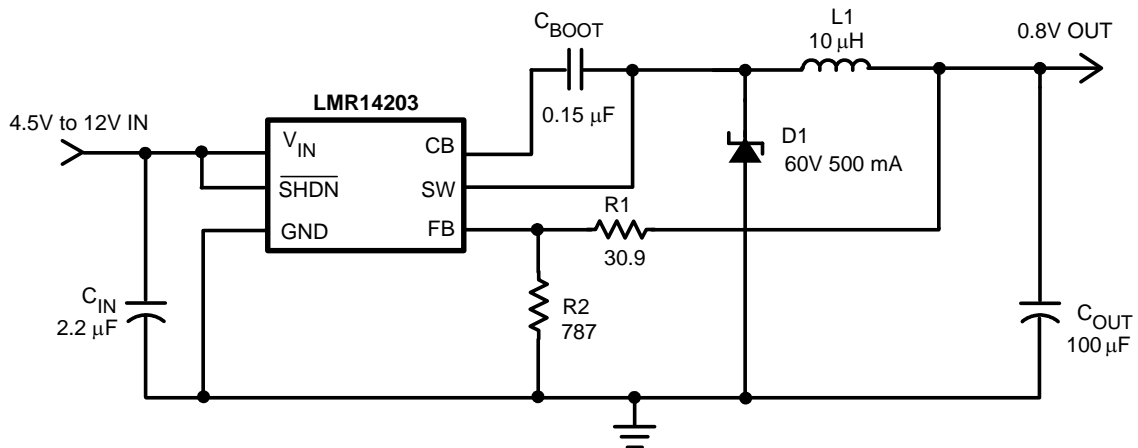


Figure 13. Application Circuit, 0.8V Output

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**REVISION HISTORY**

<b>Changes from Revision B (April 2013) to Revision C</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format .....	<a href="#">10</a>

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR14203XMK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SJ3B	<a href="#">Samples</a>
LMR14203XMKE/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SJ3B	<a href="#">Samples</a>
LMR14203XMKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SJ3B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



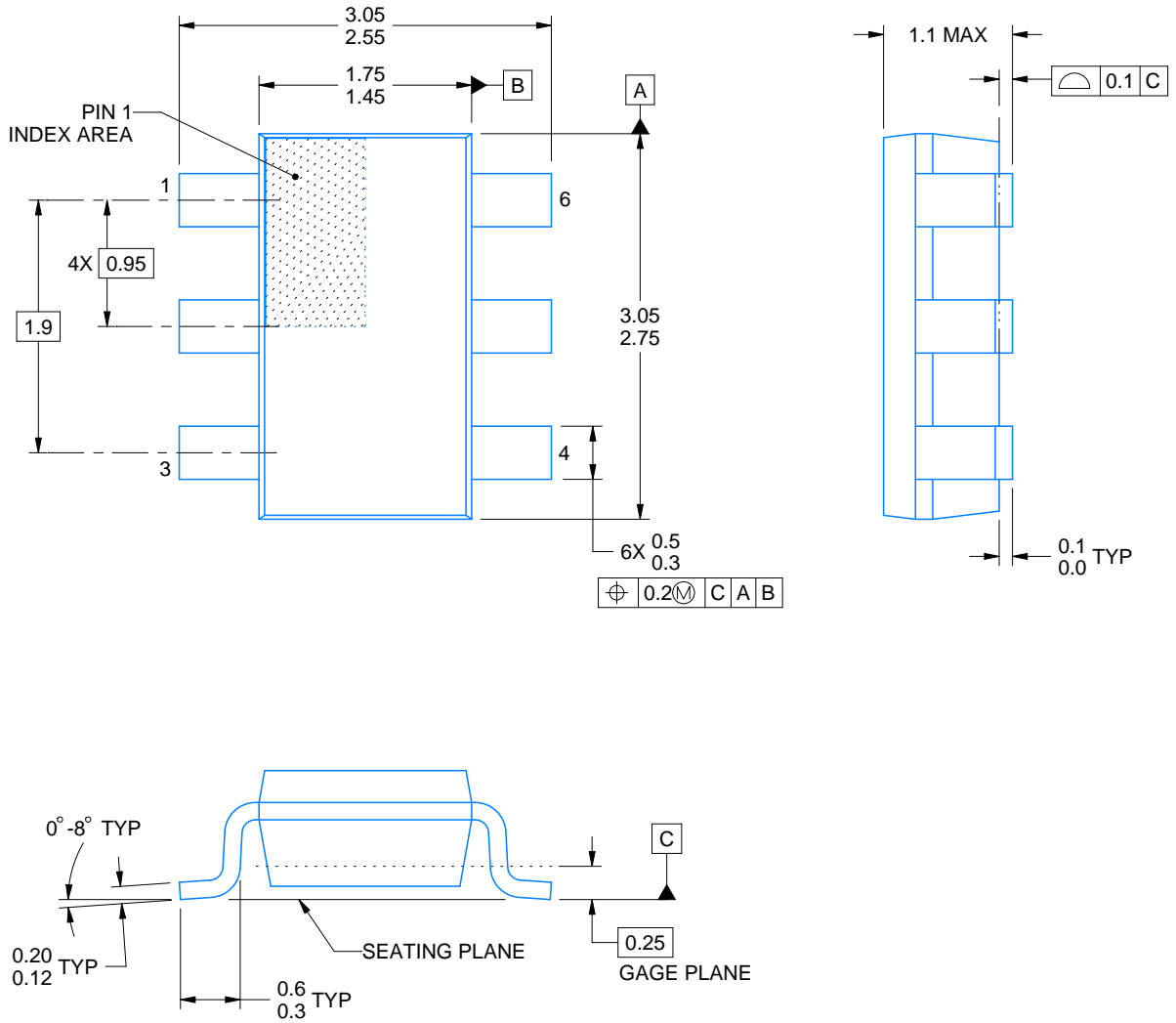
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR14203XMK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR14203XMKE/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR14203XMKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR14203XMK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LMR14203XMKE/NOPB	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LMR14203XMKX/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0

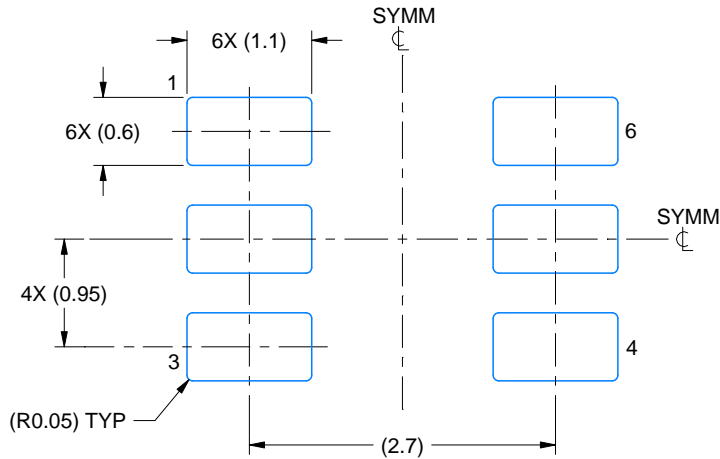


4214841/A 08/2016

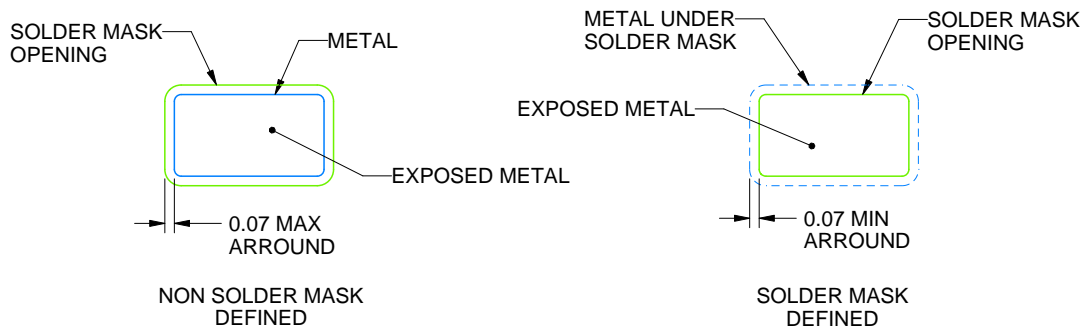
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.





LAND PATTERN EXAMPLE  
EXPLODED METAL SHOWN  
SCALE:15X

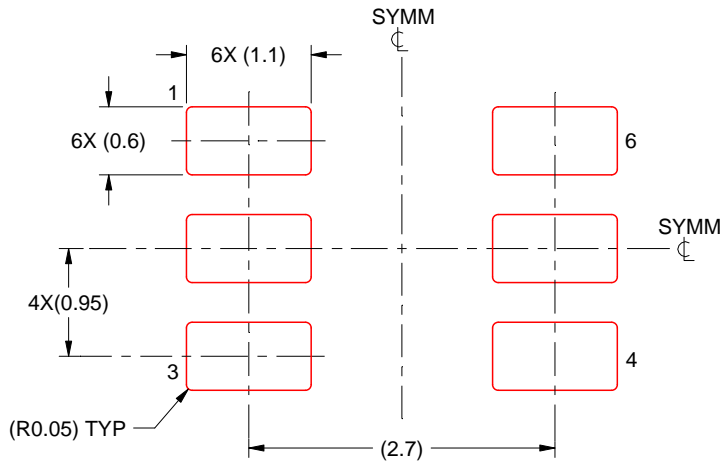


SOLDEMASK DETAILS

4214841/A 08/2016

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

4214841/A 08/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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