HM65256B Series

5.0 V Supply

32,768-word × 8-bit High Speed Psuedo Static RAM

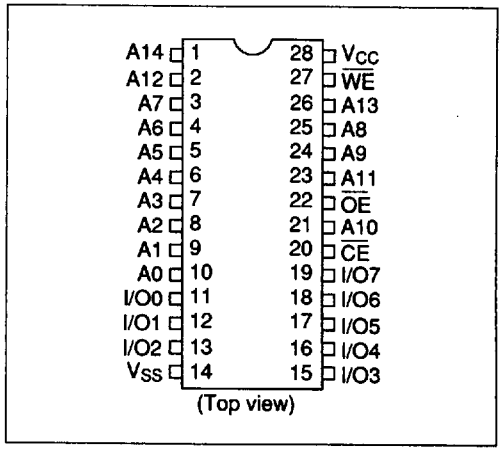
Features

- Single 5 V (±10%)
- Access time
  - — $\overline{CE}$ access time: 100/120/150/200 ns
  - — Address access time: 50/60/75/100 ns (in static column mode)
- Cycle time
  - — Random read/write cycle time: 160/190/235/310 ns
  - — Static column mode cycle time: 55/65/80/105 ns
- Low power: 175 mW typ. active
- All inputs and outputs TTL compatible
- Static column mode capability
- Non-multiplexed address
- 256 refresh cycles (4 ms)
- Refresh functions
  - — Address refresh
  - — Automatic refresh
  - — Self refresh

Ordering Information

Type No.	Access time	Package
HM65256BP-10	100 ns	600-mil 28-pin plastic DIP (DP-28)
HM65256BP-12	120 ns	
HM65256BP-15	150 ns	
HM65256BP-20	200 ns	
HM65256BLP-10	100 ns	
HM65256BLP-12	120 ns	
HM65256BLP-15	150 ns	
HM65256BLP-20	200 ns	
HM65256BSP-10	100 ns	300-mil 28-pin plastic DIP (DP-28N)
HM65256BSP-12	120 ns	
HM65256BSP-15	150 ns	
HM65256BSP-20	200 ns	
HM65256BLSP-10	100 ns	300-mil 28-pin plastic DIP (DP-28N)
HM65256BLSP-12	120 ns	
HM65256BLSP-15	150 ns	
HM65256BLSP-20	200 ns	
HM65256BFP-10T	100 ns	28-pin plastic SOP (FP-28DA)
HM65256BFP-12T	120 ns	
HM65256BFP-15T	150 ns	
HM65256BFP-20T	200 ns	
HM65256BLFP-10T	100 ns	
HM65256BLFP-12T	120 ns	
HM65256BLFP-15T	150 ns	
HM65256BLFP-20T	200 ns	

Pin Arrangement



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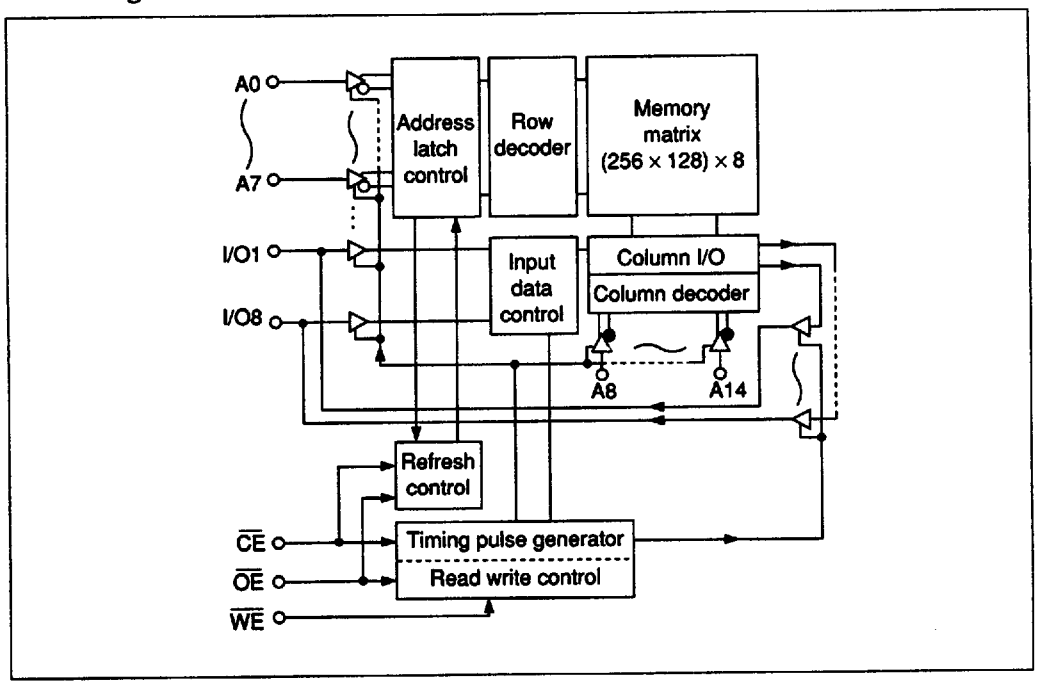
Block Diagram



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode
L	L	H	Low Z	Read
L	×	L	High Z	Write
L	H	H	High Z	—
H	L	×	High Z	Refresh
H	H	×	High Z	Standby

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Terminal voltage with respect to V_{SS}	V_T	–1.0 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	–0.5*	—	0.8	V

Note: V_{IL} min = –3.0 V for pulse width ≤ 10 ns.

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	HM65256B Min	HM65256B Typ	HM65256B Max	HM65256BL Min	HM65256BL Typ	HM65256BL Max	Unit	Test conditions
Operating power supply current	I_{CC1}	—	35	65	—	35	65	mA	$I_{I/O}$ = 0 mA tcyc = min
Standby power supply current	I_{SB1}	—	1	2	—	1	2	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$, Vin ≥ 0 v
	I_{SB2}	—	—	—	—	0.05	0.1	mA	$\overline{CE} > V_{CC} - 0.2$ V, $\overline{OE} \geq V_{CC} - 0.2$, Vin ≥ 0
Operating power supply current in self refresh mode	I_{CC2}	—	1	2	—	0.6	1	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$, Vin ≥ 0 V
	I_{CC3}	—	—	—	—	50	100	µA	$\overline{CE} \geq V_{CC} - 0.2$ V, $\overline{OE} \leq 0.2$ V, Vin ≥ 0V
Input leakage current	I_{LI}	–10	—	10	–10	—	10	µA	V_{CC} = 5.5 V, Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	–10	—	10	–10	—	10	µA	$\overline{OE} = V_{IH}$, $V_{I/O} = V_{SS}$ to V_{CC}
Output voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –1 mA

Capacitance

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	5	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	7	pF	$V_{I/O}$ = 0 V

Note: These parameters are sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

AC Test Conditions:

- Input pulse levels: 2.4 V, 0.4 V
- Input rise and fall times: 5 ns
- Timing measurement level: 2.2 V, 0.8 V
- Reference level: V_{OH} = 2.0 V, V_{OL} = 0.8 V
- Output load: 1 TTL and 100 pF (including scope and jig)

		HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Random read or write cycle time	t_{RC}	160	—	190	—	235	—	310	—	ns
Static column mode read or write cycle	t_{RSC}	55	—	65	—	80	—	105	—	ns
Chip enable access time	t_{CEA}	—	100	—	120	—	150	—	200	ns
Address access time	t_{AA}	—	50	—	60	—	75	—	100	ns
Output enable access time	t_{OEA}	—	40	—	50	—	60	—	75	ns
Chip disable to output in high Z	t_{CHZ}	—	25	—	25	—	30	—	35	ns
Chip enable to output in low Z	t_{CLZ}	30	—	30	—	35	—	40	—	ns
Output enable to output in low Z	t_{OLZ}	10	—	10	—	10	—	10	—	ns
Output disable to output in high Z	t_{OHZ}	—	25	—	25	—	30	—	35	ns
Chip enable pulse width	t_{CE}	100 ns	4 ms	120 ns	4 ms	150 ns	4 ms	200 ns	4 ms	
Chip enable precharge time	t_P	50	—	60	—	75	—	100	—	ns
Address set-up time	t_{AS}	0	—	0	—	0	—	0	—	ns
Row address hold time	t_{RAH}	20	—	20	—	25	—	30	—	ns
Column address hold time	t_{CAH}	100	—	120	—	150	—	200	—	ns
Read command set-up time	t_{RCS}	0	—	0	—	0	—	0	—	ns
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns
Output enable hold time	t_{OHC}	0	—	0	—	0	—	0	—	ns
Output enable to chip enable delay time	t_{OCD}	0	—	0	—	0	—	0	—	ns
Output hold time from column address	t_{OH}	5	—	5	—	5	—	10	—	ns
Write command pulse width	t_{WP}	25	—	25	—	30	—	35	—	ns
Chip enable to end of write	t_{CW}	100	—	120	—	150	—	200	—	ns

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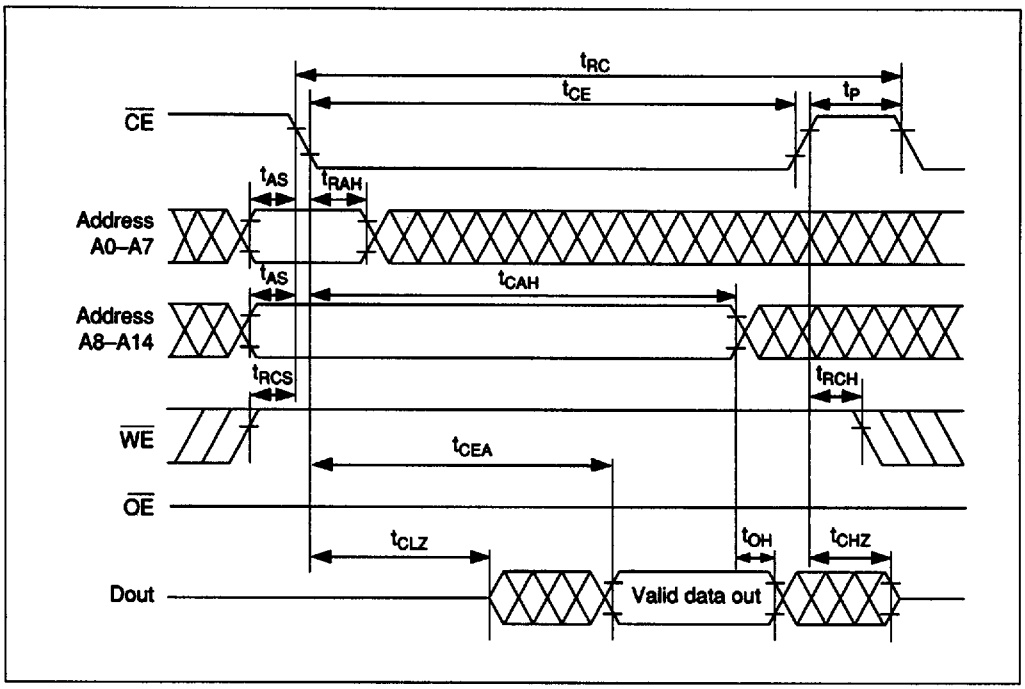
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%) (cont)

		HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Column address set-up time	t_{ASW}	0	—	0	—	0	—	0	—	ns
Column address hold time after write	t_{AHW}	0	—	0	—	0	—	0	—	ns
Data valid to end of write	t_{DW}	20	—	20	—	25	—	30	—	ns
Data in hold time for write	t_{DH}	0		0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	5	—	5	—	5	—	5		ns
Write to output in high Z	t_{WHZ}	—	25	—	25	—	30	—	35	ns
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns
Refresh command delay time	t_{RFD}	50	—	60	—	75	—	100	—	ns
Refresh precharge time	t_{FP}	30	—	30	—	30	—	30	—	ns
Refresh command pulse width for automatic refresh	t_{FAP}	80	10000	80	10000	80	10000	80	10000	ns
Automatic refresh cycle time	t_{FC}	160	—	190	—	235	—	310	—	ns
Refresh command pulse width for self refresh	t_{FAS}	10000	—	10000	—	10000	—	10000	—	ns
Refresh reset time for self refresh	t_{FRS}	160	—	190	—	235	—	310	—	ns
Refresh period	t_{REF}	—	4	—	4	—	4	—	4	ns

Notes:
1. t_{CHZ}, t_{OHZ}, and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.
2. t_{CLZ}, t_{OLZ} and t_{OW} are sampled under the condition of t_T = 5 ns, and not 100% tested.
3. A write occurs during the overlap of a low $\overline{CE}$ and low $\overline{WE}$.
4. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
5. If input signals of opposite phase to the outputs are applied in a write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
6. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. An initial pause of 100 µs is required after power-up followed by a minimum of 8 initialization cycles.
8. At the end of self refresh, refresh reset time (t_{FRS}) is required to reset the internal self refresh operation of the RAM. During t_{FRS}, $\overline{CE}$ and $\overline{OE}$ must be kept high. If auto refresh follows self refresh, low transition of $\overline{OE}$ at the beginning of auto refresh must not occur during t_{FRS} period.

Timing Waveforms

Read Cycle (1) ($\overline{CE}$ controlled)



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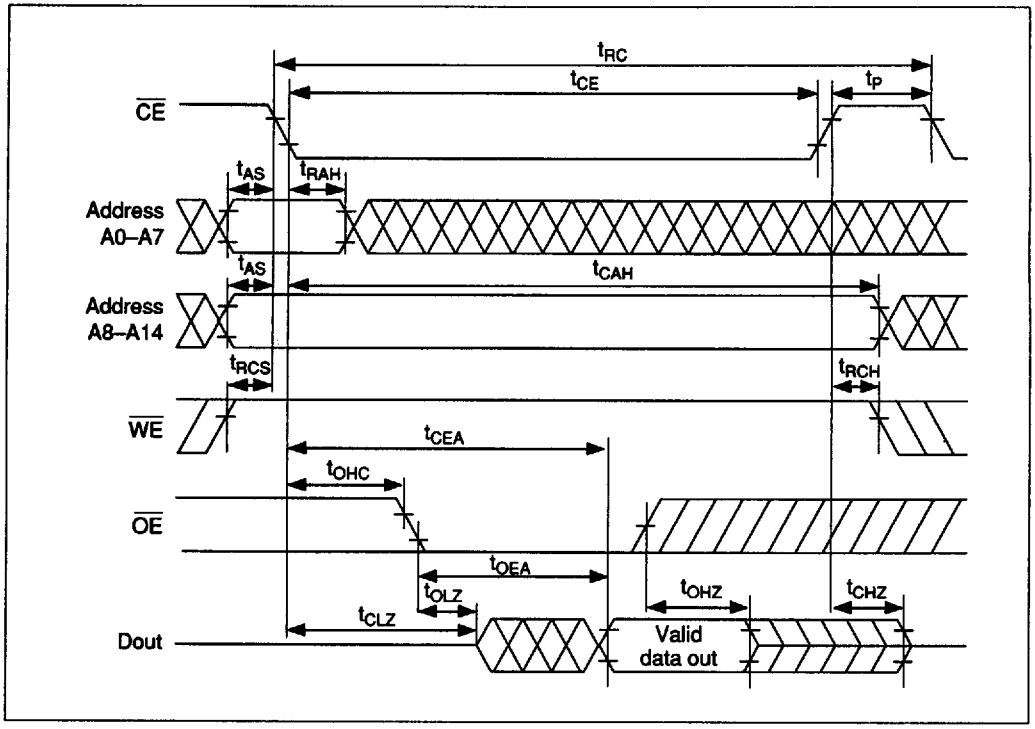
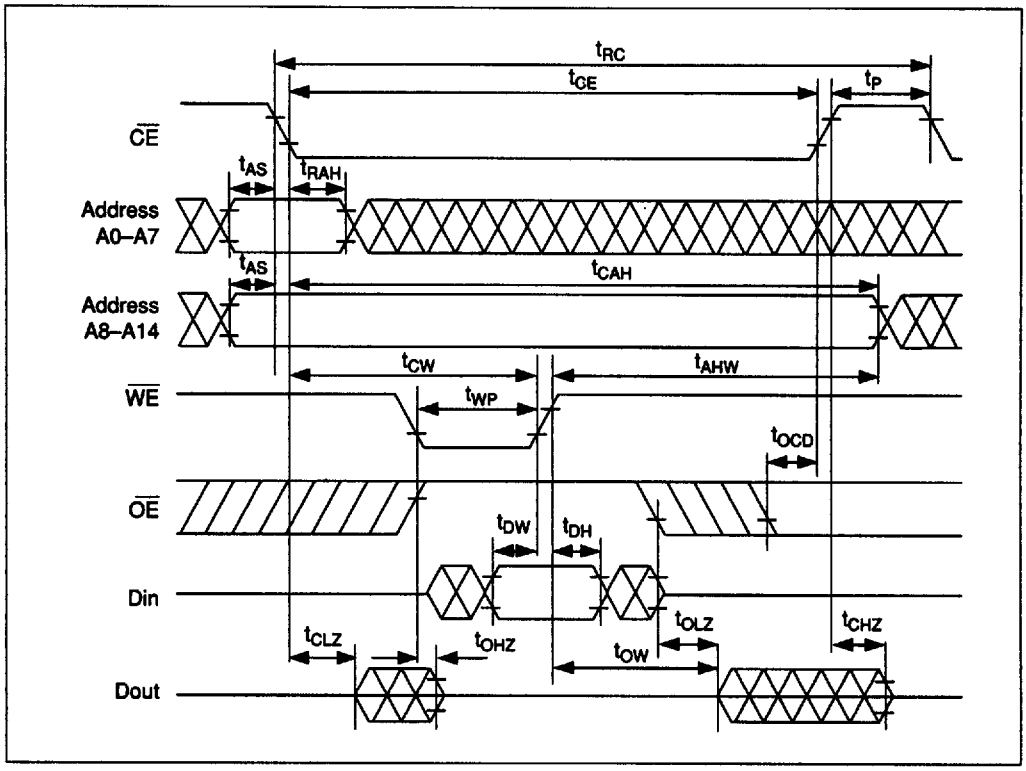
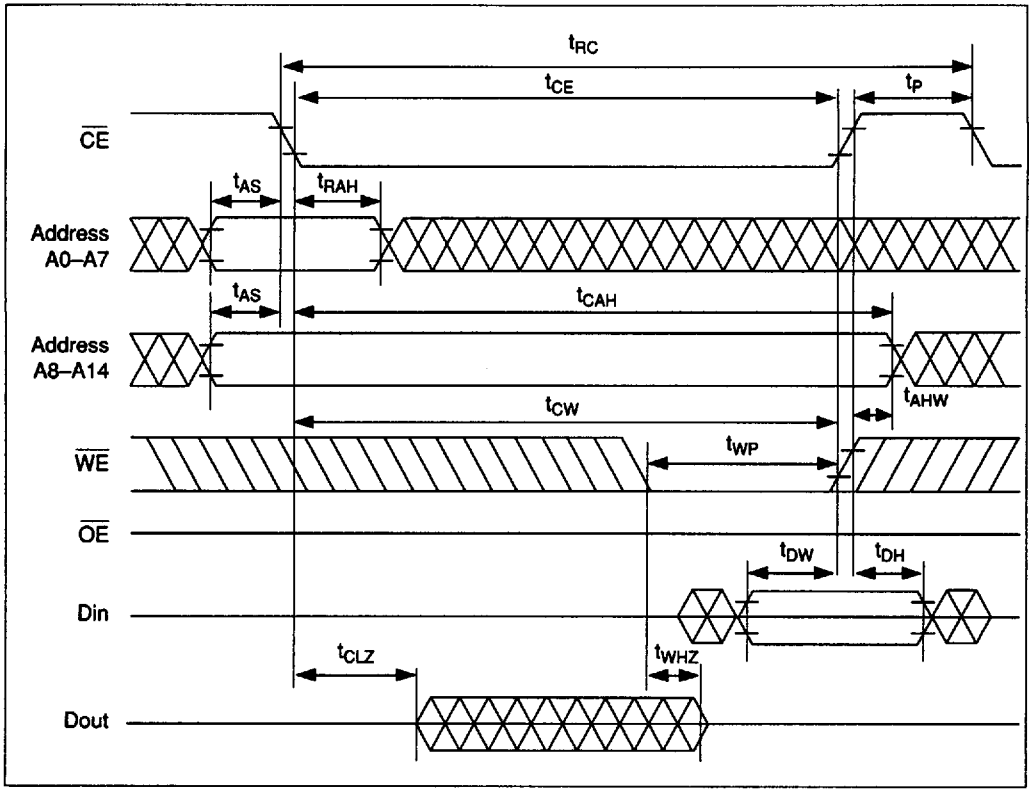
Read Cycle (2) ($\overline{OE}$ controlled)



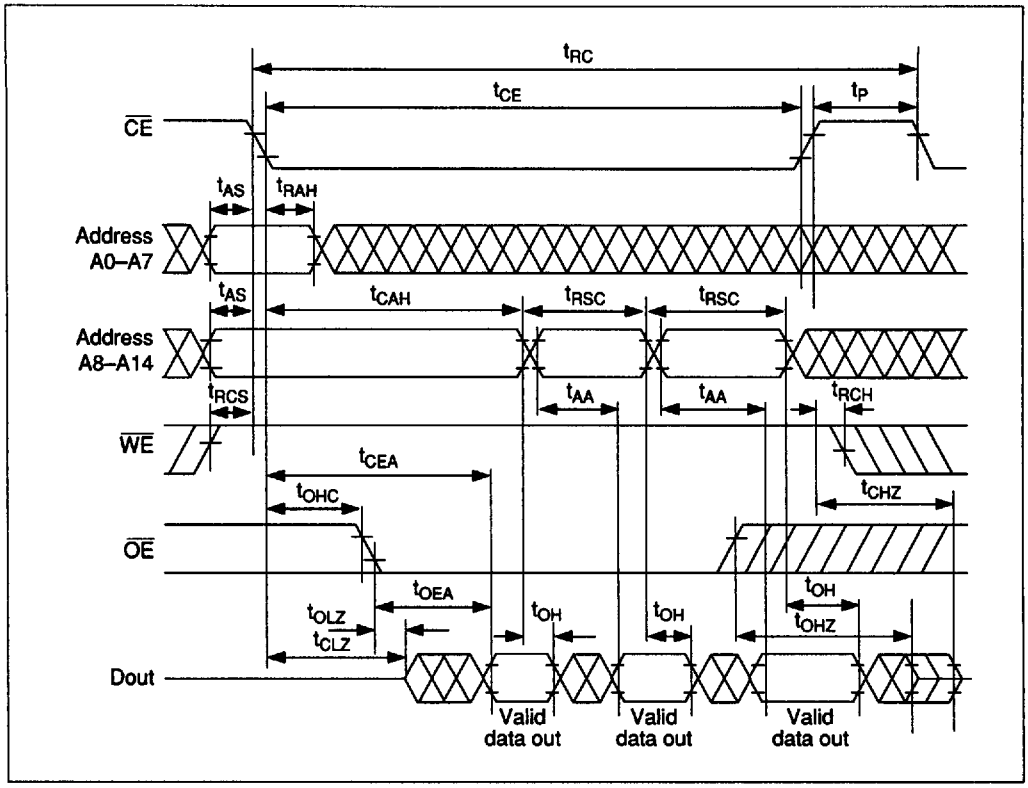
Write Cycle (1) ($\overline{OE}$ Clock)



Write Cycle (2) ($\overline{OE}$ fixed low)



Static Column Mode Read Cycle



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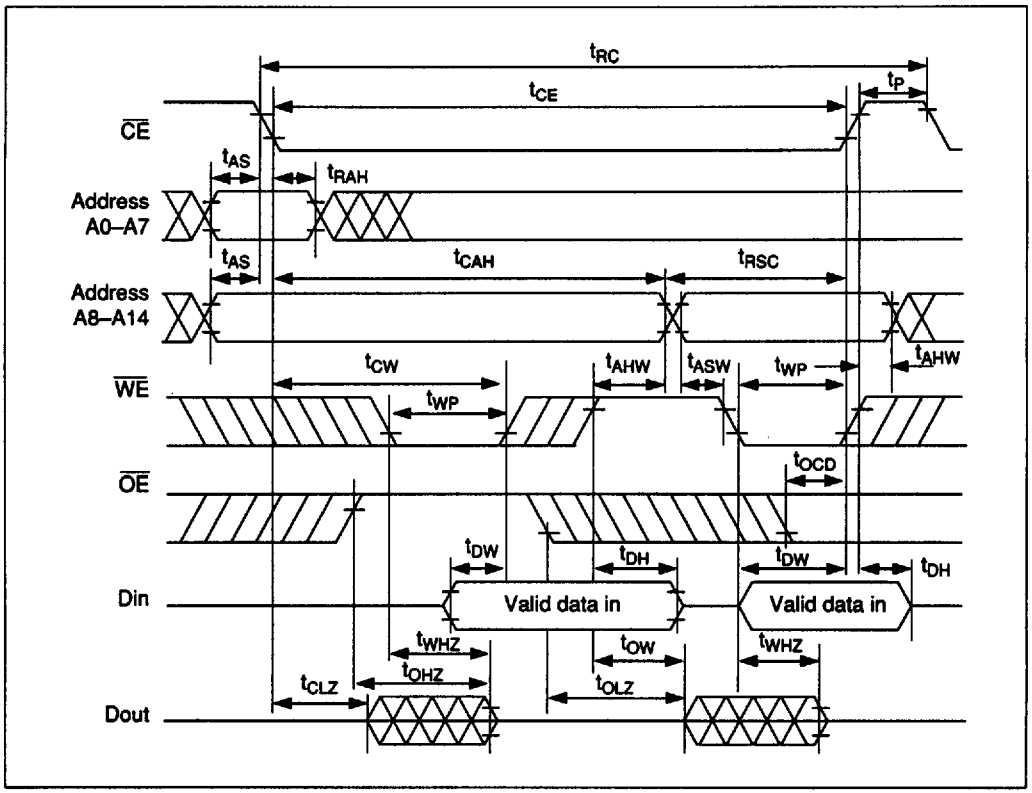
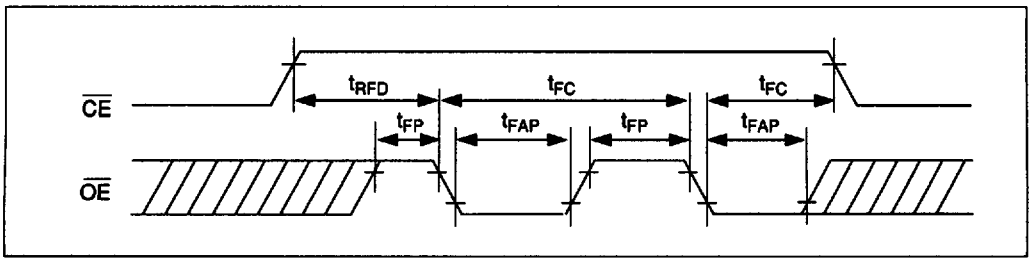
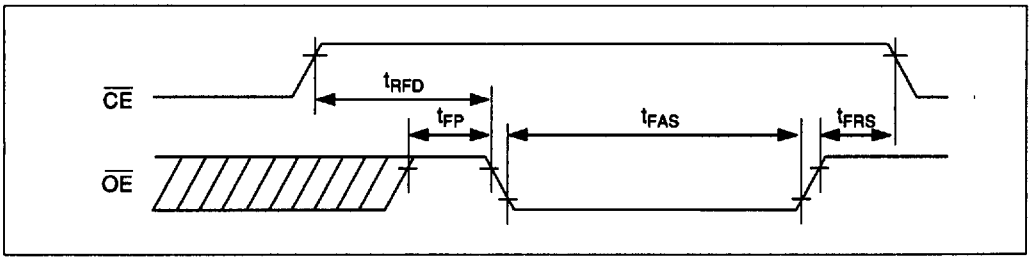
Static Column Mode Write Cycle



Automatic Refresh Cycle



Self Refresh Cycle