



# 128K x 8 Static RAM

## Features

- **High speed**  
—  $t_{AA} = 12$  ns
- **Low active power**  
— 495 mW (max. 12 ns)
- **Low CMOS standby power**  
— 55 mW (max.) 4 mW
- **2.0V Data Retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{OE}$  options**

## Functional Description<sup>[1]</sup>

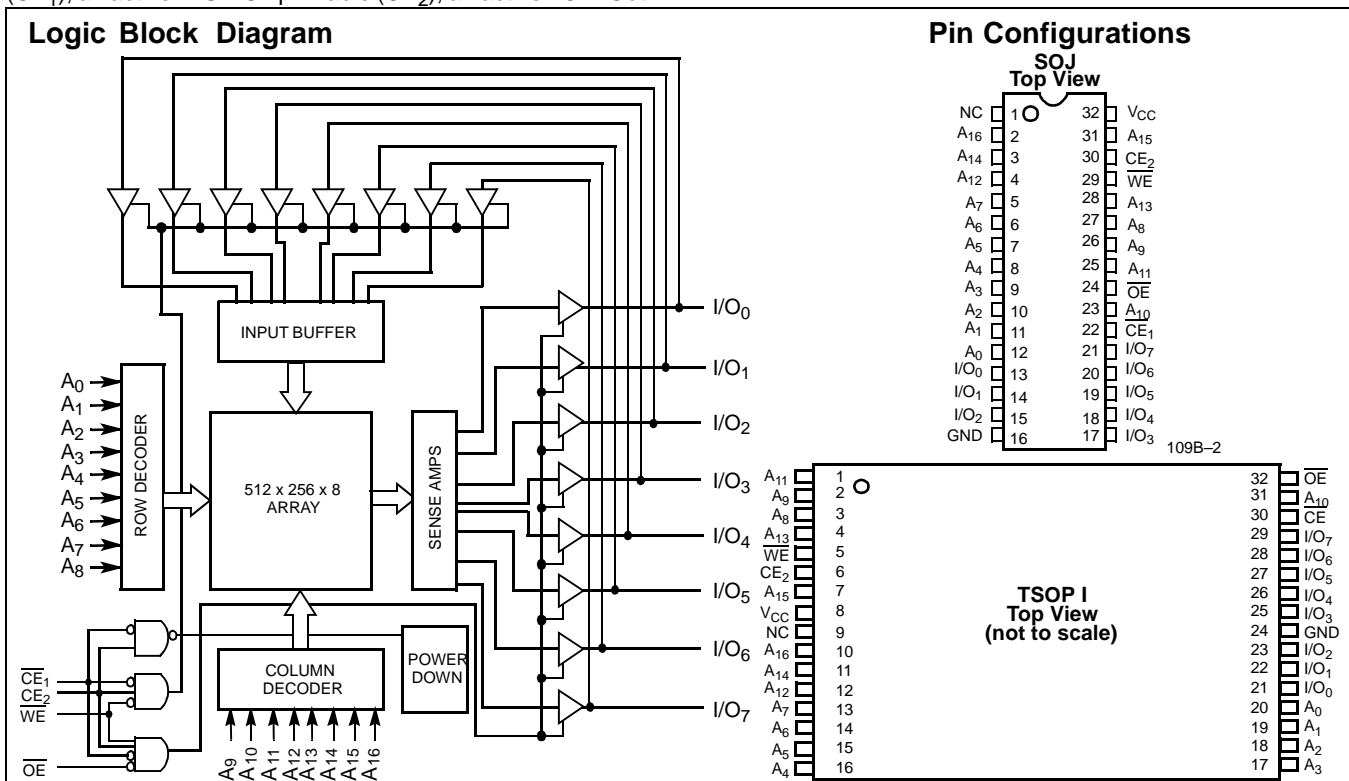
The CY7C109B / CY7C1009B is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}_1$ ), an active HIGH Chip Enable ( $\overline{CE}_2$ ), an active LOW Out-

put Enable ( $\overline{OE}$ ), and three-state drivers. Writing to the device is accomplished by taking Chip Enable One ( $\overline{CE}_1$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW and Chip Enable Two ( $\overline{CE}_2$ ) input HIGH. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking Chip Enable One ( $\overline{CE}_1$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) and Chip Enable Two ( $\overline{CE}_2$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $\overline{CE}_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $\overline{CE}_2$  HIGH, and  $\overline{WE}$  LOW).

The CY7C109B is available in standard 400-mil-wide SOJ and 32-pin TSOP type I packages. The CY7C1009B is available in a 300-mil-wide SOJ package. The CY7C1009B and CY7C109B are functionally equivalent in all other respects.



## Selection Guide

	7C109B-12 7C1009B-12	7C109B-15 7C1009B-15	7C109B-20 7C1009B-20	7C109B-25 7C1009B-25	7C109B-35 7C1009B-35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	90	80	75	70	60
Maximum CMOS Standby Current (mA)	10	10	10	10	10
Maximum CMOS Standby Current (mA) Low Power Version	2	2	2	-	-

**Note:**

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied..... -55°C to +125°C  
 Supply Voltage on  $V_{CC}$  to Relative GND<sup>[2]</sup> ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[2]</sup> ..... -0.5V to  $V_{CC} + 0.5V$   
 DC Input Voltage<sup>[2]</sup> ..... -0.5V to  $V_{CC} + 0.5V$   
 Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >2001V  
 (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature	$V_{CC}$
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	7C109B-12 7C1009B-12		7C109B-15 7C1009B-15		Unit
			Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	-0.3	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	µA
$I_{OZ}$	Output Leakage Current	$GND \leq V_I \leq V_{CC},$ Output Disabled	-5	+5	-5	+5	µA
$I_{OS}$	Output Short Circuit Current <sup>[3]</sup>	$V_{CC} = \text{Max.}, V_{OUT} = GND$		-300		-300	mA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$		90		80	mA
$I_{SB1}$	Automatic CE Power-Down Current —TTL Inputs	Max. $V_{CC}, \overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}, V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$		45		40	mA
$I_{SB2}$	Automatic CE Power-Down Current —CMOS Inputs	Max. $V_{CC}, \overline{CE}_1 \geq V_{CC} - 0.3V,$ or $CE_2 \leq 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V,$ or $V_{IN} \leq 0.3V, f = 0$		10		10	mA
			L	2		2	mA

**Notes:**

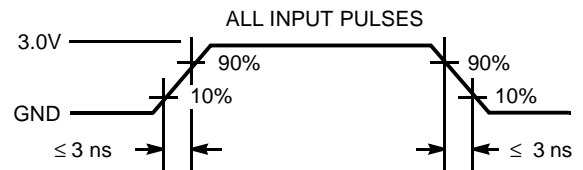
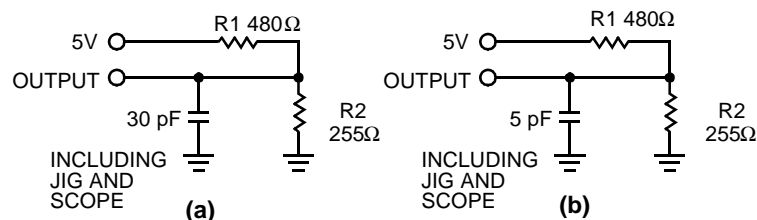
- Minimum voltage is -2.0V for pulse durations of less than 20 ns.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

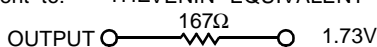
**Electrical Characteristics** Over the Operating Range (continued)

Parameter	Description	Test Conditions	7C109B-20 7C1009B-20		7C109B-25 7C1009B-25		7C109B-35 7C1009B-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$GND \leq V_I \leq V_{CC}$ , Output Disabled	-5	+5	-5	+5	-5	+5	$\mu\text{A}$
$I_{OS}$	Output Short Circuit Current <sup>[3]</sup>	$V_{CC} = \text{Max.}, V_{OUT} = GND$		-300		-300		-300	mA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$		75		70		60	mA
$I_{SB1}$	Automatic CE Power-Down Current — TTL Inputs	Max. $V_{CC}$ , $CE_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		30		30		25	mA
$I_{SB2}$	Automatic CE Power-Down Current — CMOS Inputs	Max. $V_{CC}$ , $CE_1 \geq V_{CC} - 0.3\text{V}$ , or $CE_2 \leq 0.3\text{V}$ , $V_{IN} \geq V_{CC} - 0.3\text{V}$ , or $V_{IN} \leq 0.3\text{V}$ , $f = 0$		10		10		10	mA
			L	2		—		—	mA

**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 5.0\text{V}$	9	pF
$C_{OUT}$	Output Capacitance		8	pF

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT  


**Note:**

4. Tested initially and after any design or process changes that may affect these parameters.

**Switching Characteristics<sup>[5]</sup> Over the Operating Range**

Parameter	Description	7C109B-12 7C1009B-12		7C109B-15 7C1009B-15		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{RC}$	Read Cycle Time	12		15		ns
$t_{AA}$	Address to Data Valid		12		15	ns
$t_{OHA}$	Data Hold from Address Change	3		3		ns
$t_{ACE}$	$\overline{CE}_1$ LOW to Data Valid, $CE_2$ HIGH to Data Valid		12		15	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		6		7	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		6		7	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW to Low Z, $CE_2$ HIGH to Low Z <sup>[7]</sup>	3		3		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH to High Z, $CE_2$ LOW to High Z <sup>[6, 7]</sup>		6		7	ns
$t_{PU}$	$\overline{CE}_1$ LOW to Power-Up, $CE_2$ HIGH to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH to Power-Down, $CE_2$ LOW to Power-Down		12		15	ns
<b>Write Cycle<sup>[8]</sup></b>						
$t_{WC}$	Write Cycle Time <sup>[9]</sup>	12		15		ns
$t_{SCE}$	$\overline{CE}_1$ LOW to Write End, $CE_2$ HIGH to Write End	10		12		ns
$t_{AW}$	Address Set-Up to Write End	10		12		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	10		12		ns
$t_{SD}$	Data Set-Up to Write End	7		8		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		6		7	ns

**Notes:**

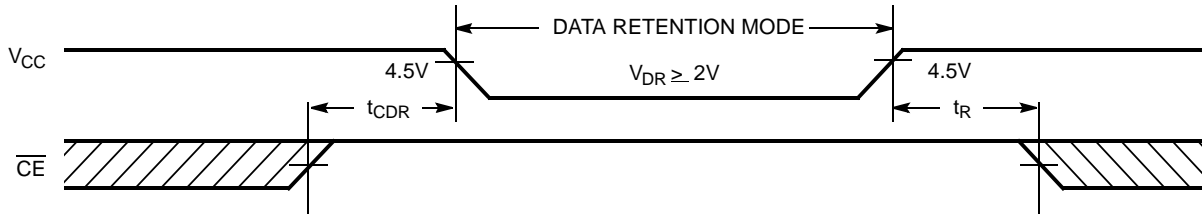
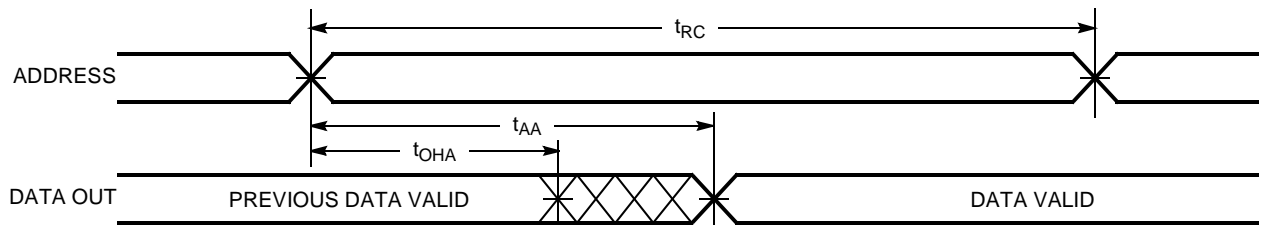
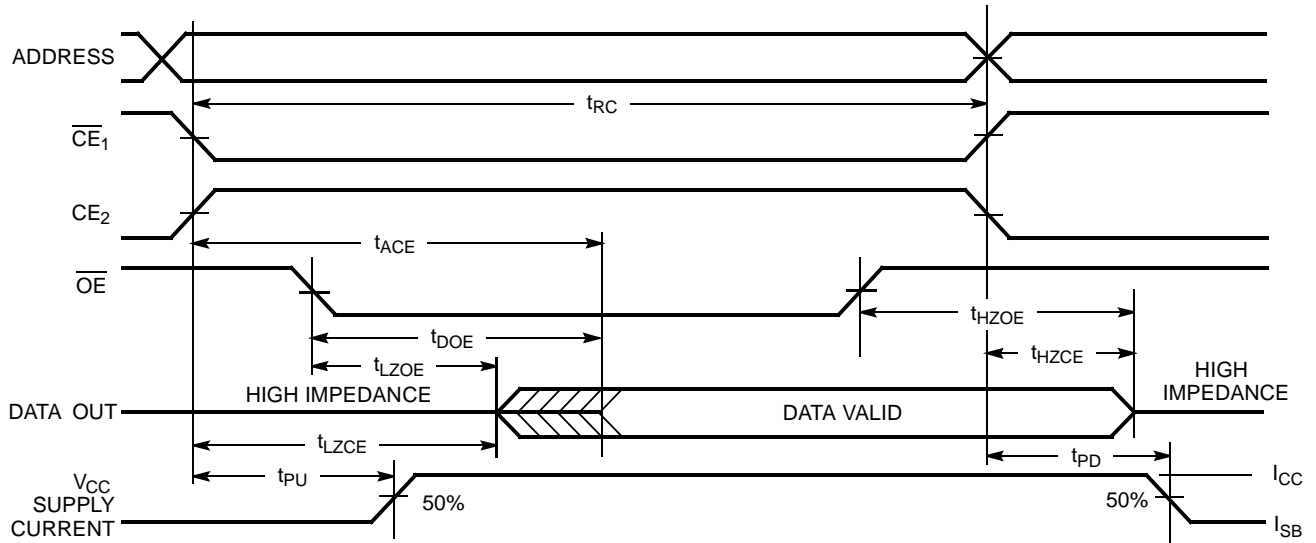
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW and  $CE_2$  HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Switching Characteristics<sup>[5]</sup> Over the Operating Range (continued)**

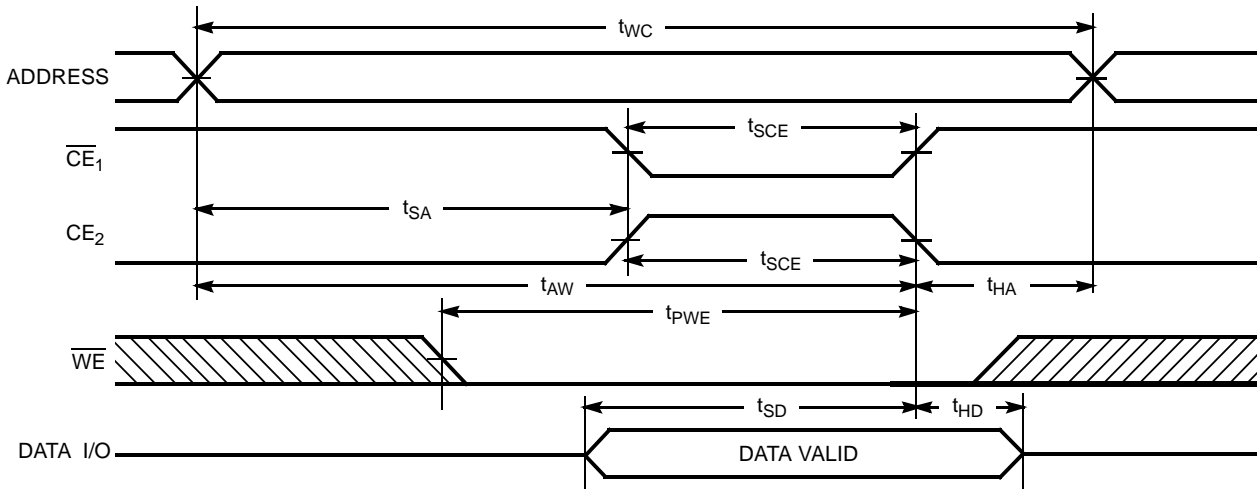
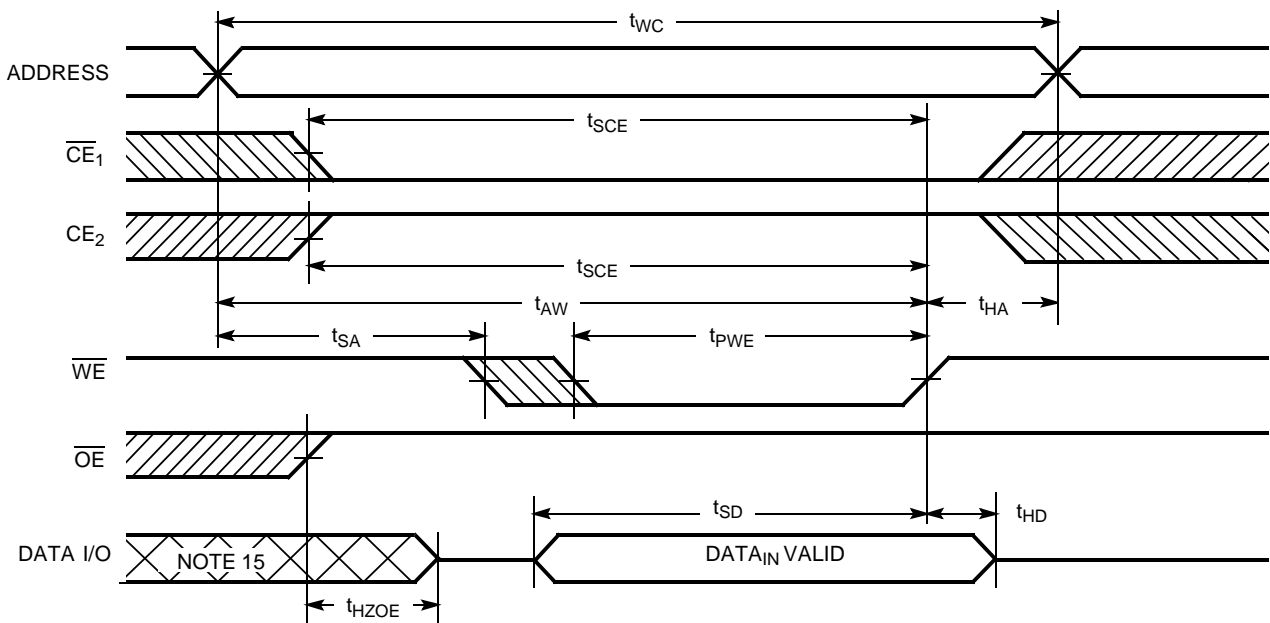
Parameter	Description	7C109B-20 7C1009B-20		7C109B-25 7C1009B-25		7C109B-35 7C1009B-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
t <sub>RC</sub>	Read Cycle Time	20		25		35		ns
t <sub>AA</sub>	Address to Data Valid		20		25		35	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		5		5		ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW to Data Valid, $CE_2$ HIGH to Data Valid		20		25		35	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		8		10		15	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		8		10		15	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW to Low Z, $CE_2$ HIGH to Low Z <sup>[7]</sup>	3		5		5		ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH to High Z, $CE_2$ LOW to High Z <sup>[6, 7]</sup>		8		10		15	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW to Power-Up, $CE_2$ HIGH to Power-Up	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH to Power-Down, $CE_2$ LOW to Power-Down		20		25		35	ns
<b>Write Cycle<sup>[8]</sup></b>								
t <sub>WC</sub>	Write Cycle Time <sup>[9]</sup>	20		25		35		ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW to Write End, $CE_2$ HIGH to Write End	15		20		25		ns
t <sub>AW</sub>	Address Set-Up to Write End	15		20		25		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	12		15		20		ns
t <sub>SD</sub>	Data Set-Up to Write End	10		15		20		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		5		5		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		8		10		15	ns

**Data Retention Characteristics Over the Operating Range (Low Power version only)**

Parameter	Description	Conditions	Min.	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	No input may exceed V <sub>CC</sub> + 0.5V V <sub>CC</sub> = V <sub>DR</sub> = 2.0V, $CE_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	2.0		V
I <sub>CCDR</sub>	Data Retention Current			150	μA
t <sub>CDR</sub>	Chip Deselect to Data Retention Time		0		ns
t <sub>R</sub>	Operation Recovery Time		200		μs

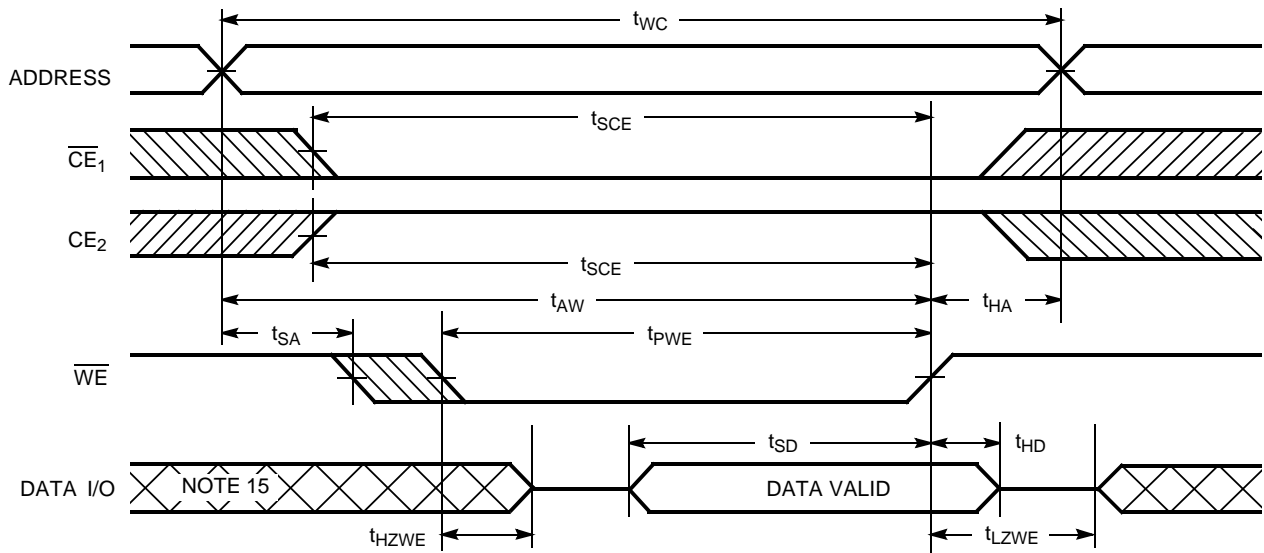
**Data Retention Waveform**

**Switching Waveforms**
**Read Cycle No. 1<sup>[10, 11]</sup>**

**Read Cycle No. 2 (OE Controlled)<sup>[11, 12]</sup>**

**Notes:**

10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{CE}_1$  or  $CE_2$  Controlled)<sup>[13, 14]</sup>**

**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[13, 14]</sup>**

**Notes:**

13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
14. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
15. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[14]</sup>**

**Truth Table**

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
X	L	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
L	H	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	H	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

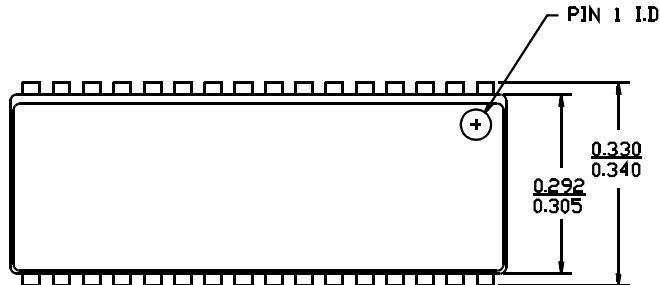


**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C109B-12VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1009B-12VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C109B-12ZC	Z32	32-Lead TSOP Type I	
15	CY7C109B-15VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
	CY7C109BL-15VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C1009B-15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C109B-15ZC	Z32	32-Lead TSOP Type I	
	CY7C109BL-15ZC	Z32	32-Lead TSOP Type I	
	CY7C109B-15VI	V33	32-Lead (400-Mil) Molded SOJ	Industrial
	CY7C109BL-15VI	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C1009B-15VI	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C109B-15ZI	Z32	32-Lead TSOP Type I	
20	CY7C109B-20VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1009B-20VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C109B-20VI	V33	32-Lead (400-Mil) Molded SOJ	Industrial
	CY7C109B-20ZC	Z32	32-Lead TSOP Type I	Commercial
	CY7C109B-20ZI	Z32	32-Lead TSOP Type I	Industrial
25	CY7C109B-25VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1009B-25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C109B-25VI	V33	32-Lead (400-Mil) Molded SOJ	Industrial
	CY7C109B-25ZC	Z32	32-Lead TSOP Type I	Commercial
	CY7C109B-25ZI	Z32	32-Lead TSOP Type I	Industrial
35	CY7C109B-35VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1009B-35VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C109B-35VI	V33	32-Lead (400-Mil) Molded SOJ	Industrial

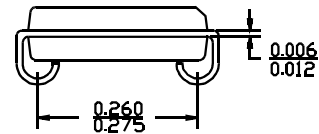
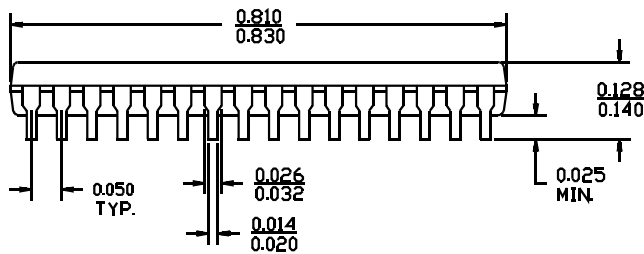
**Package Diagrams**

**32-Lead (300-Mil) Molded SOJ V32**



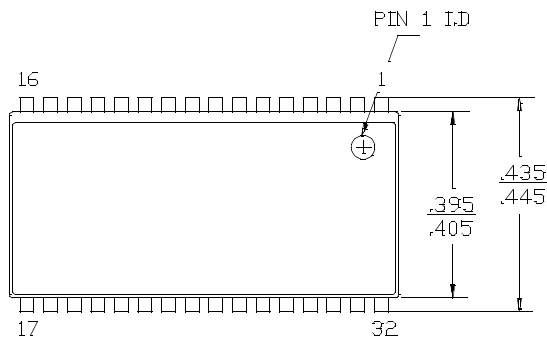
DIMENSIONS IN INCHES MIN.  
MAX.

LEAD COPLANARITY 0.004 MAX.

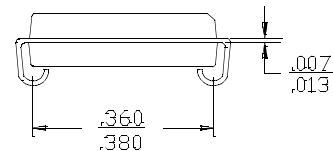
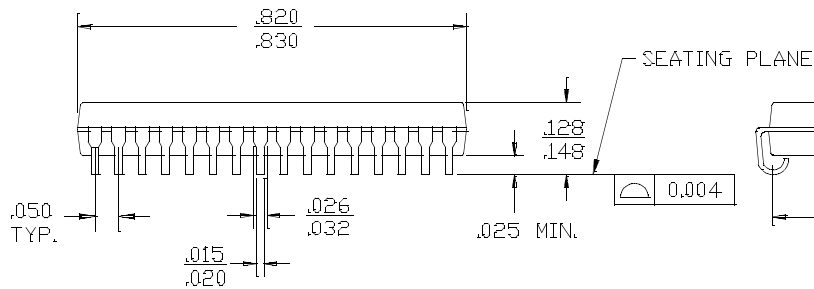


51-85041-\*A

**32-Lead (400-Mil) Molded SOJ V33**



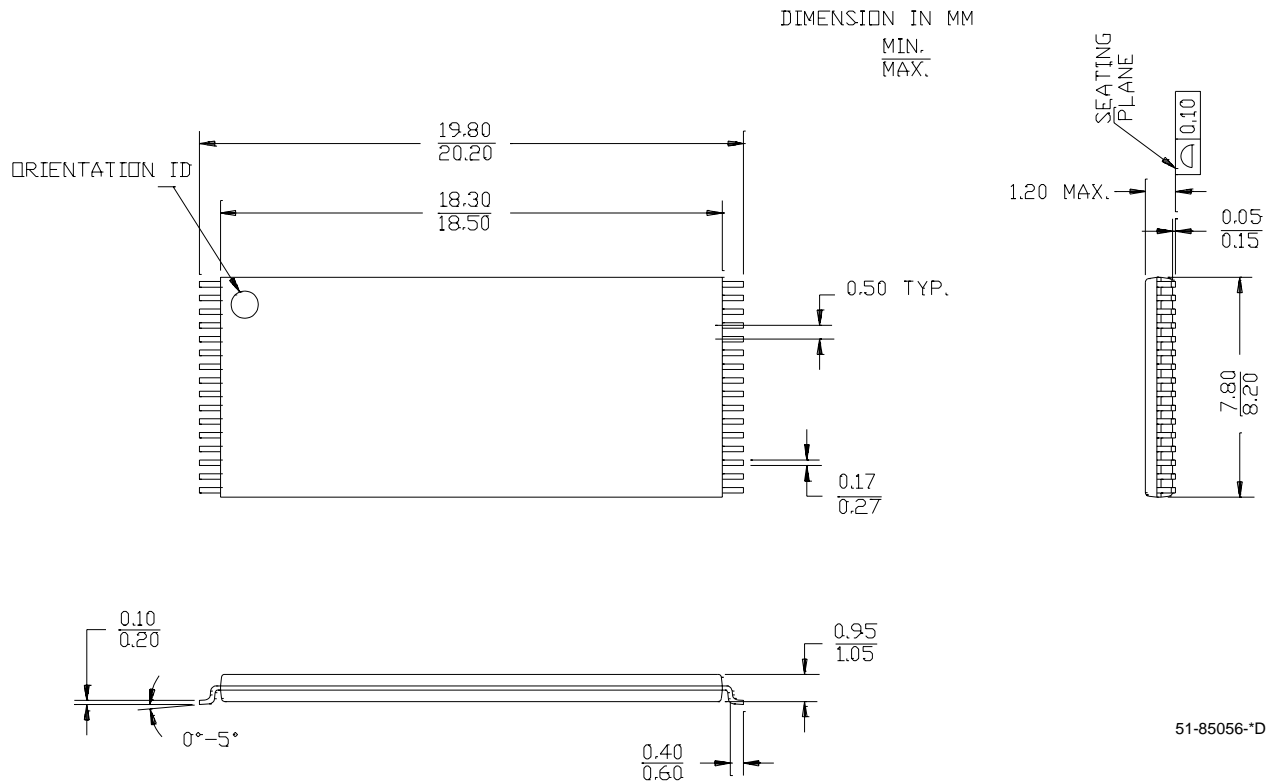
DIMENSIONS IN INCHES MIN.  
MAX.



51-85033-\*B

Package Diagrams (continued)

**32-Lead Thin Small Outline Package Type I (8x20 mm) Z32**



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**Document History Page**

<b>Document Title: CY7C109B, CY7C1009 128K x 8 SRAM</b> <b>Document Number: 38-05038</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	106832	09/22/01	SZV	Change from Spec number: 38-00971 to 38-05038
*A	116467	09/16/02	CEA	Add applications foot note to data sheet, page 1

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