FUJITSU SEMICONDUCTOR

FR50
32-BIT MICROCONTROLLER
MB91F376GS
Datasheet

Release 1.2 28-Feb-2005

Revision History

Revision	Date	Item
1.0	4-Jun-2004	First release
1.1	30-Jun-2004	Correct part number from MB91F376S to MB91F376GS
1.2	28-Feb-2005	Correct part number from MB91F376G to MB91F376GS in overview

Table of Contents

CHAPTER 1 MB91F376GS Overview

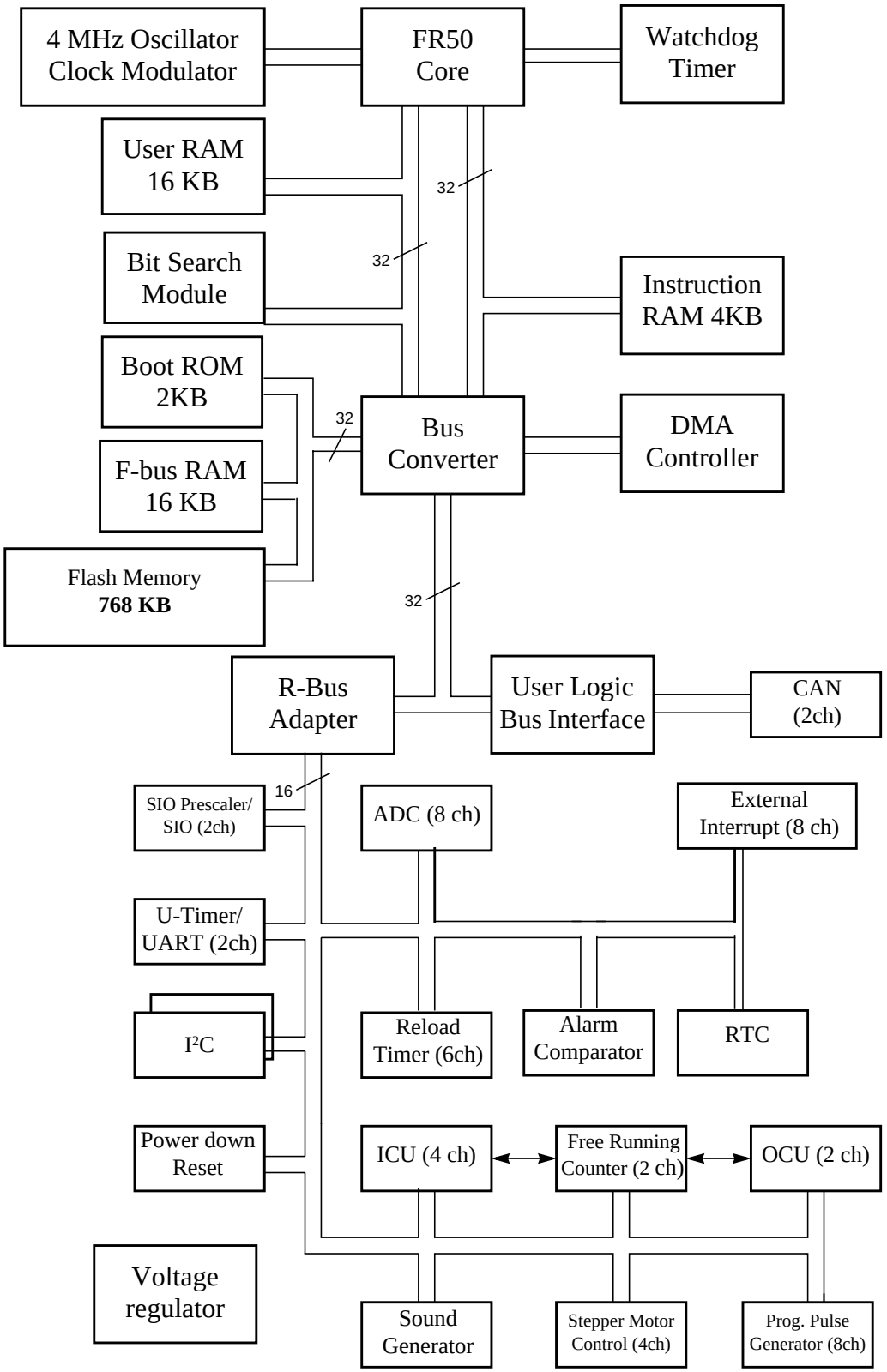
MB91F376GS (S= single clock) is a bondvariant of MB91F376G.

On MB91F376GS the RTC module is connected to the 4 MHz oscillator instead of the 32 KHz oscillator as on MB91F376G.

The 32KHz oscillator pins have no function on MB91F376GS.

Please see the documentation for MB91F376G for details.

1.1 MB91F376GS Block Structure



1.2 Core Functionality

Function	Feature	Remarks
FR50 Core	32-bit Fujitsu RISC Core FR30 software compatible	
Clock module (clock control, clock divider, PLLs)	Setting of frequencies for CPU and peripherals Low power consumption modes: RTC mode: only the **R**eal **T**ime **C**lock and the selected oscillator are active (= STOP mode and bit 0 of STCR is set to 0) STOP mode: all internal circuits and the oscillation circuits are halted	
Watchdog	adjustable watchdog timer interval (between 2^{20} and 2^{26} system clock cycles)	
I-RAM 4 kB	I-RAM	see remark below table
D-Bus RAM 16 kB	RAM for user data	see remark below table
F-Bus RAM 16 kB	RAM for data and code	see remark below table
Flash Memory 768 kB	sector architecture: sector 0 :64 kB | sector 2: 64 kB sector 1: 64 kB | sector 3: 64 kB sector 4: 64 kB | sector 11: 64 kB sector 5: 64 kB | sector 12: 64 kB sector 6: 64 kB | sector 13: 64 kB sector 7: 32 kB | sector 14: 32 kB sector 8: 8 kB | sector 15: 8 kB sector 9: 8 kB | sector 16: 8 kB sector 10:16 kB | sector 17: 16 kB sector 0 :64 kB | sector 2: 64 kB sector 1: 64 kB | sector 3: 64 kB | | V V 16 bit 16 bit write access is 16 bit wide, read access can be 16 or 32 bit wide	Flash memory on F376G connected to F-Bus Minimum 10000 program/erase cycles Minimum 10 years data retention Net read cycle time to the memory is 50ns. For overall access time see settings in Chapter 2.1
Boot ROM 2 kB		

DMA	5 channels up to 16 DMA sources can be used transfer modes: single/block, burst, continuous	
Interrupt Controller	8 external interrupt channels, 38 internal interrupts, 16 programmable priority levels	
Bit Search Module	Searches a word for the position of the first “1” and “0” change bit, starting from the MSB. Performs the search in 1 cycle.	
Fixed Reset Vector	Hard wired reset and mode vector	code start at 0F:4000H
Voltage Regulator	Generates internal voltage of 3.3 V	

Remark:

Set bit 9 (SYNCR) of TBCR to 1 to enable the synchronisation of the reset signal; a reset will be generated only after all bus accesses have been done. This avoids that erroneous data are written into the RAMs during reset.

1.3 Features

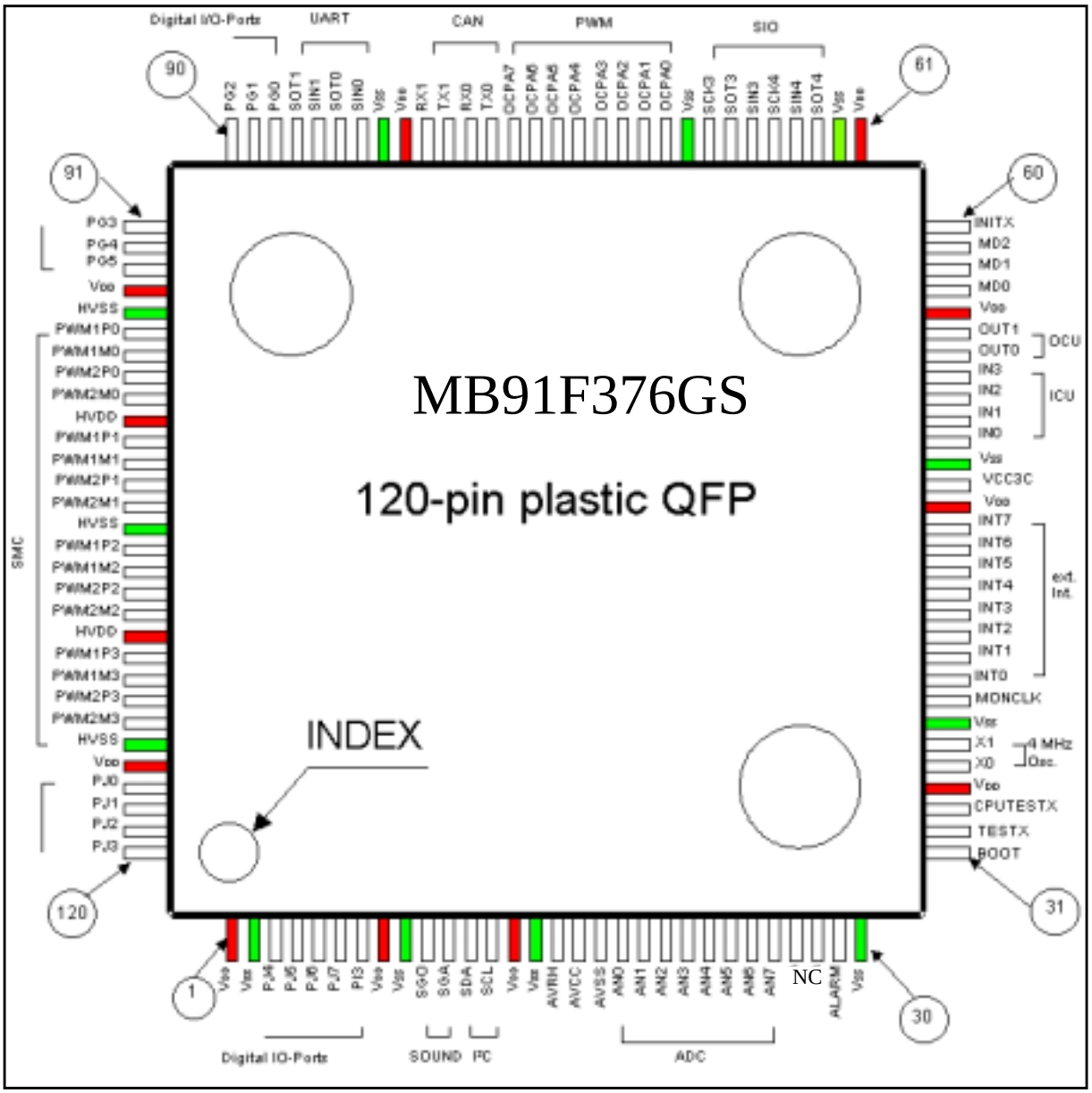
Function	Feature	Remarks
PPG for dimmer (8 channels)	16-bit PWM Timer 16 bit down counter, cycle and duty setting registers interrupt at triggering, cycle or duty match can be triggered by software or reload timer PWM operation and one-shot operation Clock disable internal prescaler allows $f_{RES}/1$, $f_{RES}/4$, $f_{RES}/16$, $f_{RES}/64$ as counter clock	required frequencies are 90-300 Hz
ADC (8 channels)	successive approximation, internal sample and hold circuit 10-bit resolution, 5 V operation, (conversion time: 178 cycles of CLKP) program selectable analogue input channels: single conversion mode continuous conversion mode stop conversion mode interrupt at the end of a conversion can be used to activate DMA transfer activation by software or reload timer can be selected Prescaling is done internally Clock disable	
Basic Interval Timer (6 channels)	16-bit reload timer, includes clock prescaler ($f_{RES}/2^1$, $f_{RES}/2^3$, $f_{RES}/2^5$)	
CAN (2 channels)	conforms to CAN specification version 2.0 A and B automatic re-transmission in case of error automatic transmission responding to remote frame prioritized 16 message buffers for data and IDs supports multiple messages flexible configuration of acceptance filtering: full bit compare / full bit mask / two partial bit masks supports up to 1 Mb/s Clock Disable	CAN allows TSEG2 = RSJW setting

External Interrupt (8 channels)	can be programmed to be edge sensitive or level sensitive interrupt masking and request pending bits per channel	
I^2C-1 for standard mode	master or slave transmission arbitration function clock synchronization function slave address and general call address detect function transfer direction detect function start condition repeat generation and detection function bus error detect function compatible to I^2C standard mode specification (operation up to 100 kHz, 7 bit addressing) includes clock divider functionality Clock disable	Only I^2C-1 or I^2C-2 can be used, not both in parallel. Bit 0 of F362MD will be used to decide which module is connected to the SCL and SDA pads. By default it is I^2C-1. Multimaster operation is not possible.
I^2C-2 for standard and fast mode	master or slave transmission arbitration function clock synchronization function slave address and general call address detect function transfer direction detect function start condition repeat generation and detection function bus error detect function compatible to I^2C standard and fast mode specification (operation up to 400 kHz, 10 bit addressing) includes clock divider functionality Clock disable	Only I^2C-1 or I^2C-2 can be used, not both in parallel. Bit 0 of F362MD will be used to decide which module is connected to the SCL and SDA pads. By default it is I^2C-1. SCL and SDA lines include optional noise filter. The noise filter allows the suppression of spikes in the range of 1 to 1.5 cycles of CLKP. Communication on the I2C bus between other connected devices is not possible if MB91F36xGB/366GA is not connected to the supply voltage. Multimaster operation is not possible.
16-bit Input Capture (ICU) (4 channels)	rising edge, falling edge or rising & falling edge sensitive two 16-bit capture registers signals an interrupt at external event Clock disable	
16-bit Output Compare OCU (2 channels)	signals an interrupt when a match with of 16-bit IO timer occurs an output signal can be generated Clock disable	

Free running Timer (2 channels for ICU and OCU modules)	16-bit free running timer, signals an interrupt when overflow or match with compare register_0 includes prescaler ($f_{RES}/2^2$, $f_{RES}/2^4$, $f_{RES}/2^5$, $f_{RES}/2^6$) timer data register has R/W access Clock disable	
Alarm Comparator (OV/UV detection)	monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds status is readable, interrupts can be masked separately Clock disable	uses external 4:1 voltage divider
Power down reset	monitors Vdd and generates a reset if Vdd is less than a defined threshold voltage	disabled in RTC and STOP modes
Serial IO SIO Synchronous Serial Interface (2 channels) + SIO-Prescaler (2 channels)	Serial IO transfer can be started from MSB or LSB supports internal clock synchronized transfer and external clock synchronized transfer prescaler for shift clock allows: $f_{RES}/3$, $f_{RES}/4$, $f_{RES}/5$, $f_{RES}/6$, $f_{RES}/7$, $f_{RES}/8$ Clock disable	supports positive and negative clock edge synchronization
Sound Generator (Buzzer)	8-bit PWM signal is mixed with tone frequency from 8-bit reload counter PWM clock by internal prescaler: $f_{RES}/1$, $f_{RES}/2$, $f_{RES}/4$, $f_{RES}/8$ tone frequency: PWM frequency / 2 / (reload value + 1) Clock disable	Target frequency to be programmable in the range of 300 Hz to 5 kHz $f_{RES}/1$ and a reload value of 5 result in 5.2 kHz at f_{RES} = 16MHz, $f_{RES}/4$ and a reload value of 25 result in 300.48 Hz @ f_{RES} = 16MHz
Stepper Motor Control (4 channels)	four high current outputs for each channel two synchronized 8-bit PWMs per channel internal prescaling for PMW clock: f_{RES}, $f_{RES}/2$, $f_{RES}/4$, $f_{RES}/5$, $f_{RES}/6$, fres/8 includes zero detection circuit Clock disable	target frequency: 16 kHz

UART (2 channel) U-Timer (1 per UART)	serial I/O port for performing asynchronous (start-stop synchronization) communication full duplex, double buffering supports multi-processor mode variable data length (7/8 bit) 1 or 2 stop bits error detection function (parity, framing, overrun) interrupt function NRZ type transfer format baud rate generated by U-Timer 16-bit timer to generate the required UART clock: $f_{RES}/2^5,\ldots,\sim f_{RES}/2^{21}$ (asynchr. mode) Clock disable	polarity of the port signals for receive and transmit is programmable
Real Time Clock (RTC) (Watch Timer)	facility to correct oscillation deviation read/write accessible second/minute/hour registers can signal interrupts every second/minute/hour/day internal clock divider and prescaler provide exact 1s clock this clock is based on the 4 MHz oscillator or if the subclock option is selected on the 32 kHz subclock Clock disable	On MB91F376GS the RTC module is connected to the 4 MHz oscillator.

1.4 Pin Assignment MB91F376GS



1.5 I/O Pins and Their Functions

Table 1.5a Pinning

Pin No. QFP120	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
1	VDD				
2	VSS				
3	PJ4	I/O	PJ4	A	Digital IO-Port
4	PJ5	I/O	PJ5	A	Digital IO-Port
5	PJ6	I/O	PJ6	A	Digital IO-Port
6	PJ7	I/O	PJ7	A	Digital IO-Port
7	PI3	I/O	PI3	A	Digital IO-Port
8	VDD				
9	VSS				
10	SGO	I/O	PM0	A	Sound Gen. SGO
11	SGA	I/O	PM1	A	Sound Gen. SGA
12	SDA	I/O	PM2	Y	I2C SDA
13	SCL	I/O	PM3	Y	I2C SCL
14	VDD				
15	VSS				
16	AVRH			R	Analog Voltage Ref. high
17	AVCC				Analog VCC
18	AVSS/AVRL				Ana.Volt.Ref.low/An.VSS
19	AN0	I/O	PH0	B	ADC input
20	AN1	I/O	PH1	B	ADC input
21	AN2	I/O	PH2	B	ADC input
22	AN3	I/O	PH3	B	ADC input
23	AN4	I/O	PH4	B	ADC input
24	AN5	I/O	PH5	B	ADC input
25	AN6	I/O	PH6	B	ADC input
26	AN7	I/O	PH7	B	ADC input
27	N.C.				not connected pin
28	N.C.				not connected pin
29	ALARM	I		D	Alarm Comparator Input
30	VSS				
31	BOOT	I/O	P93	A	BOOT pin
32	TESTX	I		E	Test mode pin
33	CPUTESTX	I		E	Test mode pin
34	VDD				
35	X0	I		H	4 MHz Oscillator Pin
36	X1	O		H	4 MHz Oscillator Pin
37	VSS				
38	MONCLK	O		G	Clock output
39	INT0	I/O	PK0	A	Ext. Interrupt
40	INT1	I/O	PK1	A	Ext. Interrupt
41	INT2	I/O	PK2	A	Ext. Interrupt
42	INT3	I/O	PK3	A	Ext. Interrupt
43	INT4	I/O	PK4	A	Ext. Interrupt
44	INT5	I/O	PK5	A	Ext. Interrupt

Table 1.5a Pinning

Pin No. QFP120	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
45	INT6	I/O	PK6	A	Ext. Interrupt
46	INT7	I/O	PK7	A	Ext. Interrupt
47	VDD				supply pin for internal voltage regulator
48	VCC3/C				Capacitor pin for internal voltage reg.
49	VSS				
50	IN0	I/O	PL0	A	ICU input
51	IN1	I/O	PL1	A	ICU input
52	IN2	I/O	PL2	A	ICU input
53	IN3	I/O	PL3	A	ICU input
54	OUT0	I/O	PL4	A	OCU Output
55	OUT1	I/O	PL5	A	OCU Output
56	VDD				supply pin for internal voltage regulator
57	MD0	I		T	Mode Pin
58	MD1	I		T	Mode Pin
59	MD2	I		T	Mode Pin
60	INITX	I		U	Initial
61	VDD				supply pin for internal voltage regulator
62	VSS				
63	SOT4	I/O	PN0	A	SIO output
64	SIN4	I/O	PN1	A	SIO input
65	SCK4	I/O	PN2	A	SIO clock
66	SIN3	I/O	PN3	A	SIO input
67	SOT3	I/O	PN4	A	SIO output
68	SCK3	I/O	PN5	A	SIO clock
69	VSS				
70	OCPA0	I/O	PO0	A	PPG output
71	OCPA1	I/O	PO1	A	PPG output
72	OCPA2	I/O	PO2	A	PPG output
73	OCPA3	I/O	PO3	A	PPG output
74	OCPA4	I/O	PO4	A	PPG output
75	OCPA5	I/O	PO5	A	PPG output
76	OCPA6	I/O	PO6	A	PPG output
77	OCPA7	I/O	PO7	A	PPG output
78	TX0	I/O	PP0	Q	CAN TX output
79	RX0	I/O	PP1	Q	CAN RX output
80	TX1	I/O	PP2	Q	CAN TX output
81	RX1	I/O	PP3	Q	CAN RX output
82	VDD				
83	VSS				
84	SIN0	I/O	PQ0	A	UART input
85	SOT0	I/O	PQ1	A	UART output
86	SIN1	I/O	PQ2	A	UART input
87	SOT1	I/O	PQ3	A	UART output
88	PG0	I/O	PG0	A	Digital IO-Port
89	PG1	I/O	PG1	A	Digital IO-Port
90	PG2	I/O	PG2	A	Digital IO-Port
91	PG3	I/O	PG3	A	Digital IO-Port

Table 1.5a Pinning

Pin No. QFP120	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
92	PG4	I/O	PG4	A	Digital IO-Port
93	PG5	I/O	PG5	A	Digital IO-Port
94	VDD				
95	HVSS				SMC VSS
96	PWM1P0	I/O	PR0	K	SMC 0
97	PWM1M0	I/O	PR1	K	SMC 0
98	PWM2P0	I/O	PR2	K	SMC 0
99	PWM2M0	I/O	PR3	M	SMC 0
100	HVDD				SMC VDD
101	PWM1P1	I/O	PR4	K	SMC 1
102	PWM1M1	I/O	PR5	K	SMC 1
103	PWM2P1	I/O	PR6	K	SMC 1
104	PWM2M1	I/O	PR7	M	SMC 1
105	HVSS				SMC VSS
106	PWM1P2	I/O	PS0	K	SMC 2
107	PWM1M2	I/O	PS1	K	SMC 2
108	PWM2P2	I/O	PS2	K	SMC 2
109	PWM2M2	I/O	PS3	M	SMC 2
110	HVDD				SMC VDD
111	PWM1P3	I/O	PS4	K	SMC 3
112	PWM1M3	I/O	PS5	K	SMC 3
113	PWM2P3	I/O	PS6	K	SMC 3
114	PWM2M3	I/O	PS7	M	SMC 3
115	HVSS				
116	VDD				
117	PJ0	I/O	PJ0	A	Digital IO-Port
118	PJ1	I/O	PJ1	A	Digital IO-Port
119	PJ2	I/O	PJ2	A	Digital IO-Port
120	PJ3	I/O	PJ3	A	Digital IO-Port

Remark: Pin 31 (BOOT) should be low by default (pull down resistor).
To avoid disturbances in case of reset/boot it should preferably only be used as output by any application.

Table 1.5b Circuit Types

Circuit Type	Description
A	I/O, IOH=4 mA / IOL=4 mA, CMOS Automotive Hysteresis Input, STOP control
B	I/O, IOH=4 mA / IOL=4 mA, CMOS Automotive Hysteresis Input, Analog Input, STOP control
D	Analog Input
E	CMOS Hysteresis Input, 50K Pull-up
G	Tristate Output, IOH=4 mA / IOL=4 mA
H	4 MHz Oscillator Pin
I	32KHz Oscillator Pin
K	I/O, IOH=30 mA / IOL=30 mA, CMOS Automotive Hysteresis Input, STOP control, slew rate improved for EMC (in SMC mode)
M	I/O, IOH=30 mA / IOL=30 mA, CMOS Automotive Hysteresis Input, Analog Input, STOP control, slew rate improved for EMC (in SMC mode)
Q	I/O, IOH=4 mA / IOL=4 mA, CMOS Input, STOP control
R	AVRH Input
T	CMOS Input, can withstand V_{ID} for flash programming
U	CMOS Hysteresis Input, 50K Pull-up, 3V and 5V input to core
Y	I/O, IOH=3mA / IOL=3mA (I2C), CMOS Input, STOP control

1.6 Flash Memory Mode of MB91F376GS

To enter the flash memory mode set mode pins MD0 to MD2 to “111”. Assert INITX for at least 500 ns to enter this mode.

The following tables show the pins which are required for the programming procedure and also describe the states for the pins not used in flash memory mode. Most of the not used pins are in their reset state (high-Z outputs, enabled inputs). To prevent misbehavior or damage these pins must be tied to VDD or VSS through resistors - see following tables for details.
Aside from the functional pins described below all power pins should be connected to a power supply in the specified range, capacitances should be connected to the VCC3C pin as recommended.

Table 1: Flash Control Signals

MB91F376GS			MBM29LV800C	Notes
Pin number	Normal function	Flash Memory mode		
31	BOOT	$\overline{WE}$	$\overline{WE}$	
32	TESTX	$\overline{BYTE}$	$\overline{BYTE}$	
33	CPUTESTX	TMODX		pull up
38	MONCLK	RY/$\overline{BY}$	RY/$\overline{BY}$	
39-46	INT0-INT7	D24 to D31	DQ8 to DQ15	
50	IN0	$\overline{CE}$	$\overline{CE}$	
51	IN1	$\overline{OE}$	$\overline{OE}$	
52	IN2	D20	DQ4	
53	IN3	D21	DQ5	
54	OUT0	D22	DQ6	
55	OUT1	D23	DQ7	
57	MD0	VDA9	A9 (V_{ID})	
58	MD1	VDRS	$\overline{RESET}$ (V_{ID})	
59	MD2	VDOE	$\overline{OE}$ (V_{ID})	
60	INITX	$\overline{RESET}$	$\overline{RESET}$	
91-93	PG3-PG5	A16-A18	A15-A17	
88	PG0	A20		pull up
89	PG1	A19	A18	
96	PWM1P0	A0	A-1	

Table 1: Flash Control Signals

MB91F376GS			MBM29LV800C	Notes
Pin number	Normal function	Flash Memory mode		
97	PWM1M0	A1	A0	
98	PWM2P0	A2	A1	
99	PWM2M0	A3	A2	
101	PWM1P1	A4	A3	
102	PWM1M1	A5	A4	
103	PWM2P1	A6	A5	
104	PWM2M1	A7	A6	
106	PWM1P2	A8	A7	
107	PWM1M2	A9	A8	
108	PWM2P2	A10	A9	
109	PWM2M2	A11	A10	
111	PWM1P3	A12	A11	
112	PWM1M3	A13	A12	
113	PWM2P3	A14	A13	
114	PWM2M3	A15	A14	
117 to 120	PJ0-PJ3	D16 to D19	DQ0 to DQ3	

Table 2: Pins not used in Flash Memory Mode

MB91F376GS			
Pin number	Normal function	Pin State	Notes
35	X0	input	pull up
36	X1	output	leave open
66	SIN3	output	leave open
67	SOT3	output	leave open
68	SCK3	output	leave open
29	ALARM	input	pull up
all other signals		input	pull up

CHAPTER 2 IO-Map

see Appendix A.

The addresses shown in this table for CAN registers are based on the settings for CS7 done in the Boot ROM

CHAPTER 3 Interrupt Vector Table

see Appendix B

CHAPTER 4 Power-on-sequence

All VDD pins should be connected to the same potential. The analogue supply voltage (AVCC) must not be turned on before the digital supply voltage.

Immediately after power on always execute INIT at the INITX pin (input a low level to the INITX pin). Hold this low level at the INITX pin long enough so that after release of the low level at INITX and the passing of the built in waiting time stable oscillation of the oscillation circuit is achieved. INITX must be pulled low for at least 8 cycles of the 4 MHz oscillation clock.

CHAPTER 5 Handling of Unused Input Pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be tied to VDD or VSS through resistors. In this case those resistors should be more than 2 KOhm.

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

The resistor of more than 2 KOhm is used to limit currents through the protection diodes. In case of voltages at the unused pin of 0.3 V or more below VSS or 0.3 V or more above VDD currents which could cause latch-up will flow through those diodes. It is possible to use one resistor to connect several pins to VDD or VSS. Care should be taken not to connect pins from different supply voltage domains to one resistor.

CHAPTER 6 Emulation Device

MB91FV360GA can be used as an emulation device for MB91F376GS. MB91F376GS uses the following resources of MB91FV360G (see MB91FV360GA IO-Map):

- Reload Timer 0 - Reload Timer 5
- UART 0 / U-Timer 0 - UART 1 / U-Timer 1
- SIO 0 - SIO 1 and their Prescalers; when emulating DMA to/from the SIOs on MB91FV360GA the restrictions given in DDI3200008 have to be observed
- I^2C (100KHz and 400KHz)
- A/D Converter (channels 0 - 7)
- Input Capture 0 - Input Capture 3
- Output Compare 0 - Output Compare 1
- Free Running Counter 0 - Free Running Counter 1
- Stepper Motor Controllers 0 - 3
- Sound Generator
- Real Time Clock
- Programmable Pulse Generators: PWM Control 0 -1, PWM channels 0 - 7
- Power down reset
- Alarm Comparator
- CAN0 - CAN 1
- User RAM 16KB: address range: 03:C000-03:FFFF
- F-Bus RAM 16KB: address range: 04:0000-04:3FFF
- I-RAM 4KB: address range: 01:1000-01:1FFF

The complete size of the flash memory of 768K can only be emulated by using external emulation RAM.

The modified watchdog behaviour - no more clearing of the watchdog reset generation flag in case of DMA to D-bus and I-Bus, instruction fetch from D-bus RAM and data operations on I-bus RAM - cannot be emulated on MB91FV360GA.

CHAPTER 7 Package

A QFP-120 package called FPT-120P-M21 (0.5 mm pin pitch) will be used for MB91F376GS.
The thermal resistance of this package is 30 degr. C/W when used on a multi-layer board with separate power and ground planes.

Thermal resistance [degr. C/W]			
theta-ja (junction to ambient)			theta-jc (junction to case)
0 m/s	1 m/s	3 m/s	
30	27	25	5

The maximum allowed ambient temperature is 85 degr. C, the maximum allowed junction temperature is 125 degr.C. Under these conditions a maximum power consumption of (125 degr. C - 85 degr. C) / 30 C/W = 1.33 W is allowed. The user must make sure that the maximum ambient temperature is not exceeded.

For other details about the package see Fujitsu Semiconductor Package Data Book.

CHAPTER 8 Electrical specification

See documentation for MB91F376G.

Appendix A I/O Map

Table A lists the addresses for the registers used by the internal peripheral functions of MB91F376GS.

- How to Read the I/O Map

Address	Register				Internal peripheral
	+0	+1	+2	+3	
000014H	PDRG [R/W]	PDRH [R/W]	PDRI [R/W]	—	Port data register
	XXXXXXXX	XXXXXXXX	----XXXX		

Read/write attribute
Register initial value after a reset (bit initial values)
"1": initial value "1", "0": initial value "0",
"x": initial value "X" (indeterminate),
"—" indicates non-existent bits
Register name (The register in column 1 is at location 4n, the register in column 2 at 4n+1, and so on.)
Location of far left of register (+0). +1, +2, and +3 each increment the location by one. When performing word access, the register in column 1 is placed at the MSB end of the data.

Precautions:

- Do not use RMW instructions on registers containing write-only (W) bits.

RMW instructions(RMW:read-modify-write)

```
AND   Rj, @Ri      OR    Rj, @Ri      EOR   Rj, @Ri
ANDH  Rj, @Ri      ORH   Rj, @Ri      EORH  Rj, @Ri
ANDB  Rj, @Ri      ORB   Rj, @Ri      EORB  Rj, @Ri
BANDL #u4, @Ri     BORL  #u4, @Ri     BEORL #u4, @Ri
BANDH #u4, @Ri     BORH  #u4, @Ri     BEORH #u4, @Ri
```

- The data in reserved areas and areas marked "—" is indeterminate. Do not use those areas !

Address	Register				Block
	+0	+1	+2	+3	
000000H	Reserved				T-unit Port Data Register
000004H	Reserved				
000008H	Reserved				
00000CH	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
000010H	PDRG [R/W] XXXXXXXX	PDRH [R/W] XXXXXXXX	PDRI [R/W] X - - - X - - -	PDRJ [R/W] XXXXXXXX	R-bus Port Data Register
000014H	PDRK [R/W] XXXXXXXX	PDRL [R/W] XXXXXXXX	PDRM [R/W] - - - - XXXX	PDRN [R/W] - - XXXXXX	
000018H	PDRO [R/W] XXXXXXXX	PDRP [R/W] ----XXXX	PDRQ [R/W] - - XXXXX	PDRR [R/W] XXXXXXXX	
00001CH	PDRS [R/W] XXXXXXXX				
000020H | 00003CH					Reserved
000040H	EIRR [R/W] 00000000	ENIR [R/W] 00000000	ELVR [R/W] 00000000 00000000		Ext int/NMI
000044H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	CLKR2 [R/W] - - - - - - 000	reserved	DLYI/I-unit RTC
000048H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
00004CH	_____		TMCSR0 [R/W] - - - - 0000 - - - 00000		
000050H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
000054H	_____		TMCSR1 [R/W] - - - - 0000 - - - 00000		
000058H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2
00005CH	_____		TMCSR2 [R/W] - - - - 0000 - - - 00000		
000060H	SSR0 [R/W] 00001 - 00	SIDR0 [R/W] XXXXXXXX	SCR0 [R/W] 00000100	SMR0 [R/W] 00 - - 0 - 0 -	UART0
000064H	ULS0 [R/W] - - - - 0000				
000068H	UTIM0/UTIMR0 [R/W] 00000000 00000000		DRCL0 [W] - - - - - - - -	UTIMC0 [R/W] 0 - - - 0 - 01	U-TIMER 0
00006CH	SSR1 [R/W] 00001 - 00	SIDR1 [R/W] XXXXXXXX	SCR1 [R/W] 00000100	SMR1 [R/W] 00 - - 0 - 0 -	UART1
000070H	ULS1 [R/W] - - - - 0000				
000074H	UTIM1/UTIMR1 [R/W] 00000000 00000000		DRCL1 [W] - - - - - - - -	UTIMC1 [R/W] 0 - - - - - 01	U-TIMER 1
000078H	_____				Reserved
00007CH					

Address	Register				Block
	+0	+1	+2	+3	
000080H	_____				Reserved
000084H	SMCS0 [R/W] 00000010 - - - - 00-0				SIO 0
			SES0 [R/W] - - - - - - 00	SDR0 [R/W] 00000000	
000088H	SMCS1 [R/W] 00000010 - - - - 00 - 0		SES1 [R/W] - - - - - - 00	SDR1 [R/W] 00000000	SIO 1
00008CH	CDCR0 [R/W] 0 - - - 1111	Reserved	CDCR1 [R/W] 0 - - - 1111	Reserved	SIO 0/1 Prescaler
000090H					Reserved
000094H	IBCR [R/W] 00000000	IBSR [R] 00000000	IADR [R/W] -XXXXXXX	ICCR [R/W] - - 0XXXXX	I2C (old) -> new I2C from address 0x184
000098H		IDAR [R/W] XXXXXXXX		IDBL [R/W] -------0	
00009CH	ADMD [R/W,W] - - - -0000	ADCH [R/W] 00000000		ADCS [R/W,W] 0000 - - 00	A/D Converter
0000A0H	ADCD [R/W] 000000XX XXXXXXXX			ADBL [R/W] - - - - - - - 0	
0000A4H	reserved				
0000A8H					
0000ACH	IOTDBL0 [R/W] - - - - - 000	ICS01 [R/W] 00000000	IOTDBL1 [R/W] - - - - - 000	ICS23 [R/W] 00000000	Input Capture 0,1,2,3
0000B0H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
0000B4H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
0000B8H	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		reserved		Output Com-pare 0,1
0000BCH	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
0000C0H					Reserved
0000C4H					Reserved
0000C8H	TCDT0 [R/W] XXXXXXXX XXXXXXXX		_____	TCCS0 [R/W] - 0000000	Free Running Counter 0 for ICU/OCU
0000CCH	TCDT1 [R/W] XXXXXXXX XXXXXXXX		_____	TCCS1 [R/W] - 0000000	Free Running Counter 1 for ICU/OCU
0000D0H	ZPD0 [R/W,R] 00000010	PWC0 [R/W] - - 000 - - 0	ZPD1 [R/W,R] 00000010	PWC1 [R/W] 00000 - - 0	SMC 0,1

Address	Register				Block
	+0	+1	+2	+3	
0000D4H	ZPD2 [R/W,R] 00000010	PWC2 [R/W] - - 000 - - 0	ZPD3 [R/W,R] 00000010	PWC3 [R/W] 00000 - - 0	SMC 2,3
0000D8H	PWC20 [R/W] XXXXXXXX	PWC10 [R/W] XXXXXXXX	PWS20 [R/W] - 0000000	PWS10 [R/W] - - 000000	SMC 0
0000DCH	PWC21 [R/W] XXXXXXXX	PWC11 [R/W] XXXXXXXX	PWS21 [R/W] - 0000000	PWS11 [R/W] - - 000000	SMC 1
0000E0H	PWC22 [R/W] XXXXXXXX	PWC12 [R/W] XXXXXXXX	PWS22 [R/W] - 0000000	PWS12 [R/W] - - 000000	SMC 2
0000E4H	PWC23 [R/W] XXXXXXXX	PWC13 [R/W] XXXXXXXX	PWS23 [R/W] - 0000000	PWS13 [R/W] - - 000000	SMC 3
0000E8H	SMDBL0 [R/W] - - - - - - - 0	SMDBL1 [R/W] - - - - - - 0	SMDBL2 [R/W] - - - - - - - 0	SMDBL3 [R/W] - - - - - - - 0	SMC 0,1,2,3
0000ECH		SGDBL [R/W] - - - - - - - 0	SGCR [R/W] 0 - - - - - 00 000 - - 000		Sound generator
0000F0H	SGAR [R/W] 00000000	SGFR [R/W] XXXXXXXX	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
0000F4H		WTDBL [R/W] - - - - - - - 0	WTCR [R/W] 00000000 000 - 0000		Real Time Clock (Watch Timer)
0000F8H		WTBR [R/W] - - XXXXXX XXXXXXXX XXXXXXXX			
0000FCH	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000		
000100H	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3
000104H	_____		TMCSR3 [R/W] - - - - XX - - - - - XXXXX		
000108H	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4
00010CH	_____		TMCSR4 [R/W] - - - - XX - - - - - XXXXX		
000110H	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5
000114H	_____		TMCSR5 [R/W] - - - - XX - - - - - XXXXX		
000118H	GCN10 [R/W] 00110010 00010000		PDBL0 [R/W] - - - -0000	GCN20 [R/W] - - - - 0000	PWM Control 0
00011CH	GCN11 [R/W] 00110010 00010000		PDBL1 [R/W] - - - -0000	GCN21 [R/W] - - - - 0000	PWM Control 1
000120H	PTMR0 [R] 11111111 11111111		PCSR0 [W] XXXXXXXX XXXXXXXX		PWM0
000124H	PDUT0 [W] XXXXXXXX XXXXXXXX		PCNH0 [R/W] 0000000 -	PCNL0 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
000128H	PTMR1 [R] 11111111 11111111		PCSR1 [W] XXXXXXXX XXXXXXXX		PWM1
00012CH	PDUT1 [W] XXXXXXXX XXXXXXXX		PCNH1 [R/W] 0000000 -	PCNL1 [R/W] 000000 - 0	
000130H	PTMR2 [R] 11111111 11111111		PCSR2 [W] XXXXXXXX XXXXXXXX		PWM2
000134H	PDUT2 [W] XXXXXXXX XXXXXXXX		PCNH2 [R/W] 0000000 -	PCNL2 [R/W] 000000 - 0	
000138H	PTMR3 [R] 11111111 11111111		PCSR3 [W] XXXXXXXX XXXXXXXX		PWM3
00013CH	PDUT3 [W] XXXXXXXX XXXXXXXX		PCNH3 [R/W] 0000000 -	PCNL3 [R/W] 000000 - 0	
000140H	PTMR4 [R] 11111111 11111111		PCSR4 [W] XXXXXXXX XXXXXXXX		PWM4
000144H	PDUT4 [W] XXXXXXXX XXXXXXXX		PCNH4 [R/W] 0000000 -	PCNL4 [R/W] 000000 - 0	
000148H	PTMR5 [R] 11111111 11111111		PCSR5 [W] XXXXXXXX XXXXXXXX		PWM5
00014CH	PDUT5 [W] XXXXXXXX XXXXXXXX		PCNH5 [R/W] 0000000 -	PCNL5 [R/W] 000000 - 0	
000150H	PTMR6 [R] 11111111 11111111		PCSR6 [W] XXXXXXXX XXXXXXXX		PWM6
000154H	PDUT 6 [W] XXXXXXXX XXXXXXXX		PCNH6 [R/W] 0000000 -	PCNL6 [R/W] 000000 - 0	
000158H	PTMR7 [R] 11111111 11111111		PCSR7 [W] XXXXXXXX XXXXXXXX		PWM7
00015CH	PDUT7 [W] XXXXXXXX XXXXXXXX		PCNH7 [R/W] 0000000 -	PCNL7 [R/W] 000000 - 0	
000160H					Reserved
000164H	CMCR [R/W] 11111111 0000000		CMPR [R/W] ----1001 1---0001		Clock Modulation
000168H	CMLS0 [R/W] 01110111 1111111		CMLS1 [R/W] 01110111 1111111		
00016CH	CMLS2 [R/W] 01110111 1111111		CMLS3 [R/W] 01110111 1111111		
000170H	CMLT0 [R/W] -----100 00000010		CMLT1 [R/W] 11110100 00000010		
000174H	CMLT2 [R/W] -----100 00000010		CMLT3 [R/W] -----100 00000010		
000178H	CMAC [R/W] 11111111 1111111		CMTS [R/W] --000001 01111111		

Address	Register				Block
	+0	+1	+2	+3	
00017CH		PDRCR [R/W] - - - - - 000			Power down reset
000180H	ACCDBL[R/W] - - - - - - - 0	ACSR [R/W] - - - XXX00			Alarm comparator
000184H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH [R/W] - - - - - - 00	ITBAL [R/W] 00000000	I2C (new) (*) old and new I2C share this bit!
000188H	ITMKH [R/W] 00 - - - - 11	ITMKL [R/W] 11111111	ISMK [R/W] 01111111	ISBA [R/W] - 0000000	
00018CH	IDARH [-] 00000000	IDAR2 [R/W] 00000000	ICCR2 [R/W] - 0011111	IDBL2(*) [R/W] - - - - - - - 0	
000190H	CUCR [R/W] - - - - - - - - - - - - 0 - -00		CUTD [R/W] 10000000 00000000		not available on MB91F376GSS
000194H	CUTR1 [R] -------- 00000000		CUTR2 [R] 00000000 00000000		
000198H | 0001F8H	----------				Reserved
0001FCH			F362MD [R/W] 00000000		F362 Mode Reg

Address	Register				Block
	+0	+1	+2	+3	
000200H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020CH	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228H | 00023CH	_____				
000240H	DMACR [R/W] 0--00000 -------- -------- --------				
000244H | 0003ECH	_____				Reserved
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
000400H	DDRG [R/W] 00000000	DDRH [R/W] 00000000	DDRI [R/W] ----0---	DDRJ [R/W] 00000000	R-bus Port Direction Register
000404H	DDRK [R/W] 00000000	DDRL [R/W] 00000000	DDRM [R/W] ----0000	DDRN [R/W] --000000	
000408H	DDRO [R/W] 00000000	DDRP [R/W] ----0000	DDRQ [R/W] --000000	DDRR [R/W] 00000000	
00040CH	DDRS [R/W] 00000000				
000410H	PFRG [R/W] 00000000	PFRH [R/W] 00000000	PFRI [R/W] ----0---	PFRJ [R/W] 00000000	R-bus Port Function Register
000414H	PFRK [R/W] 00000000	PFRL [R/W] 00000000	PFRM [R/W] ----0000	PFRN [R/W] --000000	
000418H	PFRO [R/W] 00000000	PFRP [R/W] ----0000	PFRQ [R/W] --000000	PFRR [R/W] 00000000	
00041CH	PFRS [R/W] 00000000				
000420H | 00043CH	_____				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000440H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Control unit
000444H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
00044CH	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
00045CH	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
00046CH	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470H | 00047CH	_____				
000480H	RSRR [R/W] 10000-00	STCR [R/W] 00110011	TBCR [R/W] X0000X00	CTBR [W] XXXXXXXX	Clock Control unit
000484H	CLKR [R/W] 00000000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488H | 00063CH	_____				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000640H	ASR0 [W] 00000000 00000000		AMR0 [W] 11111000 11111111		T-unit
000644H	ASR1 [W] 00000000 00000000		AMR1 [W] 00000000 00000000		
000648H	ASR2 [W] 00000000 00000000		AMR2 [W] 00000000 00000000		
00064CH	ASR3 [W] 00000000 00000000		AMR3 [W] 00000000 00000000		
000650H	ASR4 [W] 00000000 00000000		AMR4 [W] 00000000 00000000		
000654H	ASR5 [W] 00000000 00000000		AMR5 [W] 00000000 00000000		
000658H	ASR6 [W] 00000000 00000000		AMR6 [W] 00000000 00000000		
00065CH	ASR7 [W] 00000000 00000000		AMR7 [W] 00000000 00000000		
000660H	AMD0 [R/W] -00XX111	AMD1 [R/W] -XXXXXXX	AMD2 [R/W] --XXXXXX	AMD3 [R/W] --XXXXXX	
000664H	AMD4 [R/W] --XXXXXX	AMD5 [R/W] --XXXXXX	AMD6 [R/W] -XXXXXXX	AMD7 [R/W] -XXXXXXX	
000668H	CSE 11000011	_____	_____	_____	
00066CH	_____		_____		
000670H	CHE 11111111	_____	_____		
000674H | 0007F8H	_____				Reserved
0007FCH	_____	MODR [W] XXXXXXXX	_____	_____	Mode Register
000800H | 000B6CH	_____				Reserved

Address	Register				Block
	+0	+1	+2	+3	
001000H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100CH	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101CH	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028H | 006FFCH	_____				Reserved
007000H	FMCS [R/W] 0110X000	_____	_____	_____	Flash Memory Control Register
007004H	FMWT [R/W] -0010011	_____	_____	_____	
007008H | 010FFCH	_____				Reserved
011000H | 011FFCH	_____				I-RAM 4 kB
012000H | 03BFFCH	_____				Reserved
03C000H | 03FFFCH					User RAM 16 kB (D-Bus)
040000H | 043FFCH					Fast RAM 16 kB (F-Bus)

Address	Register				Block
	+0	+1	+2	+3	
044000H | 0447FCH					Boot ROM 2 kB (F-Bus)
044800H | 05FFFCH	Sector 0 (partly) 56 KB		Sector 2 (partly) 56 KB		Flash Memory 768 K on F-Bus
060000H | 07FFFCH	Sector 1 64 KB		Sector 3 64 KB		
080000H | 09FFFCH	Sector 4 64 KB		Sector 11 64 KB		
0A0000H | 0BFFFC	Sector 5 64 KB		Sector 12 64 KB		
0C0000H | 0DFFFC	Sector 6 64 KB		Sector 13 64 KB		
0E0000H | 0EFFFC	Sector 7 32 KB		Sector 14 32 KB		
0F0000H | 0F3FFCH	Sector 8 8 KB		Sector 15 8 KB		
0F4000H | 0F7FFCH	Sector 9 8 KB		Sector 16 8 KB		
0F8000H | 0FFFFCH	Sector 10 16 KB		Sector 17 16 KB		
	Fixed Mode and Reset Vector				
100000H | 11FFFCH	Sector 0 - mirrored 64 KB		Sector 2 - mirrored 64 KB		
120000H | 13FFFCH	Sector 1 - mirrored 64 KB		Sector 3 - mirrored 64 KB		

Address	Register				Block
	+0	+1	+2	+3	
200000H	BVALR0 [R/W] 00000000 00000000		TREQR0 [R/W] 00000000 00000000		CAN 0 Remark: Address range for CAN 0 to CAN 1 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
200004H	TCANR0 [W] 00000000 00000000		TCR0 [R/W] 00000000 00000000		
200008H	RCR0 [R/W] 00000000 00000000		RRTRR0 [R/W] 00000000 00000000		
20000CH	ROVRR0 [R/W] 00000000 00000000		RIER0 [R/W] 00000000 00000000		
200010H	CSR0 [R/W] 00000000 00000001			LEIR0 [R/W] 000-0000	
200014H	RTEC0 [R] 00000000 00000000		BTR0 [R/W] -1111111 11111111		
200018H	IDER0 [R/W] XXXXXXXX XXXXXXXX		TRTRR0 [R/W] 00000000 00000000		
20001CH	RFWTR0 [R/W] XXXXXXXX XXXXXXXX		TIER0 [R/W] 00000000 00000000		
200020H	AMSR0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200024H	AMR00 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200028H	AMR10 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20002CH | 200048H	GENERAL PURPOSE RAM [R/W]				
20004CH	IDR00 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200050H	IDR10 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200054H	IDR20 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200058H	IDR30 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20005CH	IDR40 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200060H	IDR50 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200064H	IDR60 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
200068H	IDR70 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				CAN 0
20006CH	IDR80 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200070H	IDR90 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200074H	IDR100 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200078H	IDR110 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20007CH	IDR120 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200080H	IDR130 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200084H	IDR140 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200088H	IDR150 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20008CH	DLCR00 [R/W] -------- ----XXXX		DLCR10 [R/W] -------- ----XXXX		
200090H	DLCR20 [R/W] -------- ----XXXX		DLCR30 [R/W] -------- ----XXXX		
200094H	DLCR40 [R/W] -------- ----XXXX		DLCR50 [R/W] -------- ----XXXX		
200098H	DLCR60 [R/W] -------- ----XXXX		DLCR70 [R/W] -------- ----XXXX		
20009CH	DLCR80 [R/W] -------- ----XXXX		DLCR90 [R/W] -------- ----XXXX		
2000A0H	DLCR100 [R/W] -------- ----XXXX		DLCR110 [R/W] -------- ----XXXX		
2000A4H	DLCR120 [R/W] -------- ----XXXX		DLCR130 [R/W] -------- ----XXXX		
2000A8H	DLCR140 [R/W] -------- ----XXXX		DLCR150 [R/W] -------- ----XXXX		
2000ACH	DTR00 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000B4H	DTR10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
2000BCH	DTR20 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 0
2000C4H	DTR30 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000CCH	DTR40 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000D4H	DTR50 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000DCH	DTR60 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000E4H	DTR70 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000ECH	DTR80 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000F4H	DTR90 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000FCH	DTR100 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200104H	DTR110 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20010CH	DTR120 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200114H	DTR130 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20011CH	DTR140 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200124H	DTR150 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20012CH	CREG0 [R/W] 00000000 00000110				

Address	Register				Block
	+0	+1	+2	+3	
200200H	BVALR1 [R/W] 00000000 00000000		TREQR1 [R/W] 00000000 00000000		CAN 1 Remark: Address range for CAN 0 to CAN 1 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
200204H	TCANR1 [W] 00000000 00000000		TCR1 [R/W] 00000000 00000000		
200208H	RCR1 [R/W] 00000000 00000000		RRTRR1 [R/W] 00000000 00000000		
20020CH	ROVRR1 [R/W] 00000000 00000000		RIER1 [R/W] 00000000 00000000		
200210H	CSR1 [R/W] 00000000 00000001			LEIR1 [R/W] 000-0000	
200214H	RTEC1 [R] 00000000 00000000		BTR1 [R/W] -1111111 11111111		
200218H	IDER1 [R/W] XXXXXXXX XXXXXXXX		TRTRR1 [R/W] 00000000 00000000		
20021CH	RFWTR1 [R/W] XXXXXXXX XXXXXXXX		TIER1 [R/W] 00000000 00000000		
200220H	AMSR1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200224H	AMR01 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200228H	AMR11 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20022CH | 200248H	GENERAL PURPOSE RAM [R/W]				
20024CH	IDR01 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200250H	IDR11 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200254H	IDR21[R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200258H	IDR31 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX-				
20025CH	IDR41 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200260H	IDR51 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200264H	IDR61 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
200268H	IDR71 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				CAN 1
20026CH	IDR81 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200270H	IDR91 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200274H	IDR101 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200278H	IDR111 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20027CH	IDR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXX---				
200280H	IDR131 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200284H	IDR141 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200288H	IDR151 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20028CH	DLCR01 [R/W] -------- ----XXXX		DLCR11 [R/W] -------- ----XXXX		
200290H	DLCR21 [R/W] -------- ----XXXX		DLCR31 [R/W] -------- ----XXXX		
200294H	DLCR41 [R/W] -------- ----XXXX		DLCR51 [R/W] -------- ----XXXX		
200298H	DLCR61 [R/W] -------- ----XXXX		DLCR71 [R/W] -------- ----XXXX		
20029CH	DLCR81[R/W] -------- ----XXXX		DLCR91 [R/W] -------- ----XXXX		
2002A0H	DLCR101 [R/W] -------- ----XXXX		DLCR111 [R/W] -------- ----XXXX		
2002A4H	DLCR121 [R/W] -------- ----XXXX		DLCR131 [R/W] -------- ----XXXX		
2002A8H	DLCR141 [R/W] -------- ----XXXX		DLCR151 [R/W] -------- ----XXXX		
2002ACH	DTR01 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002B4H	DTR11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
2002BCH	DTR21 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 1
2002C4H	DTR31 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002CCH	DTR41 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002D4H	DTR51 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002DCH	DTR61 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002E4H	DTR71 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002ECH	DTR81 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002F4H	DTR91 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002FCH	DTR101 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200304H	DTR111 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20030CH	DTR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200314H	DTR131 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20031CH	DTR141 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200324H	DTR151 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20032CH	CREG1 [R/W] 00000000 00000110				

Appendix B Interrupt Vectors

This appendix lists the interrupt vector table.

The interrupt vector table lists the interrupt vectors and interrupt control registers assigned to each MB91360 interrupt.

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	RN
Reset *6	0	00	-	-	0x3FC	0x000FFFFC	
Mode vector *6	1	01	-	-	0x3F8	0x000FFFF8	
System reserved	2	02	-	-	0x3F4	0x000FFFF4	
System reserved	3	03	-	-	0x3F0	0x000FFFF0	
System reserved	4	04	-	-	0x3EC	0x000FFFEC	
System reserved	5	05	-	-	0x3E8	0x000FFFE8	
System reserved	6	06	-	-	0x3E4	0x000FFFE4	
Co-processor fault trap *4	7	07	-	-	0x3E0	0x000FFFE0	
Co-processor error trap *4	8	08	-	-	0x3DC	0x000FFFDC	
INTE instruction *4	9	09	-	-	0x3D8	0x000FFFD8	
Instruction break exception *4	10	0A	-	-	0x3D4	0x000FFFD4	
Operand break trap *4	11	0B	-	-	0x3D0	0x000FFFD0	
Step trace trap *4	12	0C	-	-	0x3CC	0x000FFFCC	
NMI interrupt(tool)*4	13	0D	-	-	0x3C8	0x000FFFC8	
Undefined instruction exception	14	0E	-	-	0x3C4	0x000FFFC4	
NMI request	15	0F	FH fixed		0x3C0	0x000FFFC0	
External Interrupt 0	16	10	ICR00	0x440	0x3BC	0x000FFFBC	4
External Interrupt 1	17	11	ICR01	0x441	0x3B8	0x000FFFB8	5
External Interrupt 2	18	12	ICR02	0x442	0x3B4	0x000FFFB4	8
External Interrupt 3	19	13	ICR03	0x443	0x3B0	0x000FFFB0	9
External Interrupt 4	20	14	ICR04	0x444	0x3AC	0x000FFFAC	
External Interrupt 5	21	15	ICR05	0x445	0x3A8	0x000FFFA8	
External Interrupt 6	22	16	ICR06	0x446	0x3A4	0x000FFFA4	

External Interrupt 7	23	17	ICR07	0x447	0x3A0	0x000FFFA0	
Reload Timer 0	24	18	ICR08	0x448	0x39C	0x000FFF9C	6
Reload Timer 1	25	19	ICR09	0x449	0x398	0x000FFF98	7
Reload Timer 2	26	1A	ICR10	0x44A	0x394	0x000FFF94	
CAN 0 RX	27	1B	ICR11	0x44B	0x390	0x000FFF90	
CAN 0 TX/NS	28	1C	ICR12	0x44C	0x38C	0x000FFF8C	
CAN 1 RX	29	1D	ICR13	0x44D	0x388	0x000FFF88	
CAN 1 TX/NS	30	1E	ICR14	0x44E	0x384	0x000FFF84	
CAN 2 RX *7	31	1F	ICR15	0x44F	0x380	0x000FFF80	
CAN 2 TX/NS *7	32	20	ICR16	0x450	0x37C	0x000FFF7C	
CAN 3 RX [5]	33	21	ICR17	0x451	0x378	0x000FFF78	
CAN 3 TX/NS [5]	34	22	ICR18	0x452	0x374	0x000FFF74	
PPG 0/1	35	23	ICR19	0x453	0x370	0x000FFF70	
PPG 2/3	36	24	ICR20	0x454	0x36C	0x000FFF6C	
PPG 4/5	37	25	ICR21	0x455	0x368	0x000FFF68	
PPG 6/7	38	26	ICR22	0x456	0x364	0x000FFF64	
Reload Timer 3	39	27	ICR23	0x457	0x360	0x000FFF60	
Reload Timer 4	40	28	ICR24	0x458	0x35C	0x000FFF5C	
Reload Timer 5	41	29	ICR25	0x459	0x358	0x000FFF58	
ICU 0/1	42	2A	ICR26	0x45A	0x354	0x000FFF54	
OCU 0/1	43	2B	ICR27	0x45B	0x350	0x000FFF50	
ICU 2/3	44	2C	ICR28	0x45C	0x34C	0x000FFF4C	
OCU 2/3 *7	45	2D	ICR29	0x45D	0x348	0x000FFF48	
ADC	46	2E	ICR30	0x45E	0x344	0x000FFF44	14
Timebase Overflow	47	2F	ICR31	0x45F	0x340	0x000FFF40	
Free Running Counter 0	48	30	ICR32	0x460	0x33C	0x000FFF3C	
Free Running Counter 1	49	31	ICR33	0x461	0x338	0x000FFF38	
SIO 0	50	32	ICR34	0x462	0x334	0x000FFF34	12
SIO 1	51	33	ICR35	0x463	0x330	0x000FFF30	15
Sound Generator	52	34	ICR36	0x464	0x32C	0x000FFF2C	
UART 0 RX	53	35	ICR37	0x465	0x328	0x000FFF28	0
UART 0 TX	54	36	ICR38	0x466	0x324	0x000FFF24	1
UART 1 RX	55	37	ICR39	0x467	0x320	0x000FFF20	2
UART 1 TX	56	38	ICR40	0x468	0x31C	0x000FFF1C	3

UART 2 RX *7	57	39	ICR41	0x469	0x318	0x000FFF18	10
UART 2 TX *7	58	3A	ICR42	0x46A	0x314	0x000FFF14	11
I2C	59	3B	ICR43	0x46B	0x310	0x000FFF10	13
Alarm Comparator	60	3C	ICR44	0x46C	0x30C	0x000FFF0C	
RTC / Calibration (Watch timer)	61	3D	ICR45	0x46D	0x308	0x000FFF08	
DMA	62	3E	ICR46	0x46E	0x304	0x000FFF04	
Delayed interrupt activation bit	63	3F	ICR47	0x46F	0x300	0x000FFF00	
System reserved *3	64	40	-	-	0x2FC	0x000FFEFC	
System reserved *3	65	41	-	-	0x2F8	0x000FFEF8	
Security vector	66	42			0x2F4	0x000FFEF4	
System reserved	67	43	(ICR51)	0x473	0x2F0	0x000FFEF0	
System reserved	68	44	(ICR52)	0x474	0x2EC	0x000FFEEC	
System reserved	69	45	(ICR53)	0x475	0x2E8	0x000FFEE8	
System reserved	70	46	(ICR54)	0x476	0x2E4	0x000FFEE4	
System reserved	71	47	(ICR55)	0x477	0x2E0	0x000FFEE0	
System reserved	72	48	(ICR56)	0x478	0x2DC	0x000FFEDC	
System reserved	73	49	(ICR57)	0x479	0x2D8	0x000FFED8	
System reserved	74	4A	(ICR58)	0x47A	0x2D4	0x000FFED4	
System reserved	75	4B	(ICR59)	0x47B	0x2D0	0x000FFED0	
System reserved	76	4C	(ICR60)	0x47C	0x2CC	0x000FFECC	
System reserved	77	4D	(ICR61)	0x47D	0x2C8	0x000FFEC8	
System reserved	78	4E	(ICR62)	0x47E	0x2C4	0x000FFEC4	
System reserved	79	4F	(ICR63)	0x47F	0x2C0	0x000FFEC0	
Used by the INT instruction.	80 to 255	50 to FF	-	-	0x2BC to 0x000	0x000FFEBC to 0x000FFC00	

*1 The ICRs are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

*2 The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR). The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (0x000FFC00). The TBR is initialized to this value by a reset.After execution of the internal boot ROM TBR is set to 0x00FFC00.

*3 Used by REALOS

*4 System reserved

*5 Only available on MB91V360/MB91FV360

*6 Mode and reset vector cannot be changed, for their contents see IO map

*7 Not available on MB91F376GS

Remarks:

The 1-Kbyte area from the address specified in TBR is the EIT vector area.

Each vector consists of four bytes. The following formula shows the relationship between the vector number and vector address.

vctadr=TBR + vctofs

= TBR + (3FC$_H$ – 4 × vct)

vctadr:Vector address
vctofs:Vector offset
vct:Vector number