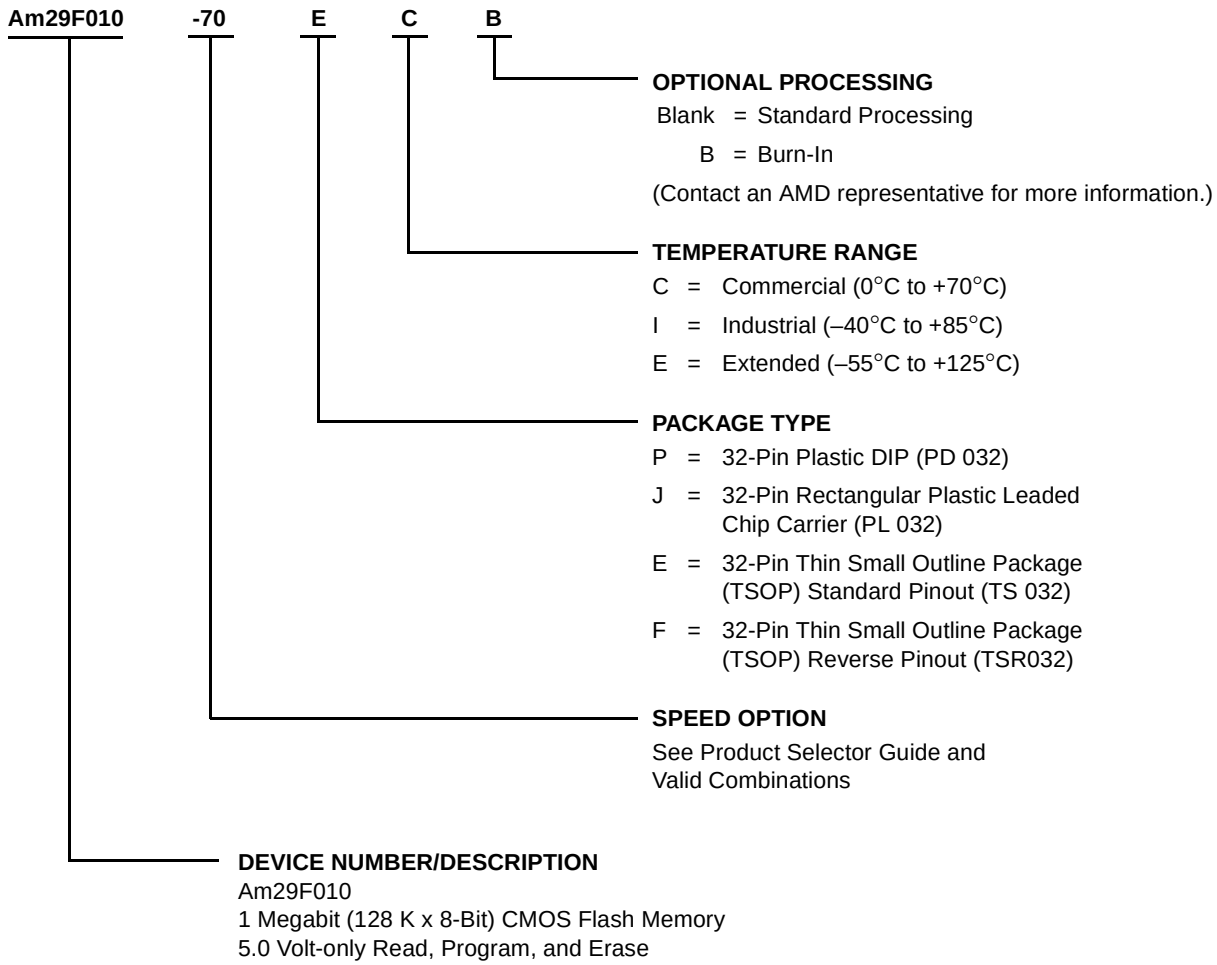
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM29F010-45	PC, PI, PE, JC, JI, JE, EC, EI, EE, FC, FI, FE
AM29F010-55 V_{CC} = 5.0 V ± 5%	PC5, PI5, PE5
AM29F010-55 V_{CC} = 5.0 V ± 10%	JC, JI, JE, EC, EI, EE, FC, FI, FE
AM29F010-70 AM29F010-90 AM29F010-120	PC, PI, PE, JC, JI, JE, EC, EI, EE, FC, FI, FE

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29F010 Device Bus Operations

Operation	CE#	OE#	WE#	Addresses (Note 1)	DQ0–DQ7
Read	L	L	H	A_{IN}	D_{OUT}
Write	L	H	L	A_{IN}	D_{IN}
Standby	V_{CC} ± 0.5 V	X	X	X	High-Z
Output Disable	L	H	H	X	High-Z
Hardware Reset	X	X	X	X	High-Z
Temporary Sector Unprotect	X	X	X	A_{IN}	D_{IN}

Legend:

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0± 0.5 V, X = Don't Care, A_{IN} = Addresses In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:

1. *Addresses are A16:A0.*
2. *The sector protect and sector unprotect functions must be implemented via programming equipment. See the "Sector Protection/Unprotection" section.*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to the Read Operations Timings diagram for the timing waveforms. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. See the "Command Definitions" section for details on erasing a sector or the entire chip.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" and "Autoselect Command Sequence" sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to "Write Operation Status" for more information, and to each AC Characteristics section in the appropriate data sheet for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# pin is held at $V_{CC} \pm 0.5$ V. (Note that this is a more restricted voltage range than V_{IH}.) The device enters the TTL standby mode when CE# is held at V_{IH}. The device requires the standard access time (t_{CE}) before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics tables represents the standby current specification.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Am29F010 Sector Addresses Table

Sector	A16	A15	A14	Address Range
SA0	0	0	0	00000h-03FFFh
SA1	0	0	1	04000h-07FFFh
SA2	0	1	0	08000h-0BFFFh
SA3	0	1	1	0C000h-0FFFFh
SA4	1	0	0	10000h-13FFFh
SA5	1	0	1	14000h-17FFFh
SA6	1	1	0	18000h-1BFFFh
SA7	1	1	1	1C000h-1FFFFh

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Autoselect Codes (High Voltage Method) table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Table 3. Am29F010 Autoselect Codes (High Voltage Method)

Description	CE#	OE#	WE#	A16 to A14	A13 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ7 to DQ0
Manufacturer ID: AMD	L	L	H	X	X	V_{ID}	X	L	X	L	L	01h
Device ID: Am29F010	L	L	H	X	X	V_{ID}	X	L	X	L	H	20h
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	01h (protected)
												00h (unprotected)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

Sector protection/unprotection must be implemented using programming equipment. The procedure requires a high voltage (V_{ID}) on address pin A9 and the control pins. Details on this method are provided in a supplement, publication number 20495. Contact an AMD representative to obtain a copy of the appropriate document.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" for details.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to the Command Definitions table). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.