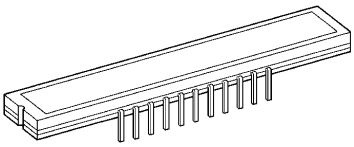
TOSHIBA CCD LINEAR IMAGE SENSOR CCD (Charge Coupled Device)

TCD2253D

The TCD2253D is a high sensitive and low dark current 2700 elements × 3 line CCD color image sensor which includes CCD drive circuit, clamp circuit and sample & hold circuit.
The sensor is designed for scanner. The device contains a row of 2700 elements × 3 line photodiodes which provide a 12 lines / mm (300DPI) across a A4 size paper. The device is operated by 5V pulse and 12V power supply.



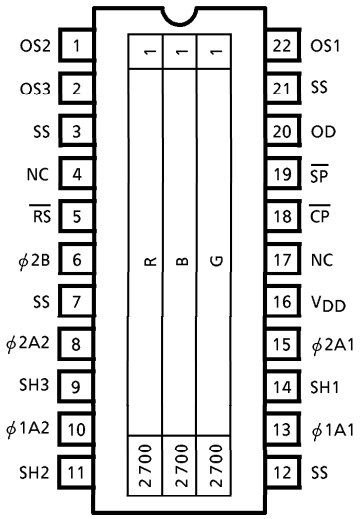
WDIP22-G-400-2.54C

Weight : 4.5g (Typ.)

FEATURES

- Number of Image Sensing Elements : 2700 elements × 3 line
- Image Sensing Element Size : 10.5μm by 10.5μm on 10.5μm centers
- Photo Sensing Region : High sensitive and low dark current PN photodiode
- Distance Between Photodiode Array : 42μm (4 lines)
- Clock : 2 phase (5V)
- Internal Circuit : Sample & Hold circuit, Clamp circuit
- Package : 22 pin CERDIP package
- Color Filter : Red, Green, Blue

PIN CONNECTION



(TOP VIEW)

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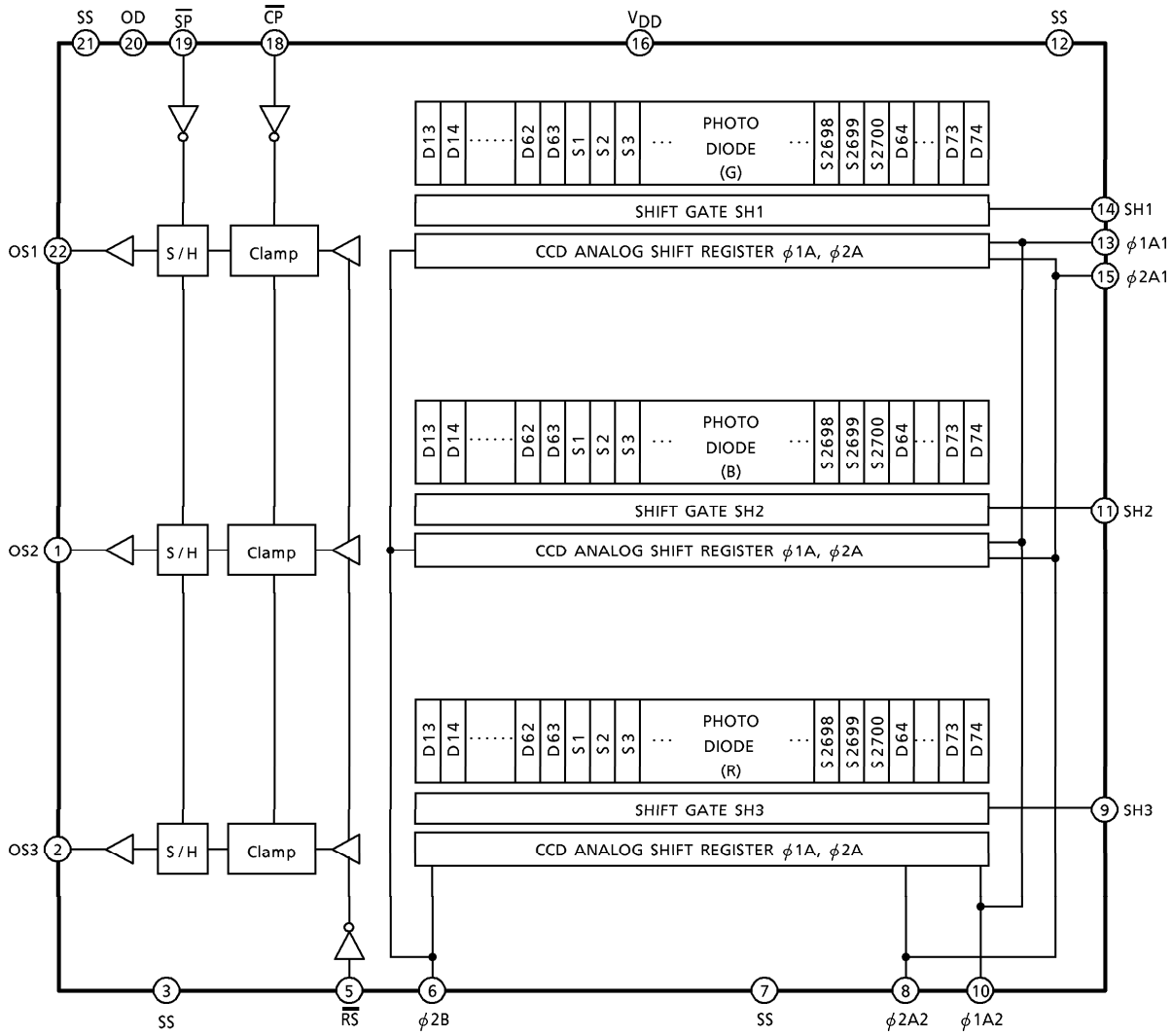
MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	V_{ϕ}	−0.3~8.0	V
Shift Pulse Voltage	V_{SH}		
Reset Pulse Voltage	$V_{\overline{RS}}$		
Sample and Hold Pulse Voltage	$V_{\overline{SP}}$		
Clamp Pulse Voltage	$V_{\overline{CP}}$		
Power Supply Voltage	V_{OD} V_{DD}	−0.3~15	V
Operating Temperature	T_{opr}	0~60	°C
Storage Temperature	T_{stg}	−25~85	°C

(Note 1) All voltage are with respect to SS terminals (Ground).

CIRCUIT DIAGRAM



PIN NAMES

PIN No.	SYMBOL	NAME	PIN No.	SYMBOL	NAME
1	OS2	Signal Output 2 (Blue)	12	OS1	Signal Output 1 (Green)
2	OS3	Signal Output 3 (Red)	13	SS	Ground
3	SS	Ground	14	OD	Power (Analog)
6	NC	Non Connection	15	$\overline{SP}$	Sample and Hold Gate
5	$\overline{RS}$	Reset Gate	16	$\overline{CP}$	Clamp Gate
6	ϕ2B	Final Stage Clock (Phase 2)	17	NC	Non Connection
7	SS	Ground	18	V_{DD}	Power (Digital)
8	ϕ2A2	Clock 2 (Phase 2)	19	ϕ2A1	Clock 1 (Phase 2)
9	SH3	Shift Gate 3	20	SH1	Shift Gate 1
10	ϕ1A2	Clock 2 (Phase 1)	21	ϕ1A1	Clock 1 (Phase 1)
11	SH2	Shift Gate 2	22	SS	Ground

OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{OD} = 12V, $V\phi = V_{RS} = V_{SH} = V_{CP}$ = 5V (pulse), $f\phi$ = 1.0MHz, $f_{\overline{RS}}$ = 1.0MHz,
LOAD RESISTANCE = 100kΩ, t_{INT} (INTEGRATION TIME) = 10ms,
LIGHT SOURCE = A LIGHT SOURCE + CM500S FILTER (t = 1.0mm))

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Sensitivity	R_R	12.2	17.4	22.6	V / (lx·s)	(Note 2)
	R_G	17.4	24.8	32.2		
	R_B	5.2	7.4	9.6		
Photo Response Non Uniformity	PRNU (1)	—	10	20	%	(Note 3)
	PRNU (3)	—	3	12	mV	(Note 4)
Saturation Output Voltage	V_{SAT}	3.0	3.5	—	V	(Note 5)
Saturation Exposure	SE	0.17	0.14	—	lx·s	(Note 6)
Dark Signal Voltage	V_{DRK}	—	2.0	6.0	mV	(Note 7)
Dark Signal Non Uniformity	DSNU	—	4.0	14.0	mV	(Note 7)
DC Power Dissipation	P_D	—	200	400	mW	
Total Transfer Efficiency	TTE	92	—	—	%	
Output Impedance	Z_o	—	0.5	1.0	kΩ	
DC Signal Output Voltage	V_{OS}	3.5	5.0	7.0	V	(Note 8)
Random Noise	$N_{D\sigma}$	—	1.2	—	mV	(Note 9)
Reset Noise	V_{RS}	—	2.1	—	V	(Note 8)

(Note 2) Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

(Note 3) PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

$$\text{PRNU (1)} = \frac{\Delta\chi}{\overline{\chi}} \times 100\ (\%)$$

When $\overline{\chi}$ is average of total signal outputs and $\Delta\chi$ is the maximum deviation from $\overline{\chi}$. The amount of incident light is shown below.

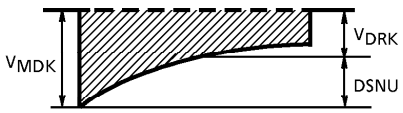
$$\text{Red} = \frac{1}{2}\ \text{SE},\ \text{Green} = \frac{1}{2}\ \text{SE},\ \text{Blue} = \frac{1}{4}\ \text{SE}$$

(Note 4) PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (Typ.).

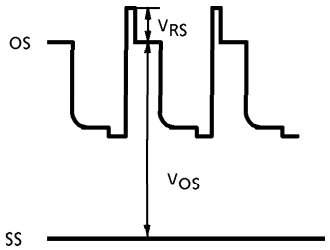
(Note 5) V_{SAT} is defined as minimum saturation output of all effective pixels.

(Note 6) Definition of SE : $\text{SE} = \frac{V_{SAT}}{R_G}$ (lx·s)

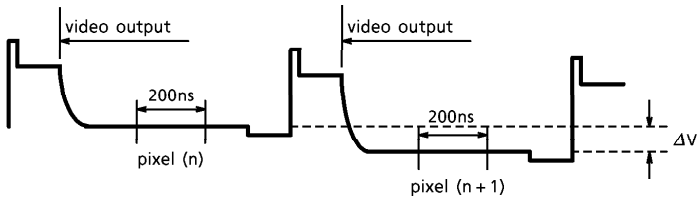
(Note 7) V_{DRK} is defined as average dark signal voltage of all effective pixels. DSNU is defined as different voltage between V_{DRK} and V_{MDK} when V_{MDK} is maximum dark signal voltage.



(Note 8) DC signal Output Voltage Reset Noise is defined as follows, but Reset Noise is a fixed pattern noise.



(Note 9) Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark conditions) calculated by the following procedure.



Output wave form (Effective pixels under dark condition)

1) Two adjacent pixels (pixel n and n + 1) in one reading are fixed as measurement points.
2) Each of the output level at video output periods averaged over 200ns period to get V (n) and V (n + 1).
3) V (n + 1) is subtracted from V (n) to get ΔV.

   $\Delta V = V(n) - V(n+1)$

4) The standard deviation of ΔV is calculated after procedure 2) and 3) are repeated 30 times (30 readings).

$$\Delta V = \frac{1}{30}\sum_{i=1}^{30} |\Delta Vi| \qquad \sigma = \sqrt{\frac{1}{30}\sum_{i=1}^{30} (|\Delta Vi| - \overline{\Delta V})^2}$$

5) Procedure 2), 3) and 4) are repeated 10 times to get 10 sigma values.
6) 10 sigma values are averaged.

$$\overline{\sigma} = \frac{1}{10}\sum_{j=1}^{10} \sigma j$$

7) $\overline{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify the random noise as follows.

$$N_{D\sigma} = \frac{1}{\sqrt{2}}\overline{\sigma}$$

OPERATING CONDITION

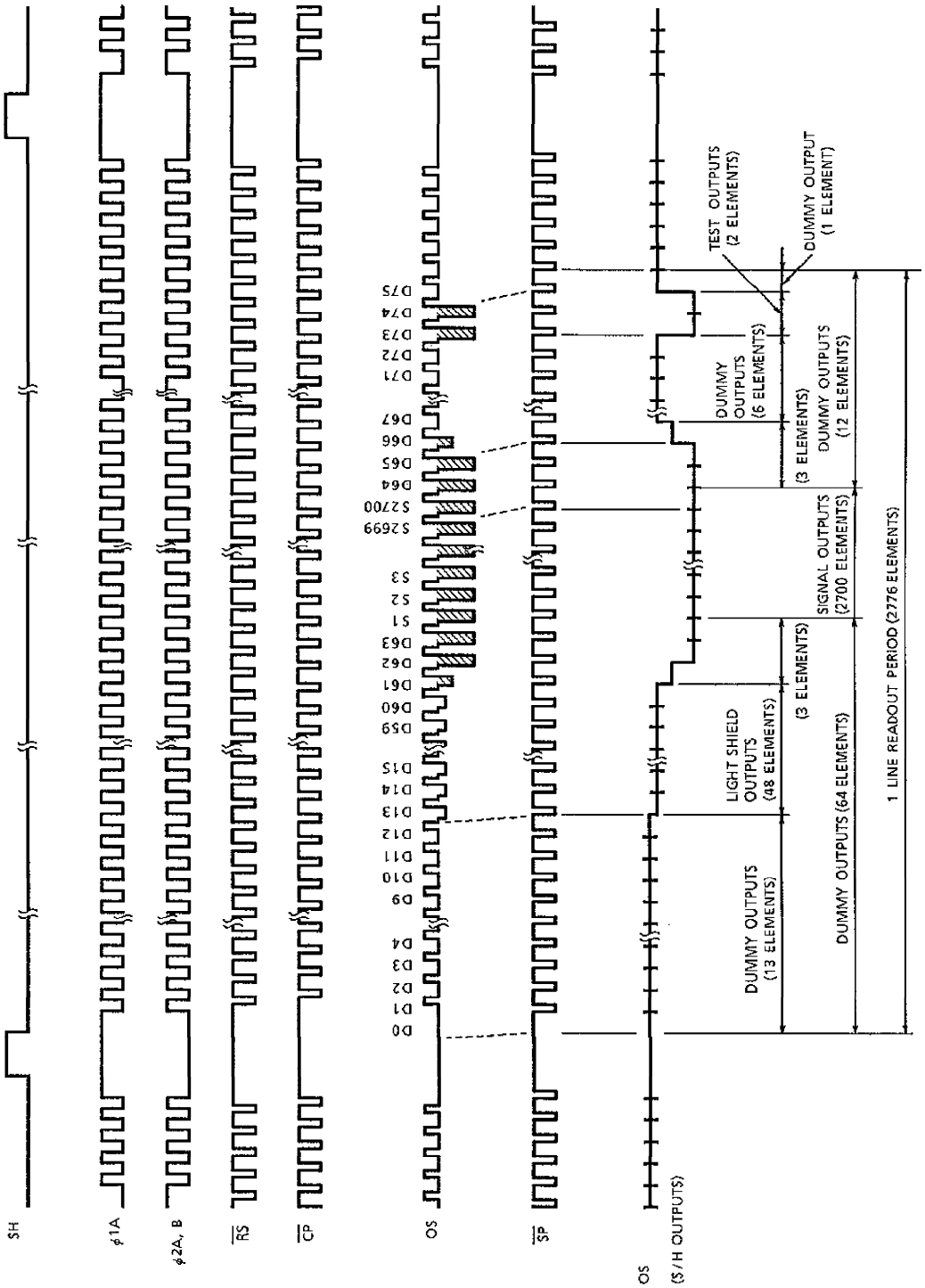
CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Pulse Voltage	"H" Level	$V_{\phi 1A}$	4.5	5.0	5.5	V	
	"L" Level	$V_{\phi 2A}$	0	—	0.5		
Final Stage Clock Pulse Voltage	"H" Level	$V_{\phi 2B}$	4.5	5.0	5.5	V	
	"L" Level		0	0	0.5		
Shift Pulse Voltage	"H" Level	V_{SH}	$V_{\phi A}$"H"-0.5	$V_{\phi A}$"H"	$V_{\phi A}$"H"	V	(Note 10)
	"L" Level		0	0	0.5		
Reset Pulse Voltage	"H" Level	$V_{\overline{RS}}$	4.5	5.0	5.5	V	
	"L" Level		0	0	0.5		
Sample and Hold Pulse Voltage	"H" Level	$V_{\overline{SP}}$	4.5	5.0	5.5	V	(Note 11)
	"L" Level		0	0	0.5		
Clamp Pulse Voltage	"H" Level	$V_{\overline{CP}}$	4.5	5.0	5.5	V	
	"L" Level		0	0	0.5		
Power Supply Voltage (Analog)		V_{OD}	11.4	12.0	13.0	V	
Power Supply Voltage (Digtal)		V_{DD}	11.4	12.0	13.0	V	

(Note 10) $V_{\phi A}$"H" means the high level voltage of $V_{\phi A}$ when SH pulse is high level.
(Note 11) Supply "L" Level to $\overline{SP}$ terminal when sample and hold circuitry is not used.

CLOCK CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	f_{ϕ}	—	1.0	5.0	MHz
Reset Pulse Frequency	$f_{\overline{RS}}$	—	1.0	5.0	MHz
Clamp Pulse Frequency	$f_{\overline{CP}}$	—	1.0	5.0	MHz
Sample and Hold Pulse Frequency	$f_{\overline{SP}}$	—	1.0	5.0	MHz
Clock Capacitance	$C_{\phi A}$	—	250	400	pF
Final Stage Clock Capacitance	$C_{\phi B}$	—	10	20	pF
Shift Gate Capacitance	C_{SH}	—	50	100	pF
Reset Gate Capacitance	$C_{\overline{RS}}$	—	10	20	pF
Clamp Gate Capacitance	$C_{\overline{CP}}$	—	10	20	pF
Sample and Hold Gate Capacitance	$C_{\overline{SP}}$	—	10	20	pF

TIMING CHART



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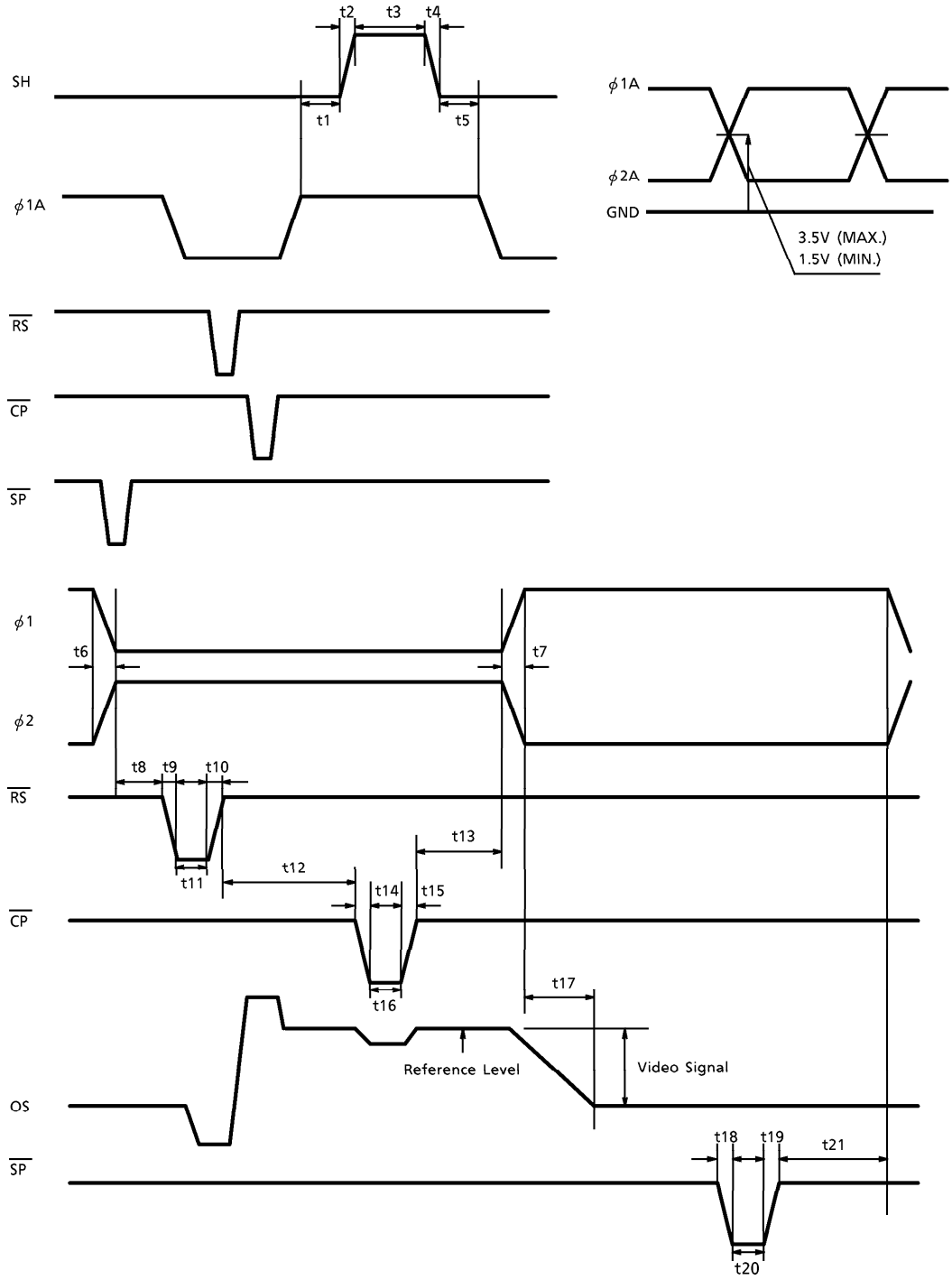
TIMING REQUIREMENTS (LINE CLAMP MODE)



TIMING REQUIREMENTS (Cont.)

CHARACTERISTIC	SYMBOL	MIN.	TYP. (Note 14)	MAX.	UNIT
Pulse Timing of SH and $\phi 1$	t1	120	1000	—	ns
	t5	200	1000	—	
SH Pulse Rise Time, Fall Time	t2, t4	0	50	—	ns
SH Pulse Width	t3	1000	2000	—	ns
$\phi 1$, $\phi 2$ Pulse Rise Time, Fall Time	t6, t7	0	50	—	ns
Pulse Timing of $\phi 2B$ and $\overline{RS}$	t8	20	40	—	ns
$\overline{RS}$ Pulse Rise Time, Fall Time	t9, t10	0	20	—	ns
$\overline{RS}$ Pulse Width	t11	40	80	—	ns
Pulse Timing of $\overline{RS}$ and $\overline{CP}$	t12	60	80	—	ns
Pulse Timing of $\phi 2B$ and $\overline{CP}$	t13	0	20	—	ns
$\overline{CP}$ Pulse Rise Time, Fall Time	t14, t15	0	20	—	ns
$\overline{CP}$ Pulse Width	t16	30	80	—	ns
Video Data Delay Time (Note 13)	t17	—	60	—	ns
$\overline{SP}$ Pulse Rise Time, Fall Time	t18, t19	0	20	—	ns
$\overline{SP}$ Pulse Width	t20	45	80	—	ns
Pulse Timing of $\overline{RS}$ and $\overline{SP}$	t21	0	20	—	ns

(Note 12) TYP. is the case of $f_{\overline{RS}} = 1.0$MHz.
(Note 13) Load Resistance is 100kΩ.

APPLICATION NOTE

Mode Select

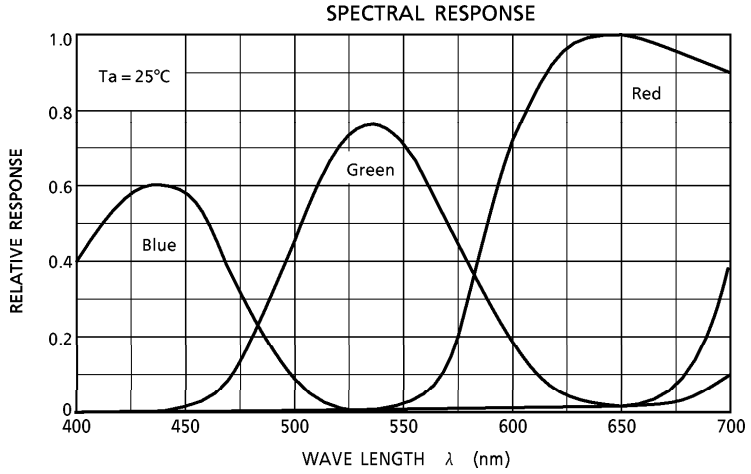
1. Sample & Hold

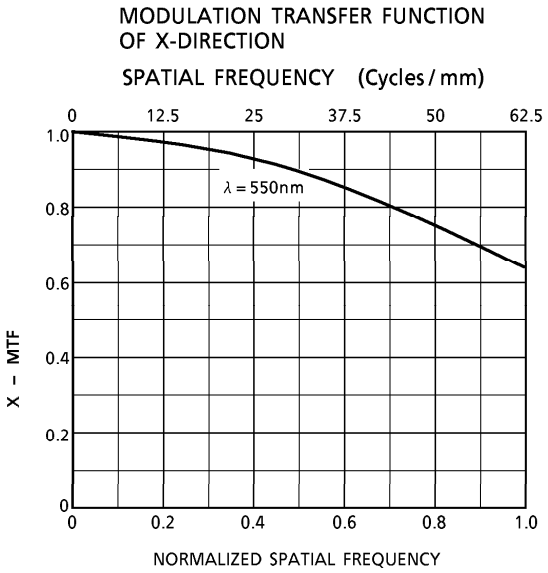
ON	OFF
$\overline{SP}$ Pulse	$\overline{SP}$ = Low

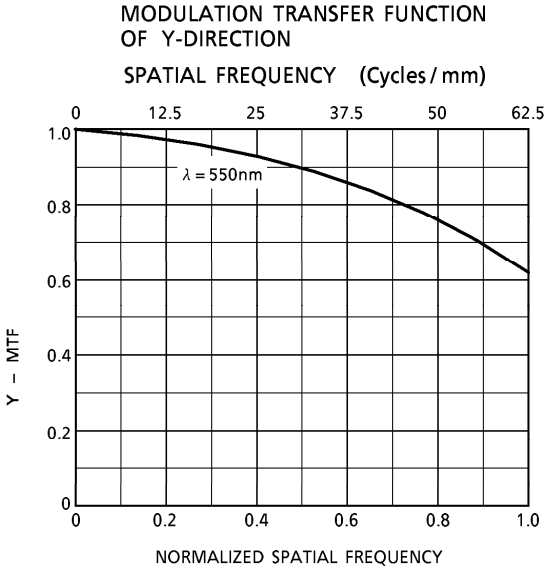
2. Clamp Mode

Bit Clamp	Line Clamp
$\overline{CP}$ Pulse	$\overline{CP} = \overline{SH}$

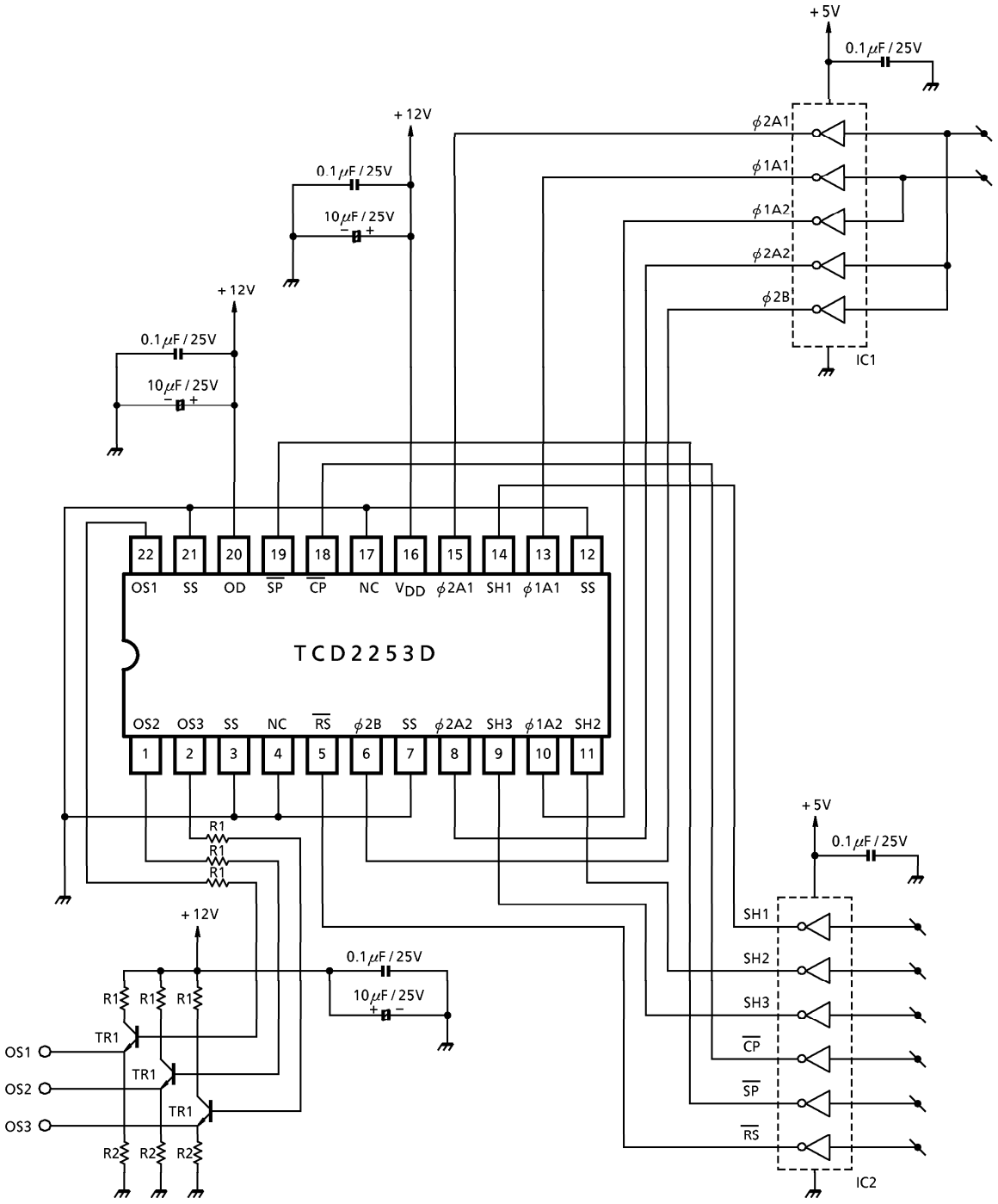
TYPICAL SPECTRAL RESPONSE







TYPICAL DRIVE CIRCUIT



IC1, 2 : TC74HC04AP
TR1 : 2SC1815-Y
R1 : 150Ω
R2 : 1500Ω

CAUTION

1. Window Glass

   The dust and stain on the glass window of the package degrade optical performance of CCD sensor.
   Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2.
   Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

   Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

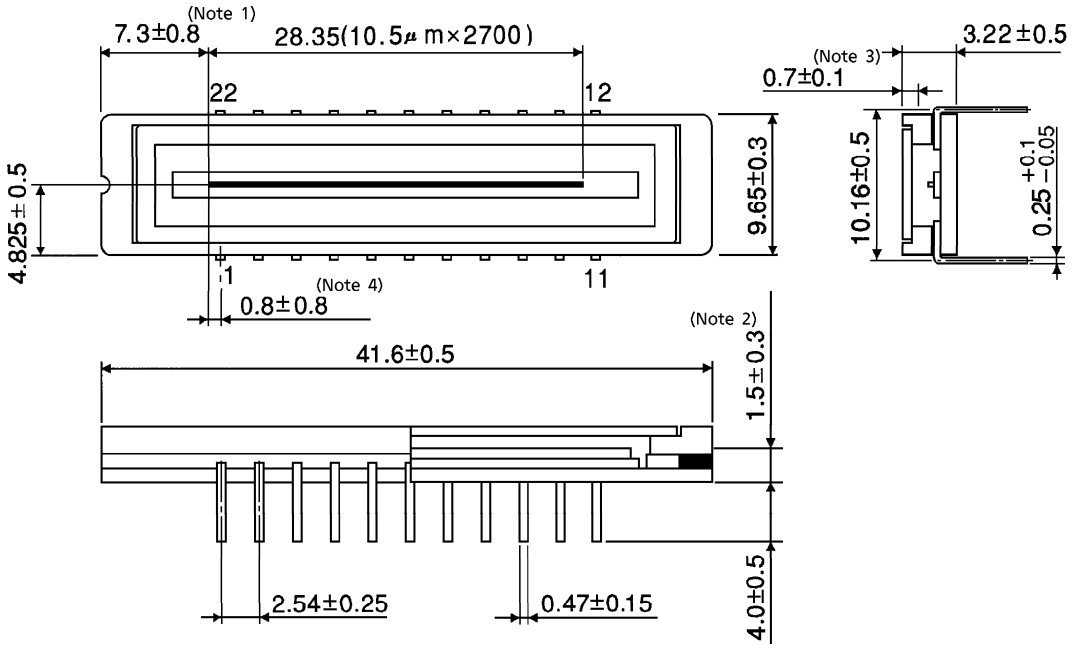
   CCD sensor is sensitive to infrared light.
   Note that infrared light component degrades resolution and PRNU of CCD sensor.

4. Lead Frame Forming
   Since this package is not strong against mechanical stress, you should not reform the lead frame.
   We recommend to use a IC-inserter when you assemble to PCB.

OUTLINE DRAWING

WDIP22-G-400-2.54C

Unit : mm



(Note 1) No.1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.
(Note 2) TOP OF CHIP TO BOTTOM OF PACKAGE.
(Note 3) GLASS THICKNESS (n = 1.5)
(Note 4) No.1 SENSOR ELEMENT (S1) TO EDGE OF No.1 PIN.

Weight : 4.5g (Typ.)

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