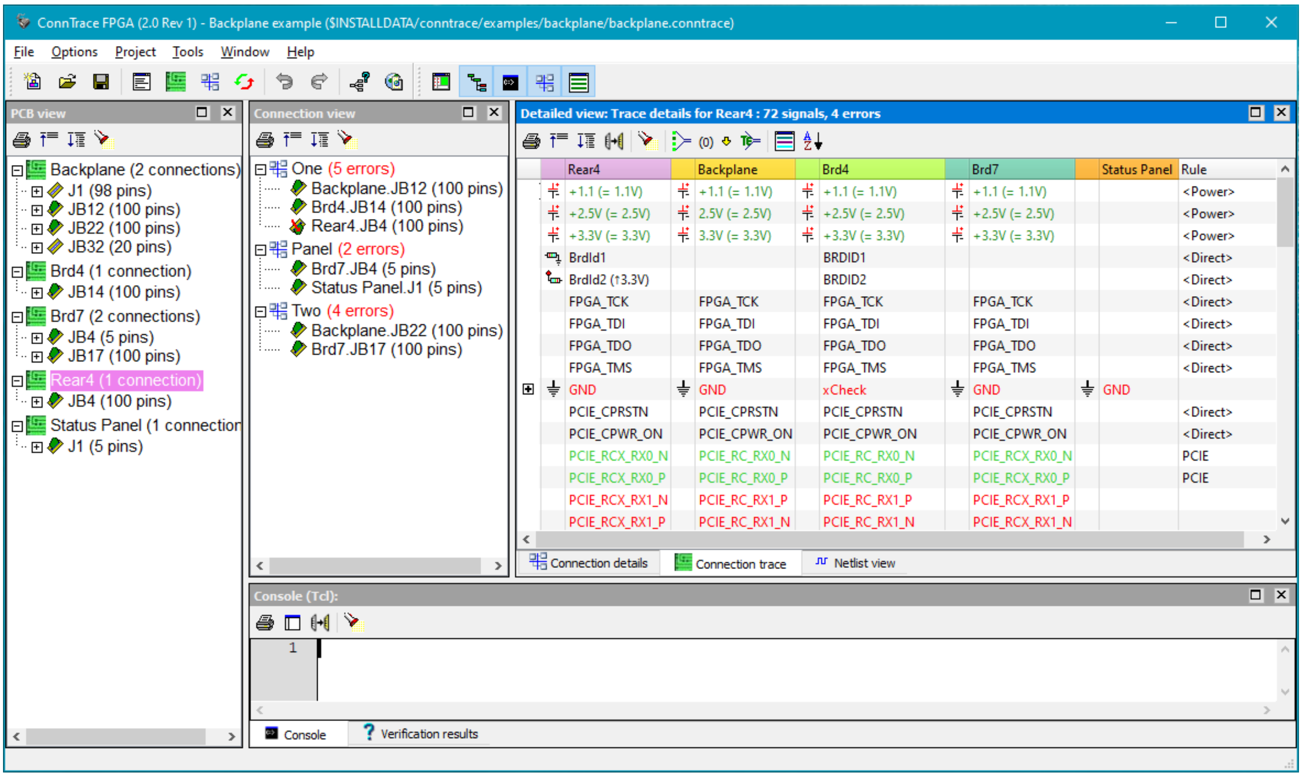
ConnTrace

Comparing hundreds of signals on PCBs in minutes

Complex electronic systems consist of one or more PCBs. They can be connected using a backplane, daughter boards and/or cables. Each schematic has to be manually checked for the correct signal names. Verifying interconnect between components on different boards is even more tedious. ConnTrace offers an easy and smart way to organize and view the schematic data. Instead of comparing two lists with hundreds of pins for each connector manually, you can load all the PCB netlist files in ConnTrace and define how boards are connected.



ConnTrace FPGA (2.0 Rev 1) - Backplane example ($INSTALLDATA/conntrace/examples/backplane/backplane.conntrace)

PCB view:

- Backplane (2 connections)
  - J1 (98 pins)
  - JB12 (100 pins)
  - JB22 (100 pins)
  - JB32 (20 pins)
- Brd4 (1 connection)
  - JB14 (100 pins)
- Brd7 (2 connections)
  - JB4 (5 pins)
  - JB17 (100 pins)
- Rear4 (1 connection)
  - JB4 (100 pins)
- Status Panel (1 connection
  - J1 (5 pins)

Connection view:

- One (5 errors)
  - Backplane.JB12 (100 pins)
  - Brd4.JB14 (100 pins)
  - Rear4.JB4 (100 pins)
- Panel (2 errors)
  - Brd7.JB4 (5 pins)
  - Status Panel.J1 (5 pins)
- Two (4 errors)
  - Backplane.JB22 (100 pins)
  - Brd7.JB17 (100 pins)

Detailed view: Trace details for Rear4 : 72 signals, 4 errors

Rear4	Backplane	Brd4	Brd7	Status Panel	Rule
+1.1 (= 1.1V)	+1.1 (= 1.1V)	+1.1 (= 1.1V)	+1.1 (= 1.1V)		<Power>
+2.5V (= 2.5V)	2.5V (= 2.5V)	+2.5V (= 2.5V)	+2.5V (= 2.5V)		<Power>
+3.3V (= 3.3V)	3.3V (= 3.3V)	+3.3V (= 3.3V)	+3.3V (= 3.3V)		<Power>
BrdId1		BRDID1			<Direct>
BrdId2 (↑3.3V)		BRDID2			<Direct>
FPGA_TCK	FPGA_TCK	FPGA_TCK	FPGA_TCK		<Direct>
FPGA_TDI	FPGA_TDI	FPGA_TDI	FPGA_TDI		<Direct>
FPGA_TDO	FPGA_TDO	FPGA_TDO	FPGA_TDO		<Direct>
FPGA_TMS	FPGA_TMS	FPGA_TMS	FPGA_TMS		<Direct>
GND	GND	xCheck	GND	GND	
PCIE_CPRSTN	PCIE_CPRSTN	PCIE_CPRSTN	PCIE_CPRSTN		<Direct>
PCIE_CPWR_ON	PCIE_CPWR_ON	PCIE_CPWR_ON	PCIE_CPWR_ON		<Direct>
PCIE_RCX_RX0_N	PCIE_RC_RX0_N	PCIE_RC_RX0_N	PCIE_RCX_RX0_N		PCIE
PCIE_RCX_RX0_P	PCIE_RC_RX0_P	PCIE_RC_RX0_P	PCIE_RCX_RX0_P		PCIE
PCIE_RCX_RX1_N	PCIE_RC_RX1_P	PCIE_RC_RX1_P	PCIE_RCX_RX1_P		
PCIE_RCX_RX1_P	PCIE_RC_RX1_N	PCIE_RC_RX1_N	PCIE_RCX_RX1_N		

ConnTrace: Connection trace of a Backplane design

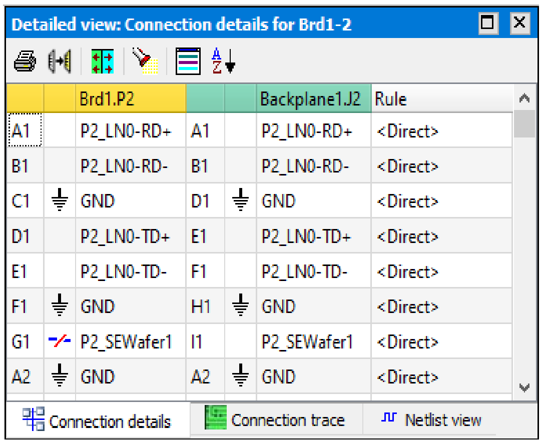
FPGAs on a board make verification even more complex. The programmable pins of an FPGA have generic names and the functional name will depend on the applied constraints. ConnTrace has a unique approach to visualise the FPGA as a virtual connector (containing a pin for each pin present on the FPGA) based on information from the FPGA pin or constraints file. This allows you to see how the internal signal names in the FPGA connect to the components on the board.

ConnTrace has 3 views for specific use cases. The connection details page shows the signal names from multiple boards over a connection. The connection trace show the connected signals on all the boards and how they match. The netlist view shows how signals connect to other (non-connector) components on the board(s).

Connection details

The connection details shows the pin number and signal name used on 2 connectors (or 3, for a backplane with a rear panel) for which you defined a connection. If any connector mapping has been applied you can see in this view how pins map.

In the image on the right (showing an OPEN VPX connector) you can see that pin D1 of P2 maps to E1 of J2. Potential errors are shown in red.



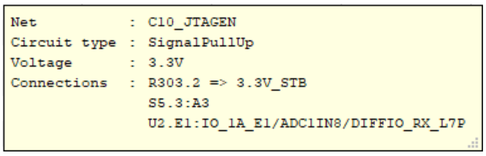
		Brd1.P2			Backplane1.J2	Rule
A1		P2_LN0-RD+	A1		P2_LN0-RD+	<Direct>
B1		P2_LN0-RD-	B1		P2_LN0-RD-	<Direct>
C1	⏚	GND	D1	⏚	GND	<Direct>
D1		P2_LN0-TD+	E1		P2_LN0-TD+	<Direct>
E1		P2_LN0-TD-	F1		P2_LN0-TD-	<Direct>
F1	⏚	GND	H1	⏚	GND	<Direct>
G1		P2_SEWafer1	I1		P2_SEWafer1	<Direct>
A2	⏚	GND	A2	⏚	GND	<Direct>

Connection details

Connection trace

The connection trace shows all nets of a selected board that connect to one of the other boards in your project in a large table. Signals that fail the matching test are displayed using a red color. ConnTrace also shows which signals in the netlist become connected to each other when the board is part of a system.

ConnTrace recognizes power and ground nets, pull-up and pull-down resistors in the netlist and shows the appropriate circuit type in the trace view (combined with the pull-up voltage). This makes it easy to see if different pull-up voltages have been used, or a voltage divider is created when connecting 2 boards. It can also look over resistors when internal net names are used.

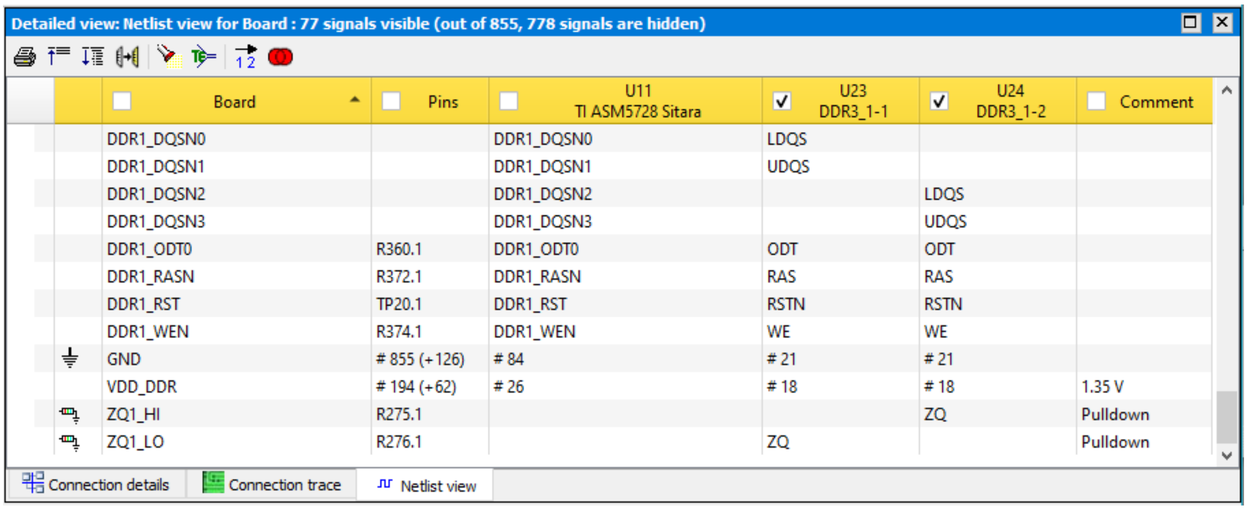


```
Net          : C10_JTAGEN
Circuit type : SignalPullUp
Voltage      : 3.3V
Connections  : R303.2 => 3.3V_STB
               S5.3:A3
               U2.E1:IO_1A_E1/ADC1IN8/DIFFIO_RX_L7P
```

Tooltips can be shown for each net showing you what kind of information ConnTrace extracted and which components and pins connect to the net.

Netlist view

The netlist view shows all nets defined on a board and how they connect to selected components that may be located on other boards. The ‘Pins’ column shows all components and pins connected to a net. If a net has a lot of connections (as is often the case with power and ground nets) a number is shown. Components can be selected to show in the table view in their own column and when possible the pin label (functional name) instead of the pin number is used. The column checkboxes and text filters make it easy to concentrate on components of interest. User notes (Comment column) can be added to every signal for documentation.

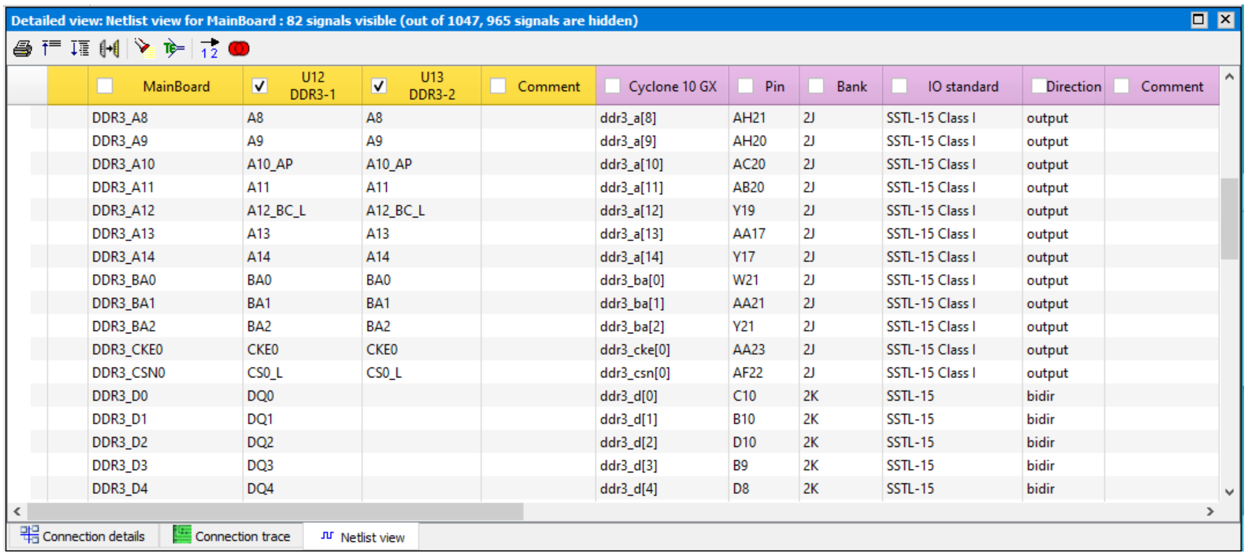

Detailed view: Netlist view for Board : 77 signals visible (out of 855, 778 signals are hidden)
Connection details
Connection trace
Netlist view

	□ Board	□ Pins	□ U11 TI ASM5728 Sitara	☑ U23 DDR3_1-1	☑ U24 DDR3_1-2	□ Comment
	DDR1_DQSN0		DDR1_DQSN0	LDQS		
	DDR1_DQSN1		DDR1_DQSN1	UDQS		
	DDR1_DQSN2		DDR1_DQSN2		LDQS	
	DDR1_DQSN3		DDR1_DQSN3		UDQS	
	DDR1_ODT0	R360.1	DDR1_ODT0	ODT	ODT	
	DDR1_RASN	R372.1	DDR1_RASN	RAS	RAS	
	DDR1_RST	TP20.1	DDR1_RST	RSTN	RSTN	
	DDR1_WEN	R374.1	DDR1_WEN	WE	WE	
⏚	GND	# 855 (+126)	# 84	# 21	# 21	
	VDD_DDR	# 194 (+62)	# 26	# 18	# 18	1.35 V
	ZQ1_HI	R275.1			ZQ	Pulldown
	ZQ1_LO	R276.1		ZQ		Pulldown

Verification strategies

ConnTrace uses various strategies to try to match signal names in the Connection trace. The first one is obvious: a direct string match. The second approach is power matching. When possible the voltage value of a power net is extracted and used. Next approach is fuzzy matching. ConnTrace treats all bus indicators (‘(‘, ‘[‘ and ‘<’) as the same and the fuzzy name comparator ignores underscores in names. So the signals bus[2], bus_2 and bus<2> all denote the same signal name. The last step is the rule based matching. These rules allow non matching names to match. The matching rules use regular expressions to quickly match related names. ConnTrace is equipped with a rule generator that determines all kinds of pre- and postfix rules. The matching rules can also be written and edited by the user.

FPGAs

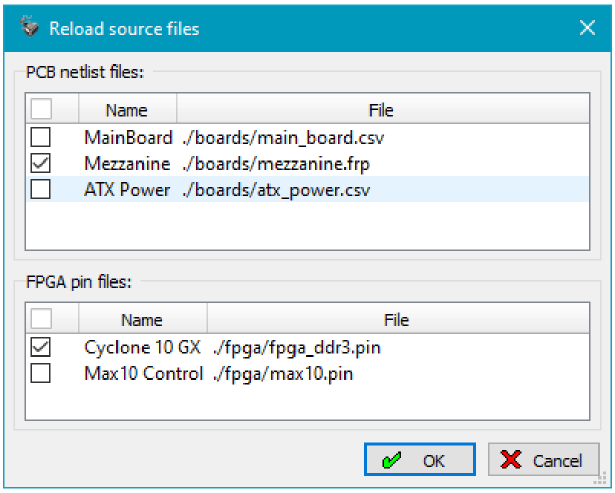

Detailed view: Netlist view for MainBoard : 82 signals visible (out of 1047, 965 signals are hidden)

□ MainBoard	☑ U12 DDR3-1	☑ U13 DDR3-2	□ Comment	□ Cyclone 10 GX	□ Pin	□ Bank	□ IO standard	□ Direction	□ Comment
DDR3_A8	A8	A8		ddr3_a[8]	AH21	2J	SSTL-15 Class I	output	
DDR3_A9	A9	A9		ddr3_a[9]	AH20	2J	SSTL-15 Class I	output	
DDR3_A10	A10_AP	A10_AP		ddr3_a[10]	AC20	2J	SSTL-15 Class I	output	
DDR3_A11	A11	A11		ddr3_a[11]	AB20	2J	SSTL-15 Class I	output	
DDR3_A12	A12_BC_L	A12_BC_L		ddr3_a[12]	Y19	2J	SSTL-15 Class I	output	
DDR3_A13	A13	A13		ddr3_a[13]	AA17	2J	SSTL-15 Class I	output	
DDR3_A14	A14	A14		ddr3_a[14]	Y17	2J	SSTL-15 Class I	output	
DDR3_BA0	BA0	BA0		ddr3_ba[0]	W21	2J	SSTL-15 Class I	output	
DDR3_BA1	BA1	BA1		ddr3_ba[1]	AA21	2J	SSTL-15 Class I	output	
DDR3_BA2	BA2	BA2		ddr3_ba[2]	Y21	2J	SSTL-15 Class I	output	
DDR3_CKE0	CKE0	CKE0		ddr3_cke[0]	AA23	2J	SSTL-15 Class I	output	
DDR3_CSN0	CS0_L	CS0_L		ddr3_csn[0]	AF22	2J	SSTL-15 Class I	output	
DDR3_D0	DQ0			ddr3_d[0]	C10	2K	SSTL-15	bidir	
DDR3_D1	DQ1			ddr3_d[1]	B10	2K	SSTL-15	bidir	
DDR3_D2	DQ2			ddr3_d[2]	D10	2K	SSTL-15	bidir	
DDR3_D3	DQ3			ddr3_d[3]	B9	2K	SSTL-15	bidir	
DDR3_D4	DQ4			ddr3_d[4]	D8	2K	SSTL-15	bidir	

The FPGA module allows you to define that a component is an FPGA and specify either a pin list or constraint file. The FPGA is shown as a separate board with only one component. The pin list or constraint file is processed and presented as a netlist. A (virtual) connection for the FPGA to the real board is automatically defined. The Connection trace shows how the FPGA signal names relate to the netlist on the board. The Netlist view shows pin number, bank number, IO standard and direction (depending on what is present for a specific FPGA vendor). This can be done for multiple FPGAs on the various boards, showing how they connect to each other and to other components like memories (over multiple boards).

Re-processing sources

Once a ConnTrace project is created it is easy to verify changes to existing PCBs or to add new boards to the project. Modified sources (both PCB and FPGA) can be re-processed in one action, while keeping all user defined data.


Reload source files

PCB netlist files:

□	Name	File
□	MainBoard	./boards/main_board.csv
☑	Mezzanine	./boards/mezzanine.frp
□	ATX Power	./boards/atx_power.csv

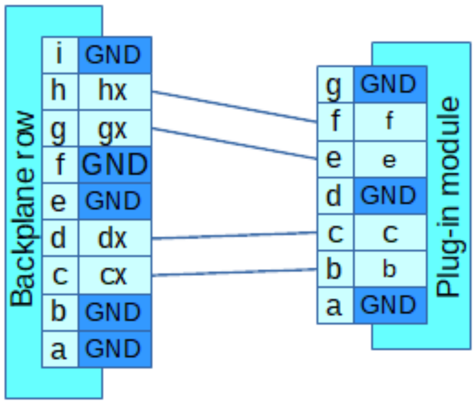
FPGA pin files:

□	Name	File
☑	Cyclone 10 GX	./fpga/fpga_ddr3.pin
□	Max10 Control	./fpga/max10.pin

Connector transformations

Some connector standards (like OPENVPX) have a different number of pins on the backplane connector and the plug-in board. The connections created also depend on odd and even pin numbers.

To handle these connectors ConnTrace is equipped with connector transformations. They allow you to re-define how connector pins connect between boards. These mappings can easily be extended by the user.



Even differential plug-in module to backplane pin mapping

HTML report

The HTML report function allows you to export the ConnTrace Connections and Trace views into an HTML document. It can be used to document the verification results.

Features and benefits	
• Rule based verification	• Replaces error prone labour
• Fits in any flow	• Reduces verification time
• Table based signal to component visibility	• Allows re-verification with little effort

FPGA Vendors	
• Intel (Altera)	• Microsemi (Actel)
• Lattice semiconductor	• Xilinx

Schematic capture / PCB Systems	
• Altium Designer	• DxDesigner generic netlist
• Cadence Allegro / Orcad Packager netlist	• DxDesigner Quick Connection View
• Cadence Allegro (Orcad) PCB (board file)	• DxDesigner packager cross reference netlist
• Cadence Telesis netlist	• Mentor Board Station netlist
• CADSTAR (Zuken)	• PADS ascii database
• CR-8000 / CR-5000 (Zuken)	• Generic CSV file

Operating Systems	System Requirements	License Configuration
• Windows (64 bit) 8.1 / 10 • Linux (x86_64, any recent distribution)	• 75 MB free disk space • 4 GB system RAM recommended	• Time based • Floating • FlexLM protected

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